Benefits of the MX Family of Devices

Each generation of FPGA devices makes complex system designs easier than designs of previous generations. New circuit design techniques are developed in response to the emerging needs of designers. The MX family of devices from Actel provides a wide range of key features that make it much easier for designers to meet performance, cost, and system interface requirements.

- Low internal signal skew for high performance between modules.
- Tuned clock buffer for high-speed clock-to-output (pin-to-pin) operation and maximum clock frequency.
- New MultiPlex I/O buffer design for high performance, low noise, and optimal I/O thresholds.
- Improved ActionProbe circuitry for high-speed probe operation.
- Abundant routing resources tuned to achieve high performance in A42MX36 SRAM blocks.

Performance improvements over other FPGAs are made possible by the new 0.45μ triple-layer metal process, and by the re-design of key circuits in the clocking, input buffer, output buffer, and logic module blocks in the MX family. Several of these circuits have been further tuned, based on the capacity of the MX device, providing even more performance increases over a simple process shrink used by some manufacturers. Secondary circuits also have been re-designed to provide better internal probe capabilities and to reduce signal skew.

MX devices are manufactured using Actel's non-volatile antifuse technology, which enables the devices to retain their configuration indefinitely. It is not necessary to store the configuration data in an external component. Designers can save up to 60% in component cost as well as saving valuable board space by choosing Actel's single-chip solution.

Additionally, Actel's antifuse technology provides for much better protection against design copying and pirating. There is no start-up configuration bitstream to intercept, since the devices are permanently programmed. Reverse engineering the antifuses themselves is impractical because there are so many of them; for example, there are >100,000 in the smallest device. Also, it is extremely difficult to differentiate between programmed and unprogrammed antifuses, even with an electron microscope.

The MX family delivers cost-effective performance through the use of an advanced 0.45μ triple-layer metal process. This process results in a die 25% smaller than devices of comparable gate counts from other FPGA vendors.

System interface requirements have become more complicated with the advent of 5.0V, 3.3V, PCI, low-power and hot-insertion standards. FPGA devices must be able to comply with a variety of these standards to solve the majority of current design problems. The Actel MultiPlex I/O architecture addresses all of these emerging system interface requirements.

- V_{CC} options: 5.0V core and 5.0V I/O for 5.0V-only operation. 3.3V core and 3.3V I/O for 3.3V-only operation. 5.0V core and 3.3V I/O for 3.3V interface with 5.0V tolerance.
- Programmable 5.0V, 3.3V, and PCI trip points on input buffers chip-wide.
- Array designed for high-performance operation at 5.0V as well as at 3.3V.
- Low-power mode to turn off input isolation devices, pump, input buffers, tri-state I/Os, and to turn off silicon signature sense amps (I_{CC} will be 100μA maximum).

The three most common voltage standards are supported on MX family devices. MX devices can be driven from a 5.0V power supply to ensure that outputs swing to a true 5.0 volts. This provides an additional 1.7 volts of noise margin over FPGAs which only swing to 3.3V when driving 5.0V components. MX FPGAs can also operate from a 3.3V supply for wholly 3.3V systems.

Additionally, many designers today need to mix both 5.0V and 3.3V components in one system. MX devices can operate with a 5.0V core supply and a 3.3V I/O supply for 3.3V interfaces requiring 5.0V tolerance.

Programmable 5.0V and 3.3V input voltage trip points are supported by programming a single, chip-wide selection fuse. This feature improves noise margin and skew in both 5.0V and 3.3V applications. Internal array performance is retained in 3.3V systems by using complementary pass gates that operate as fast at 3.3V as they do at 5.0V.

For low-power systems, power to the device can be reduced by putting it into a power-down mode. This mode turns off all inputs and outputs, and cuts current consumption to below 100μA.

The MX family supports the PCI standard by offering PCI-compliant I/Os on all pins. PCI drivers are included in the high-capacity members of the family, and comply with the stringent I/O requirements of the high-speed PCI bus specification. On A42MX24 and A42MX52, the PCI-compliant output drivers are enabled by programming the chip-wide PCI fuse. When PCI is not used, output drive is standard. The larger of the MX devices also have internal blocks of SRAM to simplify implementation of buffer memory, which is important in many PCI-based applications.

All Actel antifuse-based FPGAs have excellent power-on characteristics, and these have been improved upon in the MX family to comply with hot-insertion standards. The MX family devices are operational within 100µs of power-up, a feature important in systems that must be ready to respond quickly and predictably when power is interrupted. During power-up, I_{CC} stays within device specification, avoiding current spikes that can hamper operation immediately after power-up. During power-up and power-down, all tri-state outputs go into the tri-state mode. This feature supports applications that must ensure buses are not driven active during power transitions, which may occur during hot swapping or sleep mode entry/exit.

The benefits of power-up friendly devices are:

- Full operation of the device within 100µs of start of power-up, approximately 1000 times faster than parts from other FPGA vendors.
- I_{CC} spec not exceeded during power-up.
- During power-up, tri-state outputs are in high-impedance mode for power-down and hot-insertion compliance.
- During power-down, all inputs and outputs are in the high impedance state.

Actel’s MX FPGAs feature a segmented routing architecture with abundant routing tracks. This enables designers to achieve full utilization of the logic resources, even with 100% pin fixing.

Conclusion

The new MX family from Actel, with it’s MultiPlex I/O architecture, provides system designers with the right set of features to solve today’s multiple standard-based system interface problems—at the right cost and at the required performance levels.

Take it to a higher level.

http://www.actel.com

Actel Europe Ltd.
Daneshill House, Lutyens Close
Basingstoke, Hampshire RG24 8AG
United Kingdom
Tel: +44(0).1256.305600
Fax: +44(0).1256.355420

Actel Corporation
955 East Arques Avenue
Sunnyvale, California 94086
USA
Tel: 408.739.1010
Fax: 408.739.1540

Actel Japan
EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ka
Tokyo 150 Japan
Tel: +81.(0)3445.7671
Fax: +81.(0)3445.7668

5192640-1