RadTolerant RAD-PAK®
Field Programmable Gate Arrays

Features

Radiation Characteristics

- RAD-PAK® Package Technology from Space Electronics, Inc.
- Improved Total Ionizing Dose (TID) Survivability
  - Can Improve TID 2-10x Over Standard Package
  - Can Achieve > 100 KRads (Si) in Some Orbits
- Packages: 172-Pin and 256-Pin RAD-PAK® Ceramic Quad Flat Pack
- Offered as E-Flow (Actel Space Level Flow) and Class B

High Density and Performance

- 16,000 and 20,000 Gates
- 8,000 and 10,000 ASIC Equivalent Gates
- Up to 85 MHz On-Chip Performance
- Up to 228 User I/Os
- Up to Four Fast, Low-Skew Clock Networks

Easy Logic Integration

- Non-Volatile, User Programmable
- Pin-Compatible Commercial Devices Available for Prototyping
- Highly Predictable Performance with 100% Automatic Place and Route
- 100% Resource Utilization with 100% Pin-Locking
- Secure Programming Technology Prevents Reverse Engineering and Design Theft
- Permanently Programmed for Instantaneous Operation on Power-Up
- Unique In-System Diagnostic and Debug Facility with Silicon Explorer
- Actel Designer Series Design Tools, Supported by Cadence, Exemplar, Mentor Graphics, Model Tech, Synopsys, Synplicity and Viewlogic Design Entry and Simulation Tools

General Description

Actel builds the most reliable field programmable gate arrays (FPGAs) in the industry, with overall antifuse reliability ratings of less than 10 failures-in-time (FITs), corresponding to a useful life of more than 40 years. Actel FPGAs are production-proven, with more than five million devices shipped and more than one trillion antifuses manufactured. Actel devices are fully tested prior to shipment, with an out-going defect level of only 122 ppm. (Further reliability data is available in the "Actel Device Reliability Report" at http://www.actel.com/products/devices/hireldev.html.)

Product Family Profile

Device	RP1280A	RP14100A
Gates	16,000	20,000
ASIC Equivalent Gates	8,000	10,000
PLD Equivalent Gates	20,000	25,000
TTL Equivalent Package	200	250
20-Pin PAL Equivalent Packages	80	100
Logic Modules	1,232	1,377
S-Modules	624	697
C-Modules	608	680
User I/Os	140	228
CQFP Package Pin Count	172	256
Performance System Speed (Maximum)	40 MHz	60 MHz
Ordering Information		
Part Number (Class B)	RP1280A-CQ172B	RP14100A-CQ256B
Part Number (E-Flow)	RP1280A-CQ172E	RP14100A-CQ256E
Commercial Equivalent for Prototyping	A1280A-CQ172C	A14100A-CQ256C

Additionally, the programmable architecture of both the RP1280A and RP14100A offers high performance, design flexibility, and fast and inexpensive prototyping—all without the expense of test vectors, NRE charges, long lead times, and schedule and cost penalties for design refinements.

Recently, Actel joined with Space Electronics, Inc. (SEi) to combine Actel's antifuse-based FPGAs with SEi's RAD-PAK® package shielding technology. This technology incorporates radiation shielding in the FPGA package, eliminating the requirement for box- or board-level shielding and significantly improving the total ionizing dose survivability of Actel devices. The RP1280A and the RP14100A provide a high-reliability, low-risk, and fast time-to-launch solution that survives in a wide subset of Earth orbits and deep space environments.

The RP1280A device uses the A1280A die from the ACT 2 Family of Actel FPGAs in a RAD-PAK® package. It utilizes a two-module architecture, consisting of combinatorial modules (C-modules) and sequential modules (S-modules) optimized for both combinatorial and sequential designs. Based on Actel's patented channeled array architecture, the RP1280A has 8,000 ASIC-equivalent gates and 140 user I/Os.

The RP1280A device is fully pin- and function-compatible with the commercially-equivalent A1280A-CQ172C device for easy and inexpensive prototyping.

The RP14100A device uses the A14100A die in a RAD-PAK® package. This device is from the ACT 3 Family of Actel devices, which also utilizes the two-module architecture. The RP14100A offers additional device resources above the RP1280A, including increased gates (10,000 gate array equivalent gates), higher I/Os (228), and faster performance.

The RP14100A device is fully pin- and function-compatible with the commercially-equivalent A14100A-CQ256C device for easy and inexpensive prototyping.

Radiation Survivability

The bare die of both the RP1280A and RP14100A devices have some inherent total dose radiation survivability. The levels at which these bare die are able to survive varies by lot and device type. Actel provides Group E testing on the bare die that gives an indication of the lot characteristics. These results are provided for reference and customer evaluation, and the testing is performed to MIL-STD-883, Method 1019.5 by Space Electronics, Inc.

The radiation survivability levels of the RAD-PAK® devices varies due to a number of factors. The customer must evaluate and determine the applicability of these devices to their specific design and environmental requirements.

A summary of the radiation performance of Actel products ("Radiation Performance of Actel Products") can be found on the Actel Web site at:

http://www.actel.com/products/devices/radhard/radperf.pdf.

Radiation Performance of RAD-PAK® FPGAs

The components of natural radiation in space consist of trapped electrons, trapped protons, galactic cosmic rays, solar flare protons, and alpha particles. Depending on the orbit or deep space probe mission, the energy levels and magnitude of each component will vary. Since shielding effectiveness is dependent on the radiation component type and its energy level, the overall performance of RAD-PAK® FPGAs will vary with the application. Typical applications for two different orbits are shown below. Figure 1 and Figure 2 show the amount of mission dose which can be expected when a given amount of shielding is utilized for the two sample orbits.

A closer examination of the box shielding and RAD-PAK® shielding shows how the specific requirements for components are originated. Figure 3 below shows a typical orbit of 705 km, 98 degrees, for 5 years. Under these conditions, typical satellite designers might have a 40 to 120 mil aluminum box shield between the components and the outside environment. The figure shows that a shield of average thickness yields approximately 10 KRad (Si) inside the box shield. This specification becomes a design requirement for all of the active components in the satellite. When the RAD-PAK® shielding is added to the box shielding, as shown by the RP line, the total dose seen by the component is only 2.4 KRad (Si).

When a second orbit (35,790 km, 0 degrees, for 5 years) is examined using the same methodology, similar results can be achieved at higher total dose levels. Figure 4 below shows that average box shielding provides protection to 250 KRad(Si). Use of the RAD-PAK® design brings the total dose seen at the device level down to 5.8 KRad (Si).

The above discussion shows how use of RAD-PAK® products can shield significant levels of total dose seen at the die level. The ability of the Actel FPGA die to meet these lower levels of total dose radiation make the RAD-PAK® FPGAs a design choice for many space applications.

For proper application of the RAD-PAK® FPGA products, the following information should be available:

- Orbit or mission
- Satellite level shielding thickness and type

  or
- Mission dose vs. shielding thickness curves

Actel personnel can then assist in determining whether the RAD-PAK® FPGA devices are usable for the customers application and radiation requirements.

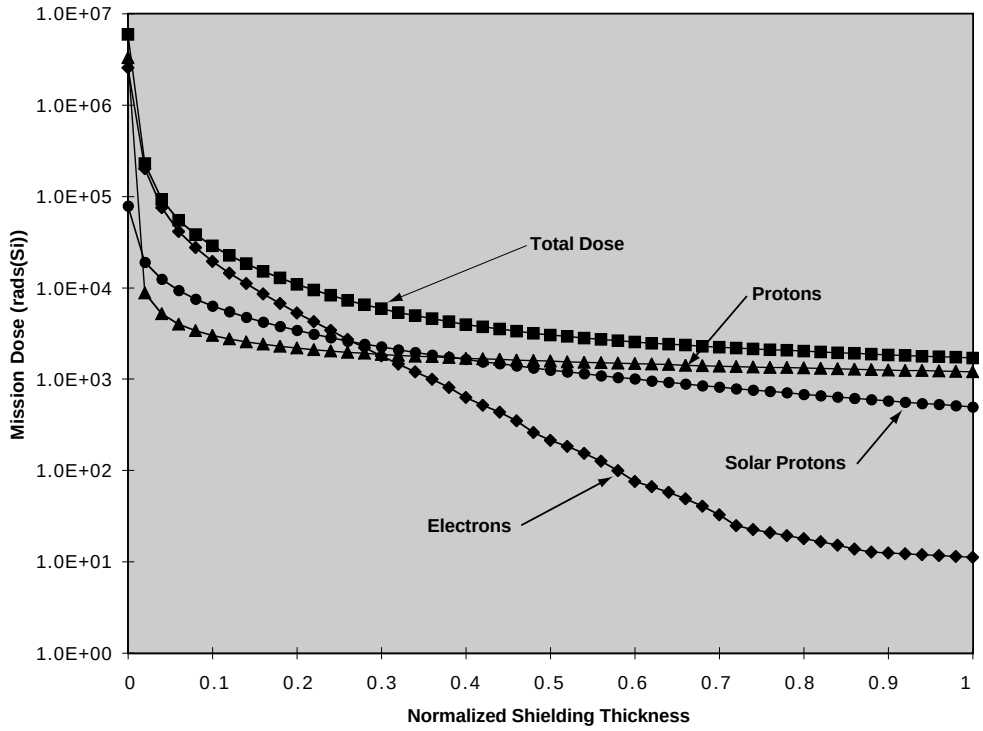


***Figure 1** • Space-Level Total Dose: Typical Orbit—705km, 98°, 5 years*

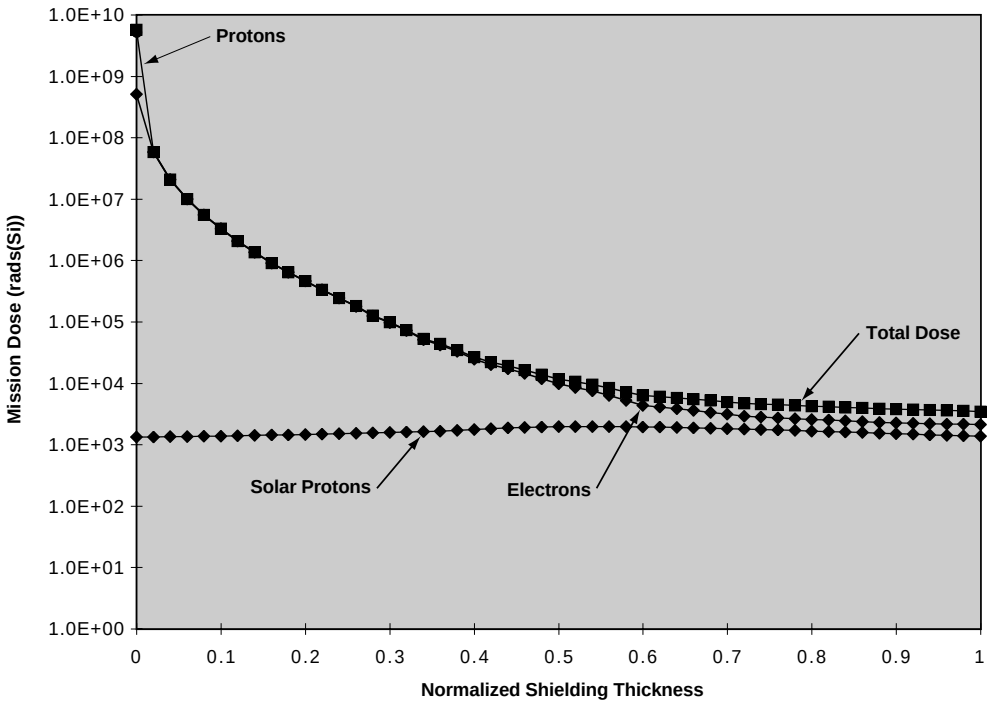


***Figure 2** • Space-Level Total Dose: Typical Orbit—35,790 km, 0°, 5 years*

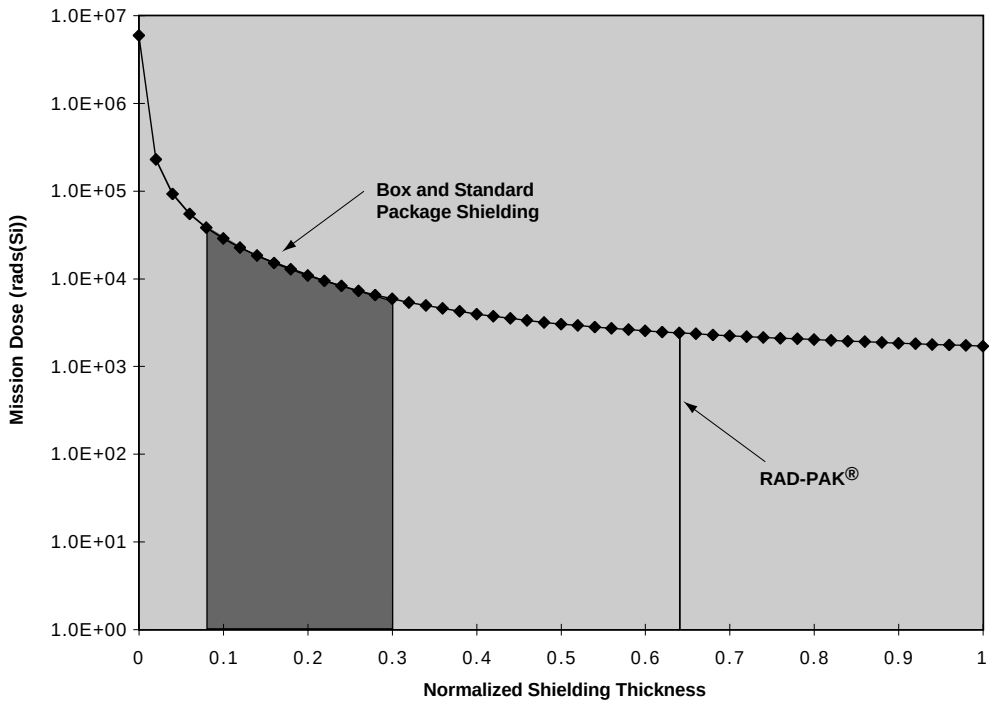


Figure 3 • *RAD-PAK® Total Dose Shielding: Typical Orbit—705 km, 98°, 5 years*

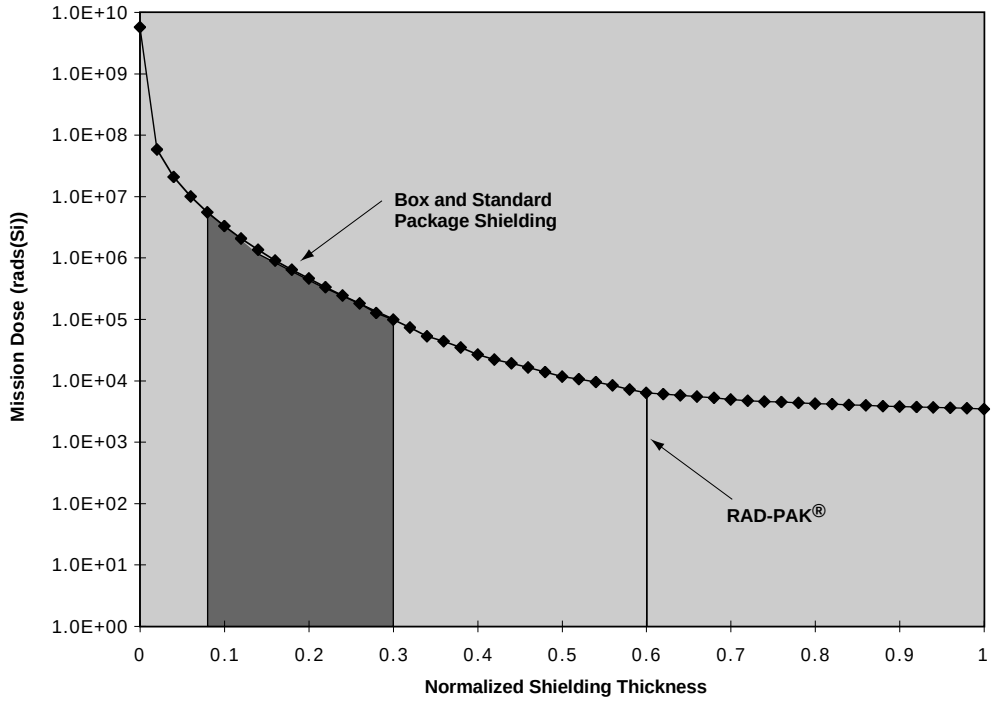


Figure 4 • *RAD-PAK® Total Dose Shielding: Typical Orbit—35,790 km, 0°, 5 years*

Disclaimer

All radiation performance information is provided for information purposes only and is not guaranteed. The total dose effects on the bare die is lot-dependent, and Actel does not warrant that future devices will continue to exhibit similar radiation characteristics. In addition, due to the nature of RAD-PAK® shielding, actual performance can vary widely due to a variety of factors, including but not limited to, characteristics of the orbit, radiation environment, proximity to satellite exterior, amount of inherent shielding from other sources within the satellite and actual bare die variations. For these reasons, Actel does not warrant any level of radiation survivability, and it is solely the responsibility of the customer to determine whether the device will meet the requirements of the specific design.

Design Tool Support

As with all Actel FPGAs, RAD-PAK® devices are fully supported by Actel's Designer Series development tools, which include:

- DirectTime for automated, timing-driven place and route;
- ACTgen for fast development using a wide range of macro functions; and
- ACTmap for logic synthesis.

Designer Series supports industry-leading VHDL- and Verilog-based design tools, including synthesis tools from industry leaders such as Exemplar Logic, Synplicity, and Synopsys.[1]

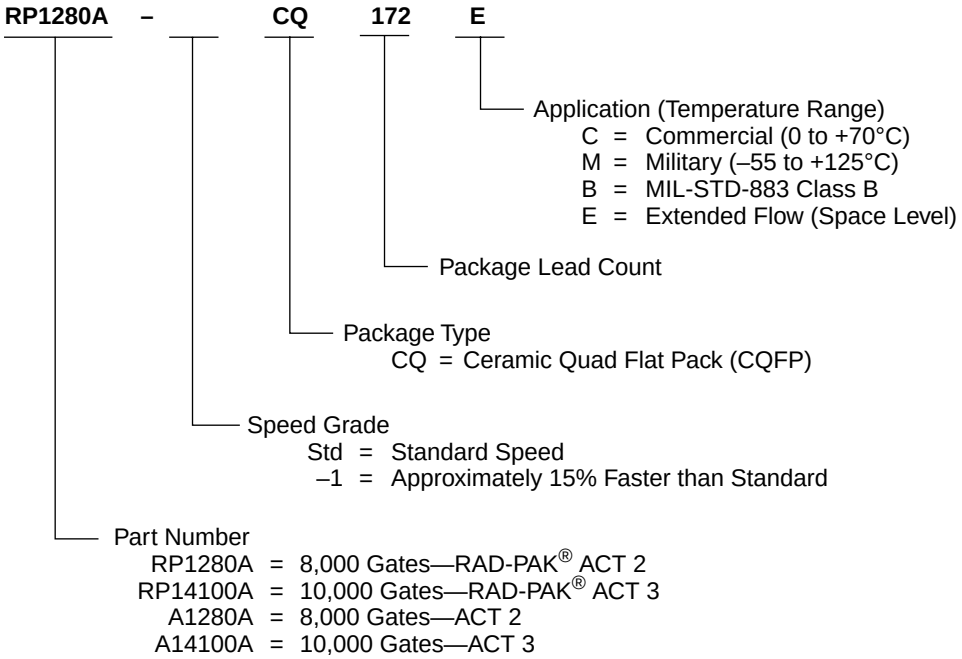
In addition, the RAD-PAK® devices are supported by Actel's new Silicon Explorer diagnostic and debugging tool kit. Silicon Explorer dramatically reduces verification time from several hours per cycle to a few seconds by enabling real-time, in-circuit debugging. Silicon Explorer includes:

- Probe Pilot, a high-speed signal acquisition and control tool that samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Probe Pilot features 18 probing channels and connects to the user's PC via a standard serial port connection.
- Diagnostic software, which turns the PC into a fully-featured, 100 MHz logic analyzer for easy graphical analysis of waveforms.

Silicon Explorer probes 100 percent of the device circuitry using Probe Pilot's powerful, 18-channel signal acquisition capability. Individual bugs are then isolated and passed to the user interface, providing the user with complete waveform data.

1. Designer Series also supports design entry and simulation tools from Cadence, Mentor Graphics, and Viewlogic.

RAD-PAK® Device Ordering Information



Product Plan

	Application			
	C	**M**	**B**	**E**
ACT 2				
RP1280A RAD-PAK® Device				
172-Pin Ceramic Quad Flat Pack (CQFP)	—	—	✔	✔
A1280A Device (Prototyping Use)				
172-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	—
ACT 3				
RP14100A RAD-PAK® Device				
256-Pin Ceramic Quad Flat Pack (CQFP)	—	—	P	P
A14100A Device (Prototyping Use)				
256-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	—

Applications: *C = Commercial*, *M = Military*, *B = MIL-STD-883 Class B*, *E = Extended Flow (Space Level)*

Availability: ✔ = *Available*, *P = Planned*, — = *Not Planned*

Device Resources

FPGA Device Type	**Logic Modules**	**Gate Array Equivalent Gates**	**User I/Os**	
			CQFP 172-Pin	**CQFP 256-Pin**
RP1280A/A1280A	1232	8000	140	—
RP14100A/A14100A	1377	10000	—	228

Architectural Overview

The RP1280A and RP14100A architecture is composed of fine-grained logic modules which produce fast, efficient logic designs. All devices are composed of logic modules, routing resources, clock networks, and I/O modules which are the building blocks for fast logic designs.

Logic Modules

Both devices contain two types of logic modules: combinatorial (C-modules) and sequential (S-modules).

The C-module, shown in Figure 5, implements the following function:

Y=!S1*!S0*D00+!S1*S0*D01+S1*!S0*D10+S1*S0*D11

where:

S0=A0*B0

S1=A1+B1

The S-module shown in Figure 6 is designed to implement high-speed sequential functions within a single logic module. The S-module implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D-type flip-flop or a transparent latch. To increase flexibility, the S-module register can be by-passed so it implements purely combinatorial logic.

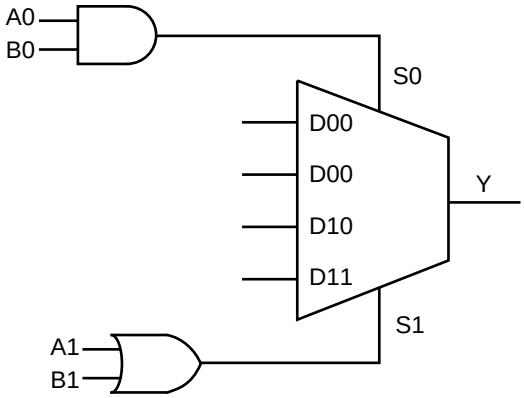


Figure 5 • *C-Module Implementation*

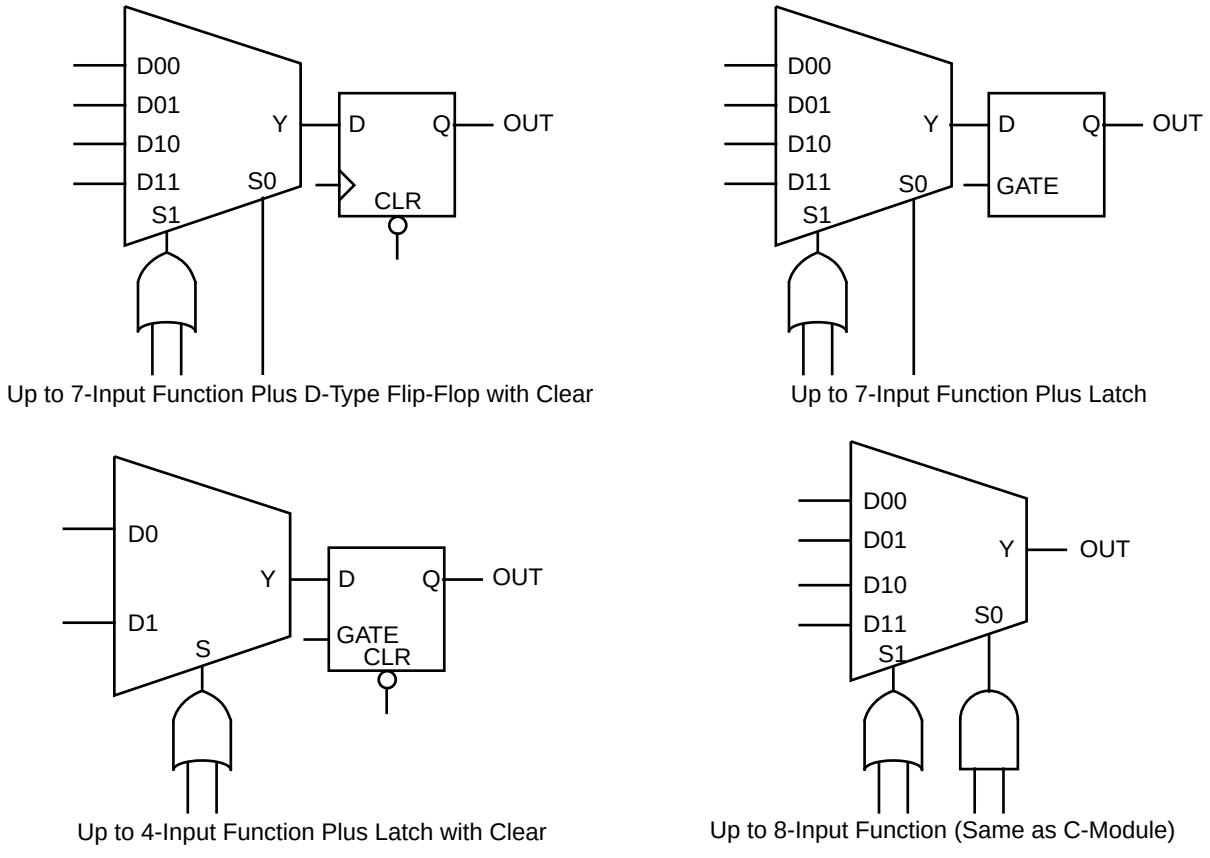


Figure 6 • *S-Module Implementation*

Flip-flops can also be created using two C-modules. The single event upset (SEU) characteristics differ between an S-module flip-flop and a flip-flop created using two C-modules. See the *Radiation Specifications* in this Data Sheet for details and the Actel Application Note, "Design Techniques for RadHard Field Programmable Gate Arrays" found at http://www.actel.com/products/radhard.html.

Pin Description

CLKA Clock A (Input)

TTL clock input for global clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

TTL clock input for global clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-Wired) Array Clock (Input)

RP14100A and A14100A only. TTL clock input for sequential modules. This input is directly wired to each S-module, offering clock speeds independent of the number of S-modules being driven. This pin can also be used as an I/O.

I/O Input/Output (Input, Output)

I/O pin functions as an input, output, tri-state, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW.

IOCLK Dedicated (Hard-Wired) I/O Clock (Input)

RP14100A and A14100A only. TTL clock input for I/O modules. This input is directly wired to each I/O module, offering clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

IOPCL Dedicated (Hard-Wired) I/O Preset/Clear (Input)

RP14100A and A14100A only. TTL input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

MODE Mode (Input)

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide ActionProbe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled HIGH when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA, I/O Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB, I/O Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} 5V Supply Voltage

HIGH supply voltage.

Actel MIL-STD-883 Product Flow

Step	Screen	883 Method	883—Class B Requirement
1.0	Internal Visual	2010, Test Condition B	100%
2.0	Temperature Cycling	1010, Test Condition C	100%
3.0	Constant Acceleration	2001, Test Condition E (Min), Y1, Orientation Only	100%
4.0	Seal a. Fine b. Gross	1014	 100% 100%
5.0	Particle Impact Noise Detection[1]	2020, Test Condition A	100%
6.0	Visual Inspection	2009	100%
7.0	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	100%
8.0	Burn-in Test	1015 Condition D 160 hours @ 125°C Min.	100%
9.0	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
10.0	Percent Defective Allowable	5%	All Lots
11.0	Final Electrical Test	In accordance with applicable Actel device specification	
	a. Static Tests (1) 25°C (Subgroup 1, Table I, 5005) (2) –55°C and +125°C (Subgroups 2, 3, Table I, 5005)		100%
	b. Dynamic and Functional Tests (1) 25°C (Subgroup 7, Table I, 5005) (2) –55°C and +125°C (Subgroups 8A and 8B, Table I, 5005)		100%
	c. Switching Tests at 25°C (Subgroup 9, Table I, 5005)		100%
12.0	Qualification or Quality Confirmation Inspection Test Sample Selection (Group A and Group B)	5005	All Lots
13.0	External Visual	2009	100%

Notes:

1. *Particle Impact Noise Detection (PIND) is included in the flow for RAD-PAK® devices, although it is not normally required in the MIL-STD-883 Class B flow.*

Actel Extended Flow[1]

Step	Screen	Method	Require-ment
1.	Wafer Lot Acceptance[2]	5007 with Step Coverage Waiver	All Lots
2.	Destructive In-Line Bond Pull[3]	2011, Condition D	Sample
3.	Internal Visual	2010, Condition A	100%
4.	Serialization		100%
5.	Temperature Cycling	1010, Condition C	100%
6.	Constant Acceleration	2001, Condition E (Min), Y_1 Orientation Only	100%
7.	Visual Inspection	2009	100%
8.	Particle Impact Noise Detection	2020, Condition A	100%
9.	Radiographic[4]	2012	Not Performed
10.	Pre-Burn-In Test	In accordance with applicable Actel device specification	100%
11.	Burn-in Test	1015, Condition D, 240 hours @ 125°C minimum	100%
12.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
13.	Reverse Bias Burn-In	1015, Condition C, 72 hours @ 150°C minimum	100%
14.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
15.	Percent Defective Allowable (PDA) Calculation	5%, 3% Functional Parameters @ 25°C	All Lots
16.	Final Electrical Test	In accordance with Actel applicable device specification	100%
	a. Static Tests		100%
	(1) 25°C (Subgroup 1, Table1)	5005	
	(2) –55°C and +125°C (Subgroups 2, 3, Table 1)	5005	
	b. Dynamic and Functional Tests		100%
	(1) 25°C (Subgroup 7, Table 15)	5005	
	(2) –55°C and +125°C (Subgroups 5 and 6, 8a and b, Table 1)	5005	
	c. Switching Tests at 25°C (Subgroup 9, Table 1)	5005	100%
17.	Seal	1014	100%
	a. Fine		
	b. Gross		
18.	Qualification or Quality Conformance Inspection Test Sample Selection	5005	Group A & Group B
19	External Visual	2009	100%

Notes:

1. *Actel offers the extended flow for customers that require additional screening beyond the requirements of MIL-STD-883, Class B. Actel is compliant to the requirements of MIL-STD-883, Paragraph 1.2.1, and MIL-I-38535, Appendix A. Actel is offering this extended flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883 Class S. The exceptions to Method 5004 are shown in notes 2 to 4 below.*
2. *Wafer lot acceptance is performed to Method 5007; however, the step coverage requirement as specified in Method 2018 must be waived.*
3. *Method 5004 requires a 100 percent, non-destructive bond pull to Method 2023. Actel substitutes a destructive bond pull to Method 2011, Condition D on a sample basis only.*
4. *Radiographic test is not performed since RAD-PAK® package technology screens all X-rays and the test results are uninformative.*

Absolute Maximum Ratings[1]

Free Air Temperature Range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[2]	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source Sink Current[5]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5V or less than GND – 0.5V, the internal protection diode will be forward-biased and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Military	Units
Temperature Range[1]	0 to +70	–55 to +125	°C
Power Supply Tolerance	±5	±10	%V_{CC}

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CQFP 172-pin package at military temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. military temp.}}{\theta_{jc}(\text{°C/W})} = \frac{150\text{°C} - 125\text{°C}}{6\text{°C/W}} = 4.2\text{W}$$

Package Type	Pin Count	θ_{jc}	Units
Ceramic Quad Flat Pack	176	6	°C/W
	256	TBD	°C/W

Electrical Specifications

Symbol	Parameter	Test Condition	Commercial		Military		Units
			Min.	Max.	Min.	Max.	
V_{OH}[1, 2]	HIGH Level Output	I_{OH} = –4 mA (CMOS)			3.7		V
		I_{OH} = –6 mA (CMOS)	3.84				V
V_{OL}[1, 2]	LOW Level Output	I_{OL} = +6 mA (CMOS)		0.33		0.4	V
V_{IH}	HIGH Level Input	TTL Inputs	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	LOW Level Input	TTL Inputs	–0.3	0.8	–0.3	0.8	V
I_{IN}	Input Leakage	V_I = V_{CC} or GND	–10	+10	–10	+10	µA
I_{OZ}	3-State Output Leakage	V_O = V_{CC} or GND	–10	+10	–10	+10	µA
C_{IO}	I/O Capacitance[3, 4]			10		10	pF
$I_{CC(S)}$	Standby V_{CC} Supply Current	V_I = V_{CC} or GND, I_O = 0 mA		2		20	mA
$I_{CC(D)}$	Dynamic V_{CC} Supply Current	See “Power Dissipation” Section					

Notes:

1. *Actel devices can drive and receive either CMOS or TTL signal levels. No assignment of I/Os as TTL or CMOS is required.*
2. *Tested one output at a time, V_{CC} = min.*
3. *Not tested; for information only.*
4. *V_{OUT} = 0V, f = 1 MHz*

General Power Equation

$$P = [I_{CC}standby + I_{CC}active] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} – V_{OH}) * M$$

Where:

I_{CC}standby is the current flowing when no inputs or outputs are changing.

I_{CC}active is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematical because their values depend on the family type, on design details, and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Actel FPGAs have small static power components that result in power dissipation lower than that of PALs or PLDs. By integrating multiple PALs or PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst-case conditions.

Family	I_{CC}	V_{CC}	Power
RP1280A, RP14100A, A1280A, A14100A	2 mA	5.25V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving HIGH or LOW and on the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33V will generate 42 mW with all outputs driving LOW, and 140 mW with all outputs driving HIGH.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency-dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1

$$\text{Power (uW)} = C_{EQ} * V_{CC}^2 * F \quad (1)$$

where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CC} is the power supply in volts (V).

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring I_{CC}active at a specified frequency and voltage for each circuit component of interest. Measurements are made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

CEQ Values for Actel FPGAs

	RP1280A A1280A	**RP14100A A14100A**
Modules (C_{EQM})	5.8	6.7
Input Buffers (C_{EQI})	12.9	7.2
Output Buffers (C_{EQO})	23.8	10.4
Routed Array Clock Buffer Loads (C_{EQCR})	3.9	1.6
Dedicated Clock Buffer Loads (C_{EQCD})	n/a	0.7
I/O Clock Buffer Loads (C_{EQCI})	n/a	0.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piece-wise linear summation over all components. Since the RP1280A and A1280A have two routed array clocks, the dedicated_Clk and IO_Clk terms do not apply. For RP14100A and A14100A devices, all terms will apply.

$$\text{Power} = V_{CC}^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{dedicated\_Clk} + (s_2 * C_{EQCI} * f_{s2})_{IO\_Clk}] \quad (2)$$

where:

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q_1 = Number of clock loads on the first routed array clock

q_2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

s_1 = Fixed number of clock loads on the dedicated array clock (RP14100A, A14100A only)

s_2 = Fixed number of clock loads on the dedicated I/O clock (RP14100A, A14100A only)

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_{EQCD} = Equivalent capacitance of dedicated array clock in pF

C_{EQCI} = Equivalent capacitance of dedicated I/O clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

f_{s1} = Average dedicated array clock rate in MHz (RP14100A, A14100A only)

f_{s2} = Average dedicated I/O clock rate in MHz (RP14100A, A14100A only)

Fixed Capacitance Values for Actel FPGAs (pF)

Device Type	r_1 routed_Clk1	r_2 routed_Clk2
RP1280A, A1280A	168	168
RP14100A, A14100A	195	195

Fixed Clock Loads (s_1/s_2—ACT 3 Only)

Device Type	s_1 Clock Loads on Dedicated Array Clock	s_2 Clock Loads on Dedicated I/O Clock
RP14100A, A14100A	697	228

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The guidelines in the table below are meant to represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation.

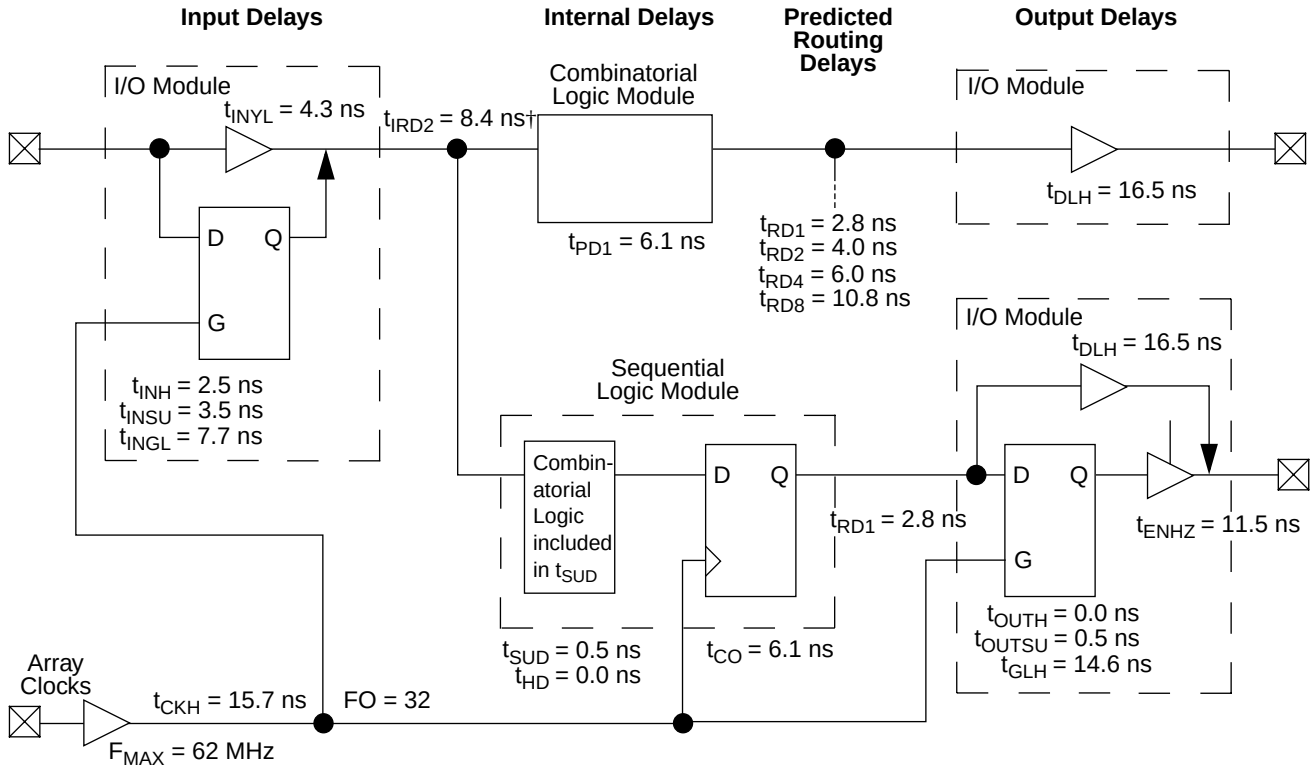
RP1280A, A1280A

Logic Modules (m)	=	80% of Combinatorial Modules
Input Switching (n)	=	# Inputs/4
Outputs Switching (p)	=	# Outputs/4
First Routed Array Clock Loads (q_1)	=	40% of Sequential Modules
Second Routed Array Clock Loads (q_2)	=	40% of Sequential Modules
Load Capacitance (C_L)	=	35 pF
Average Logic Module Switching Rate (f_m)	=	F/10
Average Input Switching Rate (f_n)	=	F/5
Average Output Switching Rate (f_p)	=	F/10
Average First Routed Array Clock Rate (f_{q1})	=	F
Average Second Routed Array Clock Rate (f_{q2})	=	F/2
Average Dedicated Array Clock Rate (f_{s1})	=	n/a
Average Dedicated I/O Clock Rate (f_{s2})	=	n/a

RP14100A, A14100A

Logic Modules (m)	=	80% of Combinatorial Modules
Input Switching (n)	=	# Inputs/4
Outputs Switching (p)	=	# Outputs/4
First Routed Array Clock Loads (q_1)	=	40% of Sequential Modules
Second Routed Array Clock Loads (q_2)	=	40% of Sequential Modules
Load Capacitance (C_L)	=	35 pF
Average Logic Module Switching Rate (f_m)	=	F/10
Average Input Switching Rate (f_n)	=	F/5
Average Output Switching Rate (f_p)	=	F/10
Average First Routed Array Clock Rate (f_{q1})	=	F/2
Average Second Routed Array Clock Rate (f_{q2})	=	F/2
Average Dedicated Array Clock Rate (f_{s1})	=	F
Average Dedicated I/O Clock Rate (f_{s2})	=	F

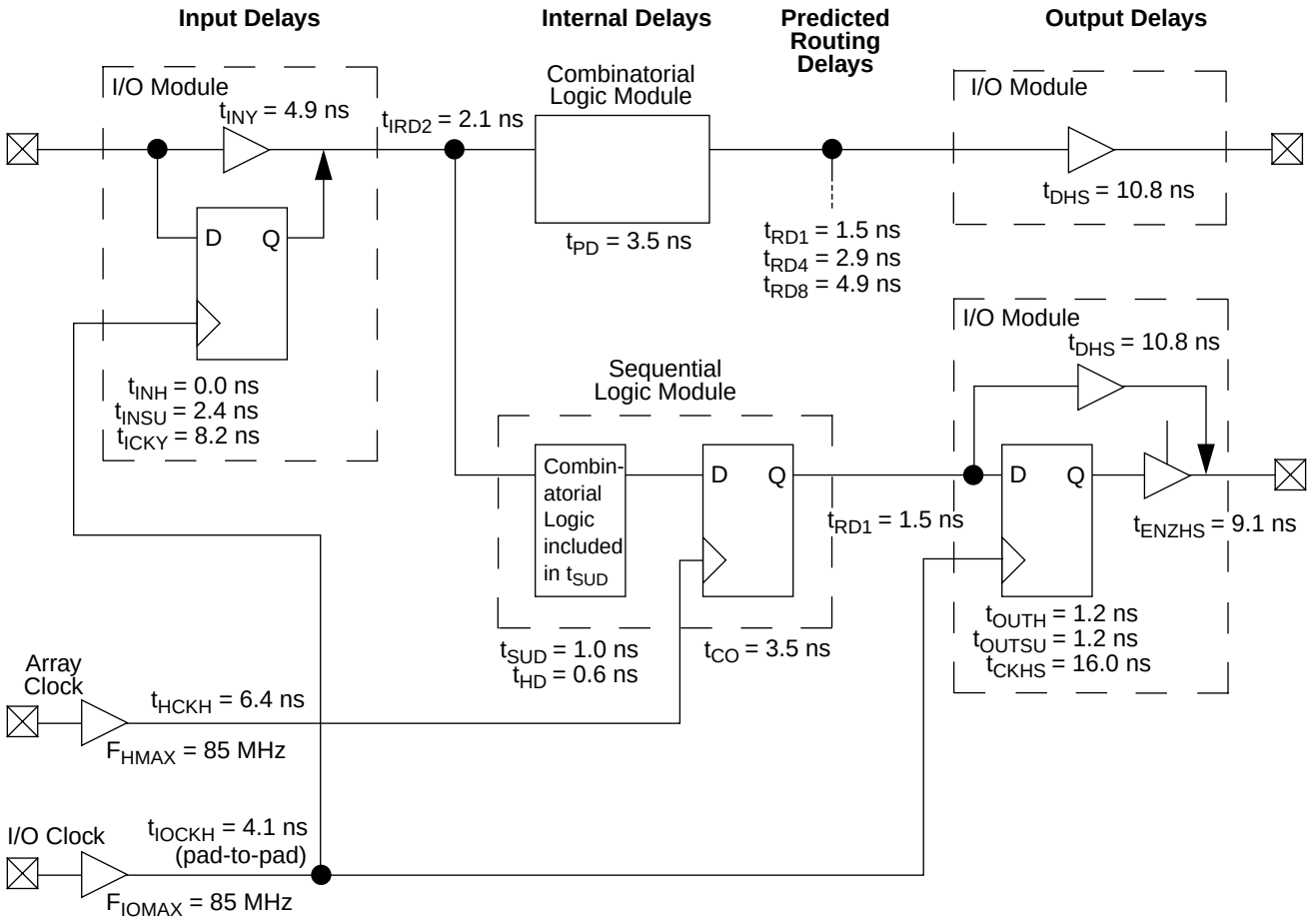
RP1280A, A1280A Timing Model*



**Values shown for RP1280A at worst-case military conditions.*

† Input module predicted routing delay

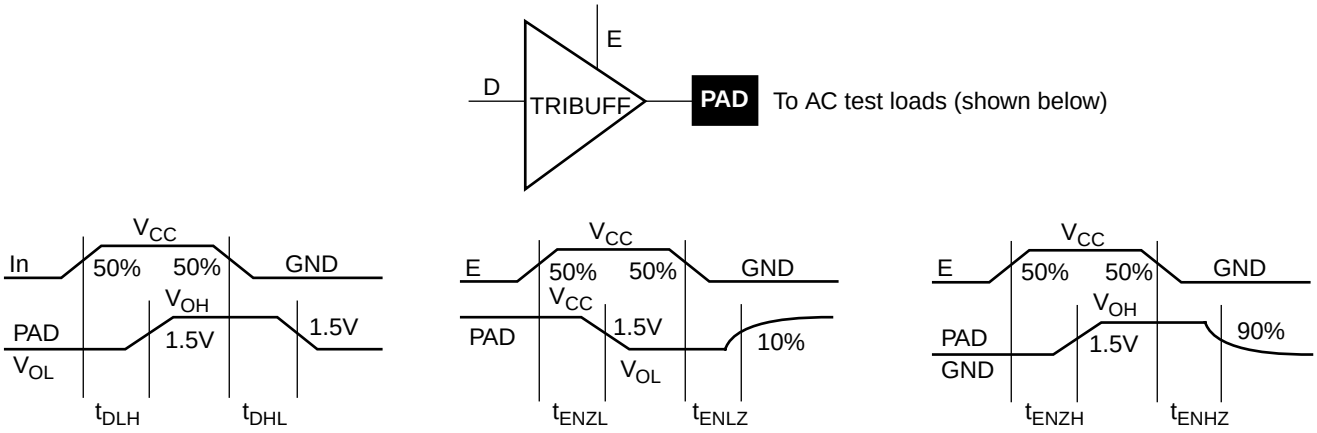
RP14100A, A14100A Timing Model*



**Values shown for RP14100A at worst-case military conditions.*

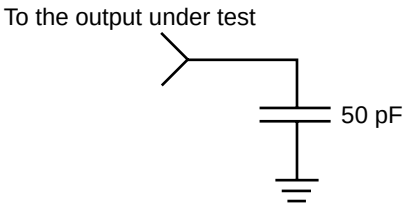
Parameter Measurement

Output Buffer Delays

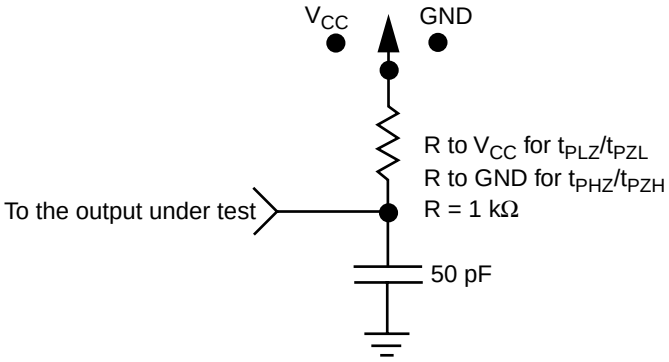


AC Test Load

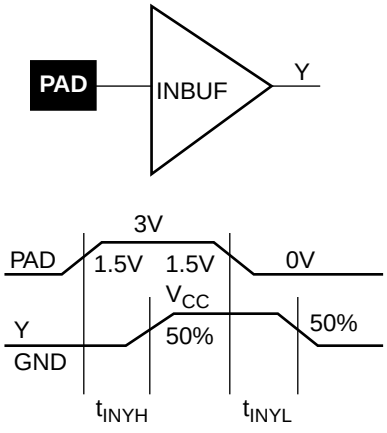
Load 1
(Used to measure propagation delay)



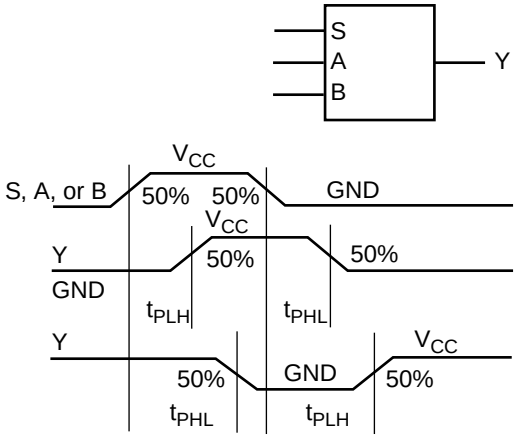
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

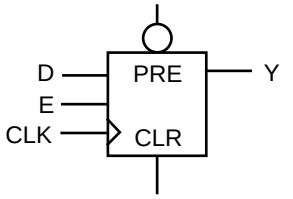


Combinatorial Macro Delays

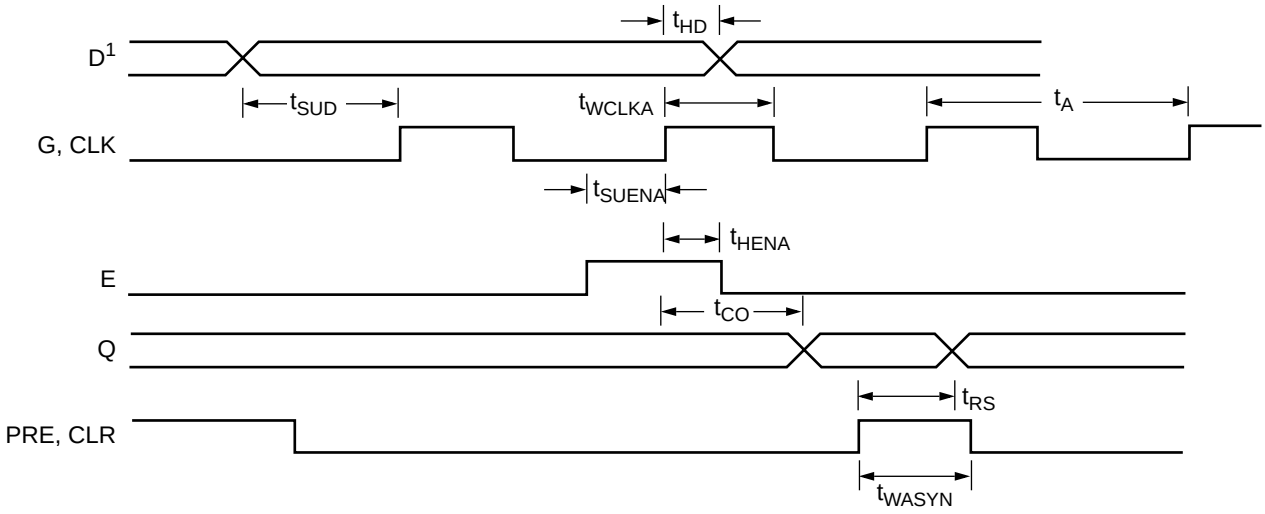


Sequential Timing Characteristics

Flip-Flops and Latches (RP1280A, A1280A)



(Positive Edge-Triggered)

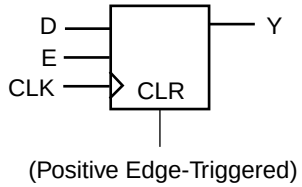


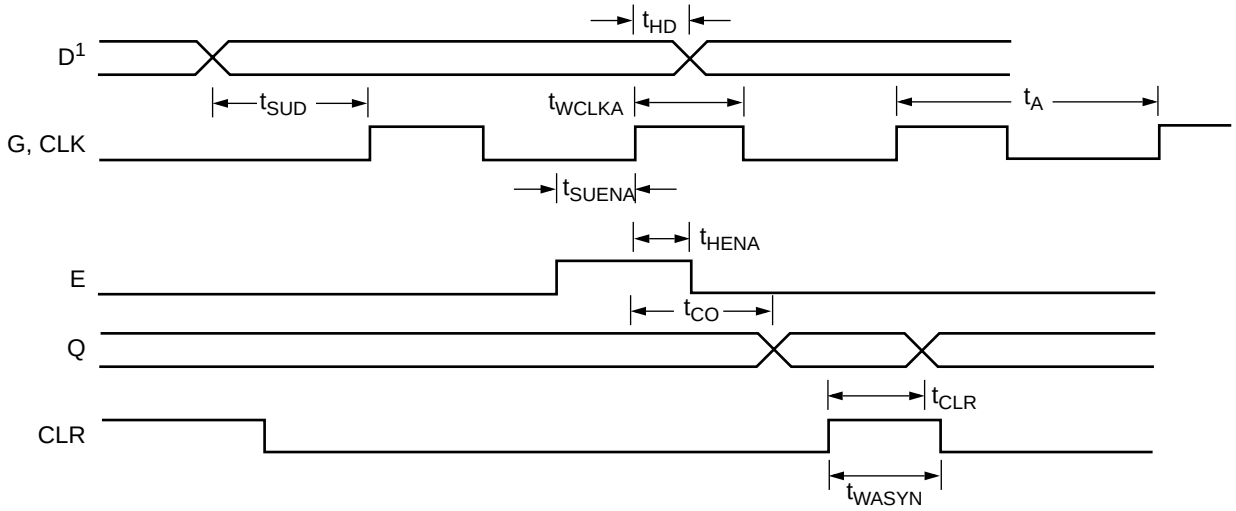
Note:

1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

Sequential Timing Characteristics (continued)

Flip-Flops and Latches (RP14100A, A14100A)



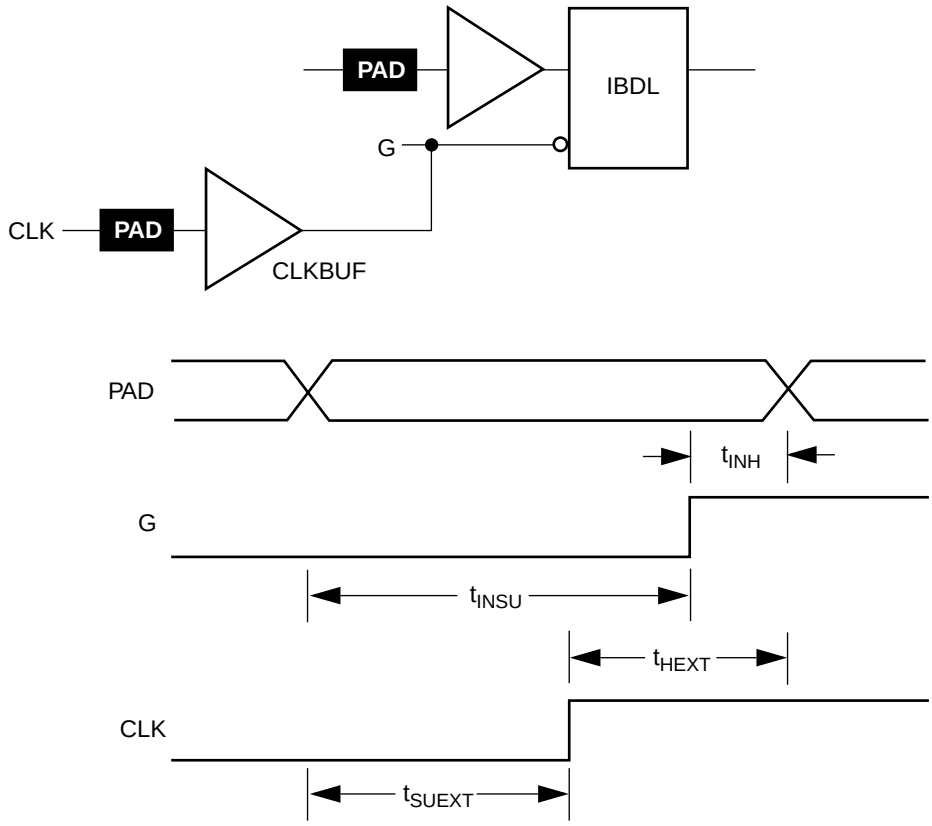


Note:

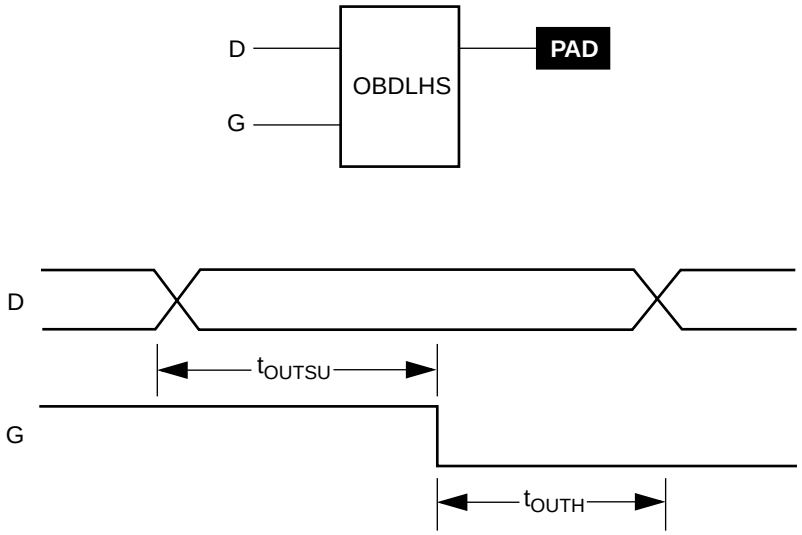
1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

Sequential Timing Characteristics (continued)

Input Buffer Latches (RP1280A, A1280A)



Output Buffer Latches (RP1280A, A1280A)



RP1280A, A1280A Timing Characteristics

(Worst-Case Military Conditions)

Logic Module Propagation Delays[1]		‘–1 Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		5.2		6.1	ns
t_{CO}	Sequential Clock-to-Q		5.2		6.1	ns
t_{GO}	Latch G-to-Q		5.2		6.1	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		5.2		6.1	ns
Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		2.4		2.8	ns
t_{RD2}	FO=2 Routing Delay		3.4		4.0	ns
t_{RD3}	FO=3 Routing Delay		4.2		4.9	ns
t_{RD4}	FO=4 Routing Delay		5.1		6.0	ns
t_{RD8}	FO=8 Routing Delay		9.2		10.8	ns
Sequential Timing Characteristics[3, 4]						
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.5		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	1.3		1.3		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	7.4		8.6		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	7.4		8.6		ns
t_{A}	Flip-Flop Clock Input Period	16.4		22.1		ns
t_{INH}	Input Buffer Latch Hold	2.5		2.5		ns
t_{INSU}	Input Buffer Latch Set-Up	3.5		3.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.5		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		60		41	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-Up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External set-up/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal set-up (hold) time.*

RP1280A, A1280A Timing Characteristics (continued)

(Worst-Case Military Conditions)

Input Module Propagation Delays			'–1' Speed		'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad-to-Y HIGH			4.0		4.7	ns
t_{INYL}	Pad-to-Y LOW			3.6		4.3	ns
t_{INGH}	G-to-Y HIGH			6.9		8.1	ns
t_{INGL}	G-to-Y LOW			6.6		7.7	ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			6.2		7.3	ns
t_{IRD2}	FO=2 Routing Delay			7.2		8.4	ns
t_{IRD3}	FO=3 Routing Delay			7.7		9.1	ns
t_{IRD4}	FO=4 Routing Delay			8.9		10.5	ns
t_{IRD8}	FO=8 Routing Delay			12.9		15.2	ns
Global Clock Network							
t_{CKH}	Input LOW to HIGH	FO = 32 FO = 384		13.3 17.9		15.7 21.1	ns
t_{CKL}	Input HIGH to LOW	FO = 32 FO = 384		13.3 18.2		15.7 21.4	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32 FO = 384	6.9 7.9		8.1 9.3		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32 FO = 384	6.9 7.9		8.1 9.3		ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 384		0.6 3.1		0.6 3.1	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 384	0.0 0.0		0.0 0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 384	8.6 13.8		8.6 13.8		ns
t_P	Minimum Period	FO = 32 FO = 384	13.7 16.0		16.2 18.9		ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 384		73 63		62 53	MHz

Note:

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

RP1280A, A1280A Timing Characteristics (continued)

(Worst-Case Military Conditions)

Output Module Timing		‘–1 Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]						
t_{DLH}	Data-to-Pad HIGH		11.0		13.0	ns
t_{DHL}	Data-to-Pad LOW		13.9		16.4	ns
t_{ENZH}	Enable-to-Pad Z to HIGH		12.3		14.4	ns
t_{ENZL}	Enable-to-Pad Z to LOW		16.1		19.0	ns
t_{ENHZ}	Enable-to-Pad HIGH to Z		9.8		11.5	ns
t_{ENLZ}	Enable-to-Pad LOW to Z		11.5		13.6	ns
t_{GLH}	G-to-Pad HIGH		12.4		14.6	ns
t_{GHL}	G-to-Pad LOW		15.5		18.2	ns
d_{TLH}	Delta LOW to HIGH		0.09		0.11	ns/pF
d_{THL}	Delta HIGH to LOW		0.17		0.20	ns/pF
CMOS Output Module Timing[1]						
t_{DLH}	Data-to-Pad HIGH		14.0		16.5	ns
t_{DHL}	Data-to-Pad LOW		11.7		13.7	ns
t_{ENZH}	Enable-to-Pad Z to HIGH		12.3		14.4	ns
t_{ENZL}	Enable-to-Pad Z to LOW		16.1		19.0	ns
t_{ENHZ}	Enable-to-Pad HIGH to Z		9.8		11.5	ns
t_{ENLZ}	Enable-to-Pad LOW to Z		11.5		13.6	ns
t_{GLH}	G-to-Pad HIGH		12.4		14.6	ns
t_{GHL}	G-to-Pad LOW		15.5		18.2	ns
d_{TLH}	Delta LOW to HIGH		0.17		0.20	ns/pF
d_{THL}	Delta HIGH to LOW		0.12		0.15	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *SSO information can be found in the “Simultaneously Switching Output Limits for Actel FPGAs” application note.*

RP14100A, A14100A Timing Characteristics

(Worst-Case Military Conditions)

Logic Module Propagation Delays[1]		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		3.0		3.5	ns
t_{CO}	Sequential Clock-to-Q		3.0		3.5	ns
t_{CLR}	Asynchronous Clear-to-Q		3.0		3.5	ns
Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{RD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{RD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{RD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{RD8}	FO=8 Routing Delay		4.2		4.9	ns
Logic Module Sequential Timing						
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	1.0		1.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.6		0.6		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	1.0		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.6		0.6		ns
t_{WASYN}	Asynchronous Pulse Width	4.8		5.6		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	4.8		5.6		ns
t_{A}	Flip-Flop Clock Input Period	9.9		11.6		ns
f_{MAX}	Flip-Flop Clock Frequency		100		85	MHz

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

RP14100A, A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions)

I/O Module Input Propagation Delays		‘–1 Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad-to-Y		4.2		4.9	ns
t_{ICKY}	Input Reg IOCLK Pad-to-Y		7.0		8.2	ns
t_{OCKY}	Output Reg IOCLK Pad-to-Y		7.0		8.2	ns
t_{ICLRY}	Input Asynchronous Clear-to-Y		7.0		8.2	ns
t_{OCLRY}	Output Asynchronous Clear-to-Y		7.0		8.2	ns
Predicted Input Routing Delays[1]						
t_{IRD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{IRD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{IRD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{IRD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{IRD8}	FO=8 Routing Delay		4.2		4.9	ns
I/O Module Sequential Timing						
t_{INH}	Input Flip-Flop Data Hold	0.0		0.0		ns
t_{INSU}	Input Flip-Flop Data Set-Up	2.1		2.4		ns
t_{IDEH}	Input Data Enable Hold	0.0		0.0		ns
t_{IDESU}	Input Data Enable Set-Up	8.7		10.0		ns
t_{OUTH}	Output Flip-Flop Data Hold	1.2		1.2		ns
t_{OUTSU}	Output Flip-Flop Data Set-Up	1.2		1.2		ns
t_{ODEH}	Output Data Enable Hold	0.6		0.6		ns
t_{ODESU}	Output Data Enable Set-Up	2.4		2.4		ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

RP14100A, A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions)

I/O Module – TTL Output Timing[1]		‘–1 Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data-to-Pad, High Slew		7.5		8.9	ns
t_{DLS}	Data-to-Pad, Low Slew		11.9		14.0	ns
t_{ENZHS}	Enable-to-Pad, Z to H/L, High Slew		6.0		7.0	ns
t_{ENZLS}	Enable-to-Pad, Z to H/L, Low Slew		10.9		12.8	ns
t_{ENHSZ}	Enable-to-Pad, H/L to Z, High Slew		11.9		14.0	ns
t_{ENLSZ}	Enable-to-Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad-to-Pad H/L, High Slew		12.2		14.0	ns
t_{CKLS}	IOCLK Pad-to-Pad H/L, Low Slew		17.8		17.8	ns
d_{TLHHS}	Delta LOW to HIGH, High Slew		0.04		0.04	ns/pF
d_{TLHLS}	Delta LOW to HIGH, Low Slew		0.07		0.08	ns/pF
d_{THLHS}	Delta HIGH to LOW, High Slew		0.05		0.06	ns/pF
d_{THLLS}	Delta HIGH to LOW, Low Slew		0.07		0.08	ns/pF
I/O Module – CMOS Output Timing[1]						
t_{DHS}	Data-to-Pad, High Slew		9.2		10.8	ns
t_{DLS}	Data-to-Pad, Low Slew		17.3		20.3	ns
t_{ENZHS}	Enable-to-Pad, Z to H/L, High Slew		7.7		9.1	ns
t_{ENZLS}	Enable-to-Pad, Z to H/L, Low Slew		13.1		15.5	ns
t_{ENHSZ}	Enable-to-Pad, H/L to Z, High Slew		11.6		14.0	ns
t_{ENLSZ}	Enable-to-Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad-to-Pad H/L, High Slew		14.4		16.0	ns
t_{CKLS}	IOCLK Pad-to-Pad H/L, Low Slew		20.2		22.4	ns
d_{TLHHS}	Delta LOW to HIGH, High Slew		0.06		0.07	ns/pF
d_{TLHLS}	Delta LOW to HIGH, Low Slew		0.11		0.13	ns/pF
d_{THLHS}	Delta HIGH to LOW, High Slew		0.04		0.05	ns/pF
d_{THLLS}	Delta HIGH to LOW, Low Slew		0.05		0.06	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the “Simultaneously Switching Output Limits for Actel FPGAs” application note.*

RP14100A, A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions)

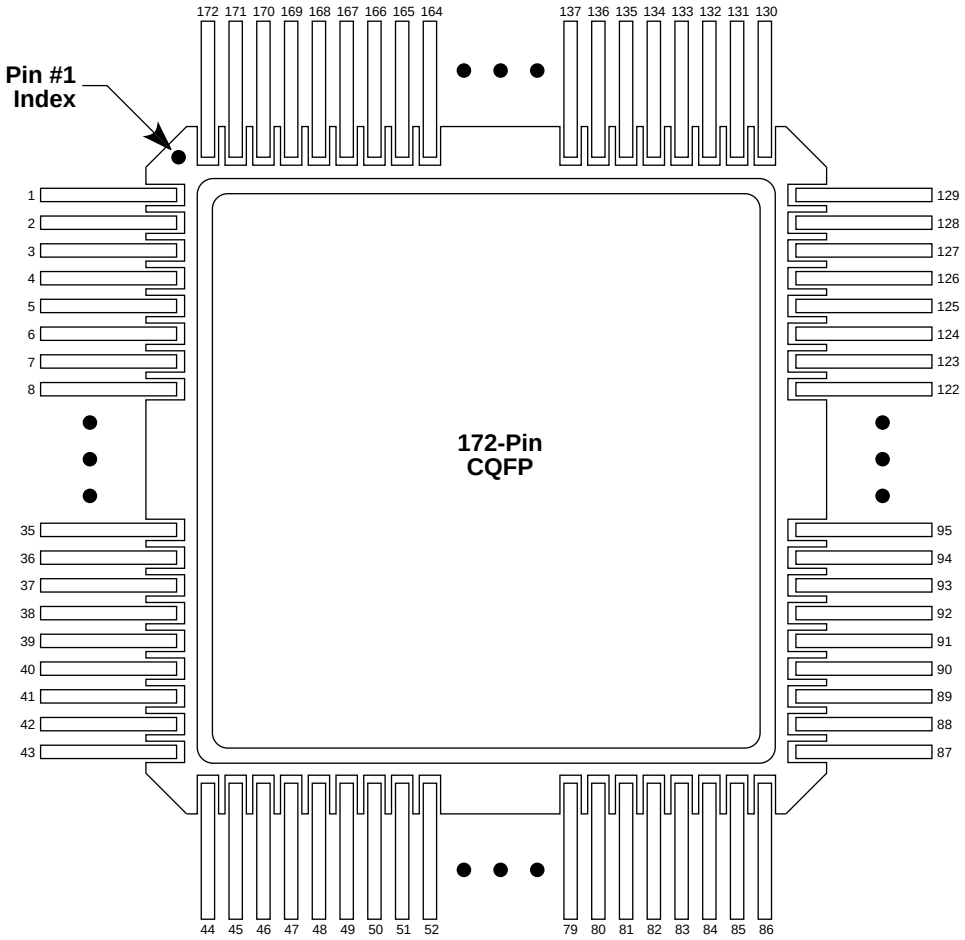
Dedicated (Hard-Wired) I/O Clock Network		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input LOW to HIGH (Pad to I/O Module Input)		3.5		4.1	ns
t_{IOPWH}	Minimum Pulse Width HIGH	4.8		5.7		ns
t_{IOPWL}	Minimum Pulse Width LOW	4.8		5.7		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.9		4.4		ns
t_{IOCKSW}	Maximum Skew		0.9		1.0	ns
t_{IOP}	Minimum Period	9.9		11.6		ns
f_{IOMAX}	Maximum Frequency		100		85	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to S-Module Input)		5.5		6.4	ns
t_{HCKL}	Input HIGH to LOW (Pad to S-Module Input)		5.5		6.4	ns
t_{HPWH}	Minimum Pulse Width HIGH	4.8		5.7		ns
t_{HPWL}	Minimum Pulse Width LOW	4.8		5.7		ns
t_{HCKSW}	Maximum Skew		0.9		1.0	ns
t_{HP}	Minimum Period	9.9		11.6		ns
f_{HMAX}	Maximum Frequency		100		85	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (FO=256)		9.0		10.5	ns
t_{RCKL}	Input HIGH to LOW (FO=256)		9.0		10.5	ns
t_{RPWH}	Min. Pulse Width HIGH (FO=256)	6.3		7.1		ns
t_{RPWL}	Min. Pulse Width LOW (FO=256)	6.3		7.1		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.9		2.1	ns
t_{RP}	Minimum Period (FO=256)	12.9		14.5		ns
f_{RMAX}	Maximum Frequency (FO=256)		75		65	MHz
Clock-to-Clock Skews						
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	3.5	0.0	3.5	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew	0.0	5.0	0.0	5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 50% max.)	 0.0 0.0	 1.0 3.0	 0.0 0.0	 1.0 3.0	ns

Note:

1. Delays based on 35 pF loading.

Package Pin Assignments

172-Pin CQFP (Top View)



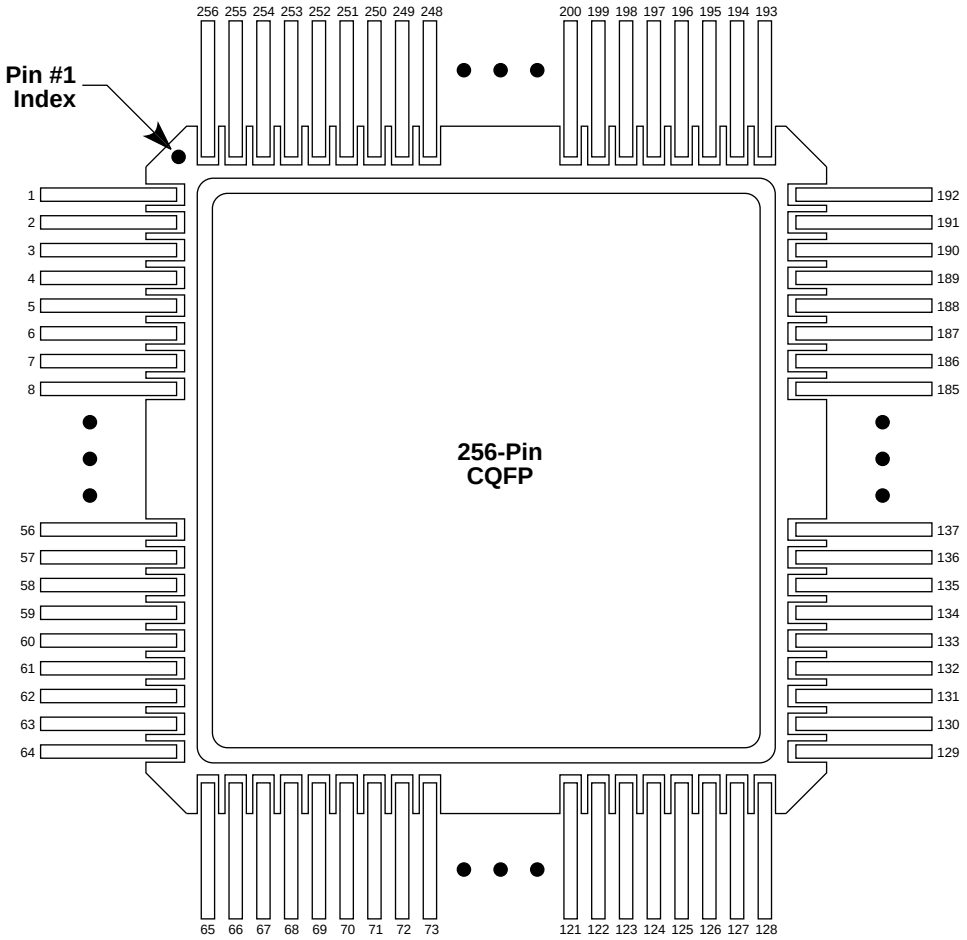
Function	RP1280A, A1280A Pin Number
CLKA or I/O	150
CLKB or I/O	154
DCLK or I/O	171
GND	7, 17, 22, 32, 37, 55, 65, 75, 98, 103, 106, 108, 118, 123, 141, 152, 161
MODE	1
PRA or I/O	148
PRB or I/O	156
SDI or I/O	131
V_{CC}	12, 23, 24, 27, 66, 80, 107, 109, 110, 113, 136, 151, 166

Notes:

1. *Unused I/O pins are designated as outputs by Designer and are driven LOW.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

Package Pin Assignments (continued)

256-Pin CQFP (Top View)



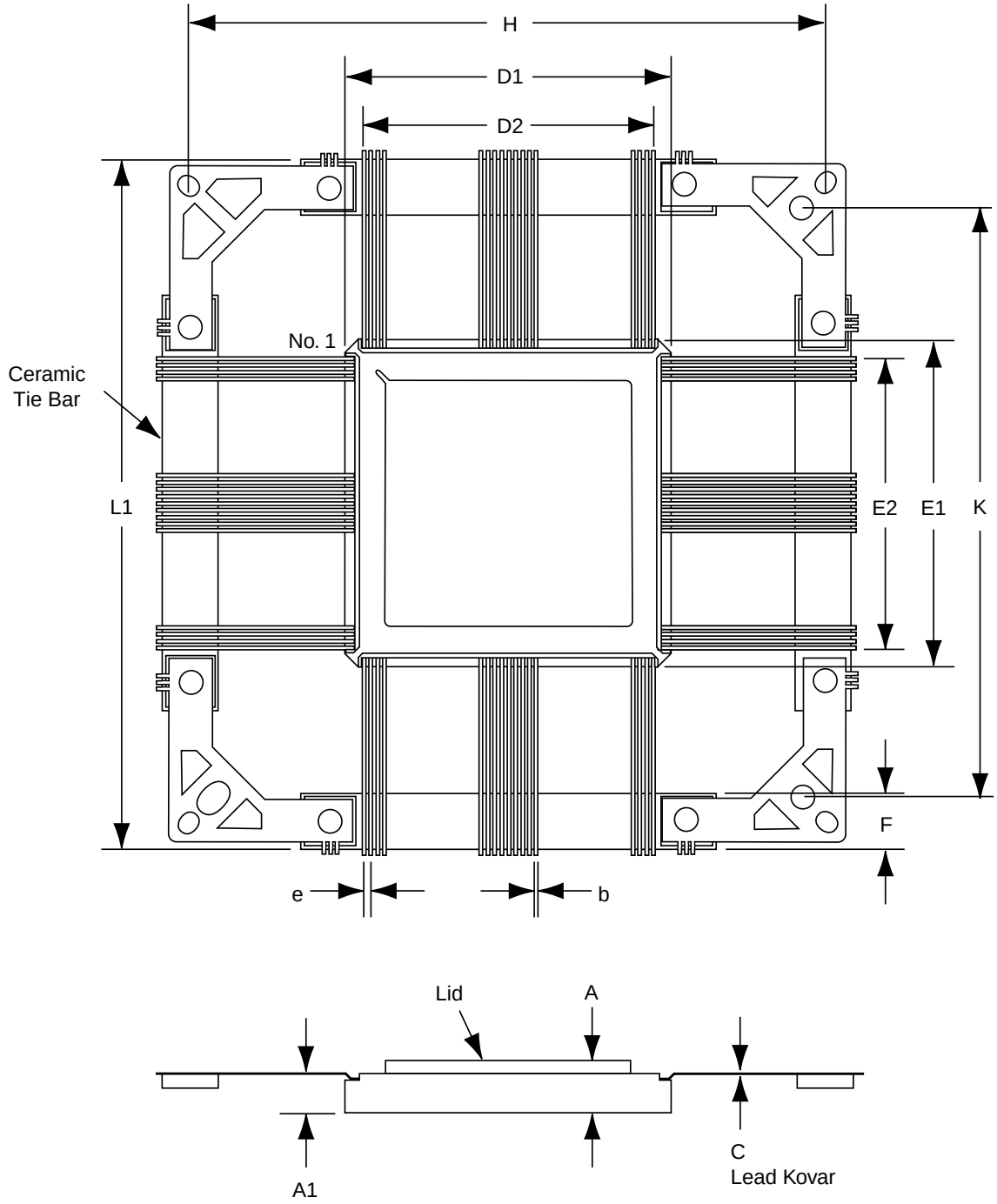
Function	RP14100A, A14100A Pin Number
CLKA or I/O	219
CLKB or I/O	220
DCLK or I/O	256
GND	1, 29, 31, 59, 91, 93, 110, 128, 158, 160, 175, 176, 189, 222, 224, 240
HCLK or I/O	96
IOCLK or I/O	188
IOPCL or I/O	127
MODE	11
PRA or I/O	225
PRB or I/O	90
SDI or I/O	2
V_{CC}	28, 30, 46, 92, 94, 141, 159, 161, 174, 221, 223

Notes:

1. *Unused I/O pins are designated as outputs by Designer and are driven LOW.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

Package Mechanical Drawings

Ceramic Quad Flatpack (CQFP—Cavity Up)

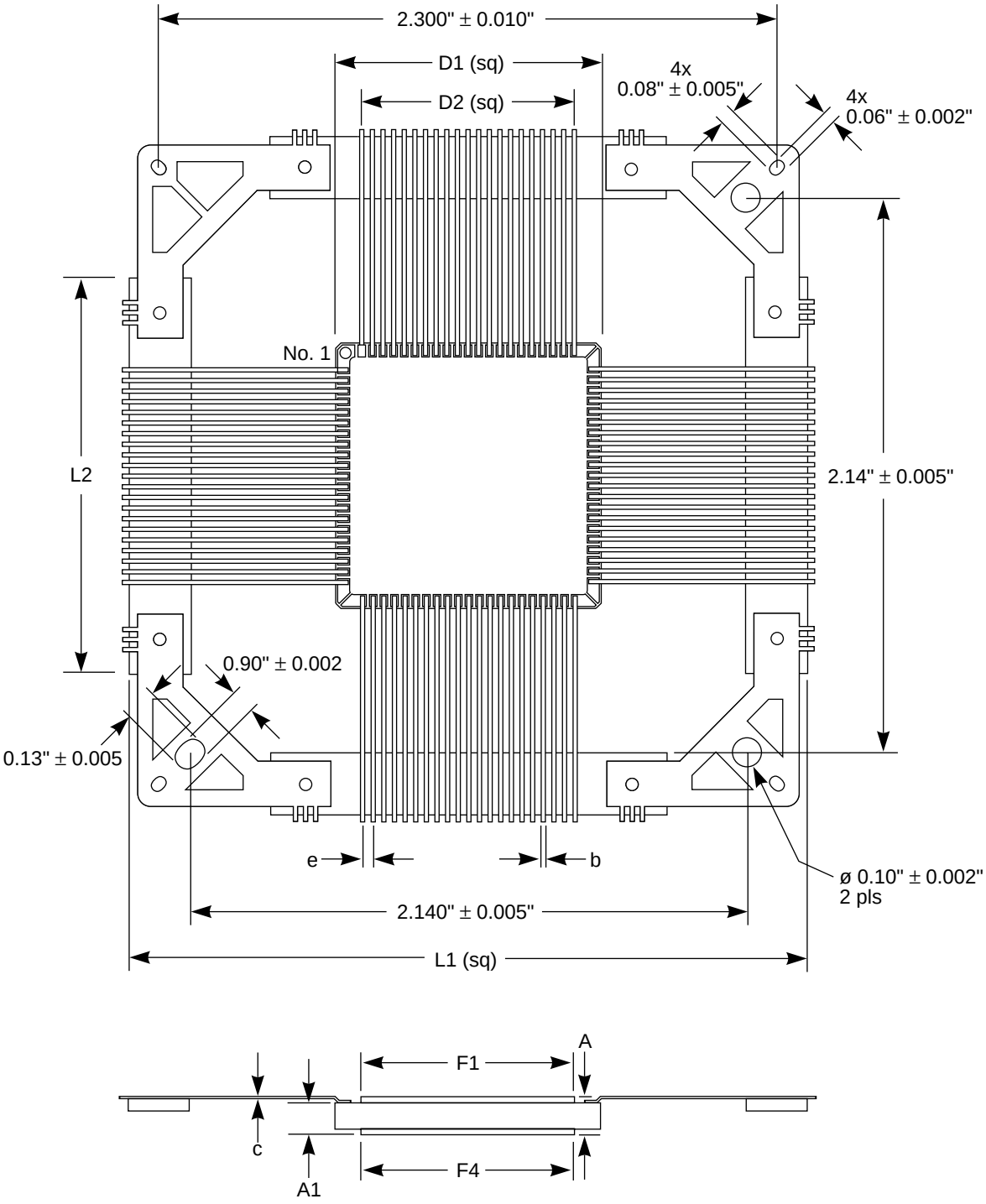


Notes:

1. *All dimensions are in inches except CQ208 and CQ256 which are in millimeters.*
2. *Outside leadframe holes (from dimension H) are circular for the CQ208 and CQ256.*
3. *Seal ring and lid are connected to Ground.*
4. *Lead material is Kovar with minimum 60 miconiches gold over nickel.*
5. *Packages are shipped unformed with the ceramic tie bar.*
6. *32200DX – CQ208 has heat sink on the backside.*

Package Mechanical Drawings (continued)

RAD-PAK® Ceramic Quad Flatpack (172-Pin CQFP RAD-PAK®)



Notes:

1. *All dimensions are in inches.*
2. *Seal ring and lid are connected to Ground.*
3. *Lead material is Kovar with gold over nickel.*
4. *Packages are shipped unformed with the ceramic tie bar.*

Ceramic Quad Flatpack (CQFP)

	CQ256		
Symbol	**Min**	**Nom.**	**Max**
A	2.28	2.67	3.06
A1	1.93	2.29	2.65
b	0.18	0.20	0.22
c	0.11	0.15	0.18
D1/E1	35.64	36.00	36.36
D2/E2	31.5 BSC		
e	0.50 BSC		
F	7.05	7.75	8.45
H	70.00 BSC		
K	65.90 BSC		
L1	74.60	75.00	75.40

Note:

1. *All dimensions are in inches.*
2. *BSC equals Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*

RAD-PAK® Ceramic Quad Flatpack (RAD-PAK® CQFP)

	RAD-PAK® CQ172		
Symbol	**Min**	**Nom.**	**Max**
A	0.116	0.133	0.146
b	0.007	0.008	0.130
c	0.004	0.006	0.009
D11	1.137	1.150	1.162
D2	1.050 BSC		
e	0.025 BSC		
F1	0.890	0.895	0.900
F4	0.881	0.890	0.899
L1	2.485	2.500	2.5095
L2	1.690	1.700	1.710
A1	0.079	0.091	0.103

Note:

1. *All dimensions are in inches.*
2. *BSC equals Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*

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