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Advanced VHDL:

VHDL for Design and Modeling Applications

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1994

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PART 1

Outline

- **Program**
- **Copyright**
- **Material**
- **Schedule**
- **Conclusions**

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Outline.program

Beginning VHDL: An Introduction to Language Concepts

Advanced VHDL: VHDL for Design and Modeling Applications

Advanced Design: CPU Design and Synthesis with VHDL

- **Preparation:** Participants are to be prepared for this unit by reading the Introductory Tutorial that is included in this training package.

- **Program:** This unit is the second unit in a series of three units. The unit is to be taught in 14 hours.

- **Prerequisites:** A general knowledge of VHDL is required as a prerequisite of this unit. Also, knowledge of digital systems and logic design is necessary**.**

- **Objectives:** Participants in this training will learn to design and model in VHDL. Details of language for advanced modeling requirements will be discussed. All language constructs will be covered.

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- This material is to be used in conjunction with the book titled: "VHDL: Analysis and Modeling of Digital Systems", McGraw-Hill 1993, by Zainalabedin Navabi. ISBN: 0-07-046472-3

- The right to copy and distribute this material in a training course is restricted and it is reserved for Zainalabedin Navabi.

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Outline.material

Course material contains:

- "VHDL: Analysis and Modeling of Digital Systems"
- Introductory tutorial
- A set of 300 transparency copies
- A set of 6 quizzes

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Outline.schedule

Part 1: Outline
30 minutes

Part 2: Review
1 hour

Part 3: VHDL Timing
1½ hour

Part 4: Structural
1½ hour

Part 5: Design Organization
1¾ hour

Part 6: Utilities
1½ hour

Part 7: Dataflow
1¾ hour

Part 8: Behavioral_Descriptions
1¾ hour

Part 9: Standards
1 hour

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Outline.conclusions

1. Outline: Introduction, Organization, Outline

2. Review: Behavioral description, Using process statements, Top-down design, Using available components, Wiring predefined components, Wiring from bottom to top, Generation of testbench data, Using procedures

3. VHDL_Timing: Modeling requirements, Objects & classes, Signals & variables, Concurrent & sequential assignments, Events, transactions & delta delays, Delay modeling, Sequential placement of transactions, Conventions

4. Structural_Description_of_Hardware: Wiring parts into larger designs, Start with primitives, Wire gates into general purpose components, Use iterative constructs, Generate testbenches, Show binding alternatives, Use gate-based components for a larger design

5. Design_Organization: Subprograms, Packaging, Parameter specification, Parametrization, Top level configuration, Design libraries, A complete example

6. Utilities_for_high_level_descriptions: Language aspects, Types, Over loading subprograms operators, Predefined Attributes, User defined attributes

7. Dataflow: Constructs for dataflow descriptions, Multiplexing and clocking, Multiple assignments, State machines, Open collector gates, A complete dataflow example, Load dependent timing

8. Behavioral_Descriptions: Constructs for sequential descriptions, Assertion for behavioral checks, Handshaking constructs, Timing control, Formatted I/O, MSI parts, A complete MSI based design

9. STANDARDS: MVL9: logic value system, Logic type, Operators, Conversions; VHDL'93: Operators, Delay model, Instantiation, Binding, Attributes, Signal assignments, Report, Postponed process

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