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Advanced Design:

CPU Design and Synthesis with VHDL

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PART 1

Outline

- **Program**
- **Copyright**
- **Material**
- **Schedule**
- **Conclusions**

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Outline.program

Beginning VHDL: An Introduction to Language Concepts

Advanced VHDL: VHDL for Design and Modeling Applications

Advanced Design: CPU Design and Synthesis with VHDL

- **Preparation:** Participants are to be prepared for this unit by reading the Advanced Tutorial that is included in this training package.

- **Program:** This unit is the third unit in a series of three units. The unit is to be taught in 14 hours.

- **Prerequisites:** Knowledge of VHDL is required as a prerequisite of this unit. General knowledge of computing structures with data and control units, and computer architectures are also necessary.

- **Objectives:** Participants in this training will learn to use VHDL in design and implementation of high level complex structures. Using VHDL for an initial high level design specification, manual design, and synthesizing a CPU will be discussed.

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- This material is to be used in conjunction with the book titled: "VHDL: Analysis and Modeling of Digital Systems", McGraw-Hill 1993, by Zainalabedin Navabi. ISBN: 0-07-046472-3

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Outline.material

Course material contains:

- "VHDL: Analysis and Modeling of Digital Systems"
- Advanced Tutorial
- A set of 250 transparency copies
- A set of 6 quizzes

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Outline.schedule

Part 1: Outline
30 minutes

Part 2: Review
1 hour

Part 3: MSI Based Design
1½ hour

Part 4: General CPU Description
1½ hour

Part 5: Manual Data_Path Design
1½ hour

Part 6: Manual Controller Design
1¾ hour

Part 7: Overview of Synthesis
1½ hour

Part 8: Behavioral Synthesis
1¾ hour

Part 9: Dataflow Synthesis
1¾ hour

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Outline. conclusions

1. Outline: Introduction, Organization, Outline

2. Review: Levels of abstraction, Entity and Architecture, Signal assignments, Guarded signal assignments, Three state bussing, Process statements, Combinational processes, Sequential processes, Multiplexing, Package

3. MSI Based Design: Use MSI parts of Part 2, Sequential multiplication, Designing the multiplier, Control and data parts, Testing the multiplier

4. General CPU Description: Will present a high level VHDL description of a small CPU. The CPU, Memory organization, Instructions, Addressing, Utilities for VHDL description, Interface, Behavioral description, Coding individual instructions

5. Manual Data_path Design: Will present VHDL description for manual design of data_path. Data components, Bussing structure, Description of logic, Description of registers, Bus resolutions, Component wiring

6. Manual Controller Design: Will present VHDL description for manual design of controller. Controller hardware, VHDL style, Signals and resolutions, State descriptions, Complete CPU, Testing CPU

7. Synthesis: Main concepts, Structural synthesis, Combinational circuits, Functional registers, State machines

8. Behavioral_Synthesis: Will present a high level synthesizable CPU description. Synthesis style, Necessary Package, Interface, General Layout, Registers, Clocking, Sequencing, Simulation and Synthesis

9. Dataflow_Synthesis: Will partition the CPU and synthesize each part separately. Synthesis style, Controller, Data components, Data path, Synthesized example, Conclusions

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