For:reese
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Test #2 – EE 4743 – Fall 1998 My Name is: ______________________________

You have 50 minutes to complete this test. Good luck!

1. (15) Answer the following short questions.
   a. You are a middle–level manager. One of your employees has fully pipelined a flowgraph (down to 1 clock cycle per sample period). He tells you that it will take him three days to design the control unit for the flowgraph. What is wrong with that?

   b. Fill in the blanks:

Pipelining increases ______________________________________ but makes

_______________________________________ worse.

   c. Name two techniques that may let you reduce the critical path without increasing latency.

2. (30 points) Consider the equation below.

$$Y = 0.5\ Y@1 + 0.75\ X - X@1$$

a. Convert the equation to "shift–and–add" format.

b. Draw a flowgraph for it. Assume shifts are combinational. Don't worry about minimizing anything!

c. What is the critical path? __________ The iteration loop critical path? __________

d. Assume that the number of clock cycles per sample period equals the critical path. Estimate the amount of resources needed based on the total number of shifts and adds that are performed and the number of clock cycles.

Number of Adders: __________ Number of Shifters: __________

e. Assign TASAP and TALAP pairs to the flowgraph. (Hint: You may want to redraw the graph below.)

f. Schedule the flowgraph. Do not worry about amount of resources (for example, number of registers).

3. (35 points) Consider the schedule below.

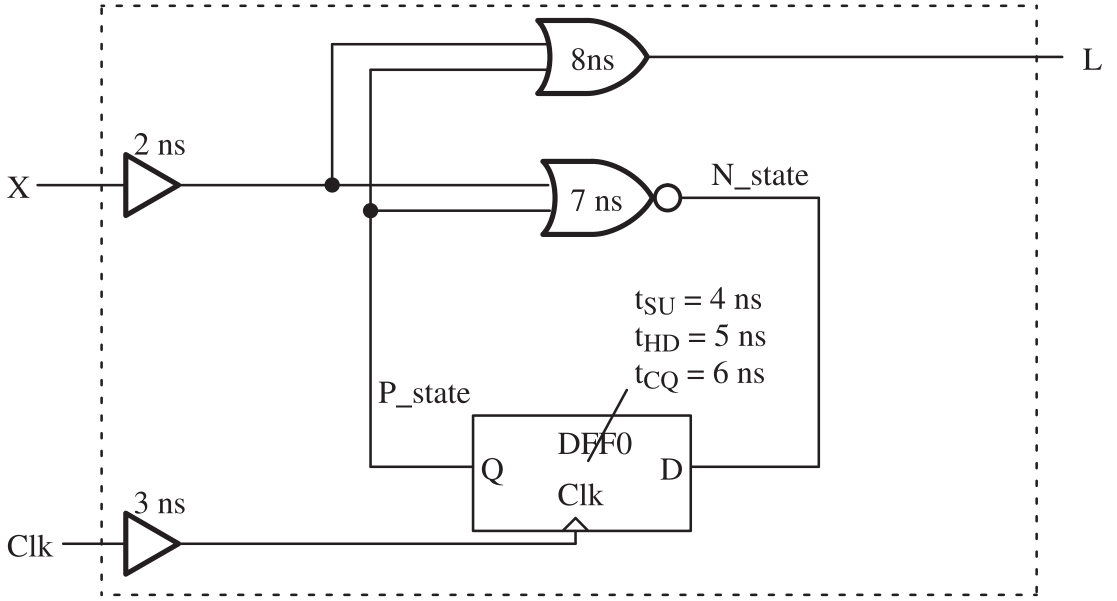
CC	Adder	Shifter	A	B	C	D	E
0		A >> 2	Ld Shifter	/////	/////	Load X	
1		D >> 1		/////	/////	/////	Ld. Shifter
2	A + E	C >> 3	Ld. Shifter	/////	Ld. Adder	/////	
3	A + C			/////	Ld. Adder	/////	
3	B + C; output is Y		Ld. Adder	Load D	Load B		

a. Use the schedule to reconstruct the original flowgraph.

b. Use the flowgraph to reconstruct the original equation.

c. Redraw the flowgraph to minimize the iteration loop critical path. For full credit, your flowgraph should have the minimum critical path that is acheivable once the iteration loop critical path has been minimized. ONLY REDRAW the flowgraph; don't pipeline it!

4. (20 points) Consider the diagrams and answer the questions below. Note that the flip flop is drawn ‘‘backwards’’.



a. (10) What are the external setup and hold times for input X? Hint:
DIN t_{SU} = DFF t_{SU} + DIN t_{PD} max – Clk t_{PD} min
DIN t_{HD} = DFF t_{HD} – DIN t_{PD} min + Clk t_{PD} max

X to DFF0: Setup Time: ____________ Hold Time: ____________

b. (10) What is the delay from the clock to output L?

Delay from Clk to L: ____________

c. (10) What is the clock cycle time based on register–to–register delays?

Register–to–Register Clock Cycle Time: ____________