A SINGLE-CHIP CCSDS PACKET TELEMETRY AND TELECOMMAND BASED MICROCAMERA

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Abstract

By applying the packet telemetry and telecommand standards endorsed by the European Space Agency (ESA) and the Consultative Committee for Space Data Systems (CCSDS) to a microcamera, the need for support from the on-board data handling system can almost be eliminated. If the microcamera is designed with interfaces that fully match those of the telemetry and the telecommand subsystem, the additional interface components will be reduced to simple transceivers. A development of such a microcamera was initiated by ESA in order to meet emerging requirements on monitoring of deployments of spacecraft appendices such as antennas and solar arrays. The first silicon has been produced and is now being considered for several missions.

1 INTRODUCTION

The objective of an on-going development is to produce a single-chip microcamera suitable for visual telemetry, image gathering on planetary probes, rovers etc., where size and power consumption has to be minimised. To accomplish this, a step away from traditional space technology had to been made.

Cameras for space applications have traditionally been based on Charge Coupled Device (CCD) technology, but this technology is now getting competition from CMOS Active Pixel Sensor (APS) technology. The APS technology offers certain benefits that are directly relevant for potential applications in space. It offers the possibility for integration of system and sensor on a single chip, with resulting gains in system dimensions, mass, and power consumption. Future generations of CMOS sensors hold the promise of radiation-tolerance, which makes them all the more interesting for these niche applications.

The most basic application for APS sensors, visual monitoring, has already been demonstrated in space. On October 30th, 1997, the Visual Telemetry System (Ref. 8), jointly produced by MMS (UK), Delft Sensor Systems - OIP (B), and IMEC (B) acquired and transmitted near-life images from the separation between the TeamSat satellite and the Speltra on an Ariane 5 flight (see figure 1). The VTS cameras were based on an already existing IMEC CMOS APS sensor, the Fuga15 (Ref. 7). Since the Fuga15 was not designed with space applications in mind, the VTS required a separate unit to interface the cameras to the onboard data handling system of the spacecraft and to perform image compression. The goal for current and planned developments is to remove the need for such a separate unit and to produce a stand alone microcamera that can be directly interfaced to the telemetry and the telecommand subsystem.

Figure 1: *Speltra separation on Ariane 5 flight A-502; an image taken with a CMOS APS camera (Ref. 9).*

2 INTEGRATED RADIATION-TOLERANT IMAGING SYSTEM (IRIS)

A CMOS APS chip targeted towards space applications, the *Integrated Radiation-tolerant Imaging System* (IRIS), is being developed in two steps. Firstly, a new imaging sensor part has been developed, based on an integrating APS previously developed by IMEC, the IBIS-1 (Ref. 5) (Ref. 6). The new sensor (named IRIS-1) has been tailored to meet specific requirements posed by the Agency, such as an increased resolution of 640 by 480 pixels, on-chip analog-to-digital conversion and the possibility for fast sub-windowing. In the second step, the sensor is integrated with all timing and control logic required to operate the sensor itself, and support for multiple variants of serial and parallel interfaces and protocols. Although the microcamera can be used in a multitude of applications, special attentions has been give to the aspect of interfacing it with modern spacecraft telemetry and telecommand systems. The resulting microcamera (named IRIS-2) will be a system-on-a-chip capable of taking images and directly communicating with the spacecraft.

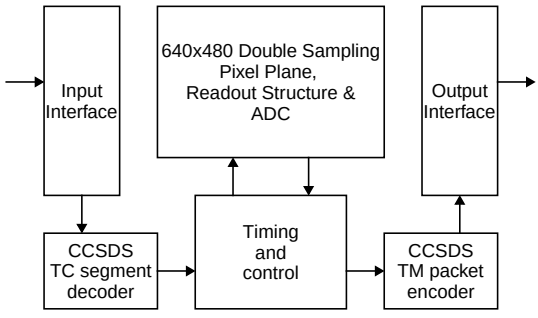

Figure 2: *Block diagram of the IRIS series of imagers.*

The IRIS chip is being developed by IMEC (B) and is manufactured in the commercial mixed-signal 0.7 µm CMOS process from Alcatel Mietec (B). System level reliability is enhanced by internal watchdogs, parity checks on most registers and finite state machines, and by voting mechanisms for the most important long-term settings. In addition, some user commands trigger an internal synchronous circuit reset, so that the IRIS control logic periodically returns to a known and valid state.

The only electrical parts required to turn IRIS into a microcamera are line drivers and receivers, passive components, and a single 5 V supply voltage.

3 SENSOR SPECIFICS

The optical sensor part of IRIS is a 640x480 pixels integrating CMOS APS. This image sensor is complemented with a voltage amplifier, featuring user-selectable gain, and with a local 8 bits flash Analogue-to-Digital Converter (ADC). The 3-transistor active pixel contains an integrating photodiode. During a fixed (but user controlled) integration time, photo-electric charge is accumulated on the junction capacitance of the diode. At readout, which is simultaneous for all pixels on a row, the row select transistor is closed and the local source follower puts the diode voltage on the column bus. With a separate reset operation, once more simultaneous for all pixels on a given row, the diode's charge is drained to a fixed potential. After this the reset diode's voltage is also output to the column bus.

Connected to each column bus is a column amplifier which performs a form of correlated double sampling on the pixel's post-integration and post-reset output signals. The correlated double sampling removes static offsets present in the pixel signal chain, as well as those present in the column amplifiers themselves. After this operation, the output of every column amplifier is sequentially selected and passed-on to the sensor's pixel-serial output port, where it receives suitable amplification and analogue-to-digital conversion. In addition to the digital output, an analogue output signal is also present and can be used in applications where higher resolution external analogue-to-digital conversion is required.

Resolution	640 by 480
Pixel pitch	14 µm
Effective fill factor	60%
Signal to noise ratio (SNR)	65 dB
Readout noise	56 e^-
Sensitivity at 100 ms exposure time for SNR = 20 dB	70 $\mu W/m^2$
Pixel response non-uniformity	8%
Dark current at 22 ˚C	4000 e^-/s
Bad pixels (typical)	none
Frame rate (full images)	10 Hz
RGB colour	optional

Table 1: *Key performance parameters for IRIS-1.*

During operation the line to be read, the line to be reset, and the pixel to be forwarded to the output, is selected by a one-hot shift register that serves as a line/pixel pointer. In the preceding version of this imager architecture, these shift registers can only be reset to the initial state or advanced one position under external control. However, in order to allow a more versatile access to the focal plane, the IRIS sensor adds to this a pre-load option, where each pointer register can be loaded with a random 10-bits address, prior to its use. This allows for windowed readout or subsampling at a low operational overhead.

Figure 3 is an unprocessed sample picture made with the IRIS-1 chip. A high image quality is obvious, yet also present is a certain amount of optical crosstalk at highly illuminated areas in the scene, a bit like local blooming. This can partly be attributed to the high infrared sensitivity of the pixel, as well as to the use of thick epi wafers during manufacturing. In future versions thinner epi will be used, which is expected to alleviate this problem somewhat.

The IRIS chips will exist in greyscale as well as in RGB colour versions, the latter is implemented by colouring individual pixels directly on the die, requiring off-line colour reconstruction.

Figure 3: *Sample image taken with an IRIS-1 chip.*

4 MICROCAMERA OPERATION

Versatile access to the IRIS pixel matrix allows readout of windows-of-interest, digital domain subsampling, and one-dimensional digital pixel binning (or averaging). With these provisions, temporal resolution can be traded for spatial resolution given a maximum pixel rate. For instance, normal 640x480 images can be acquired at 10 frames per second. By using subsampling where each second pixel is skipped (in both dimensions), the frame rate is increased to 40 frames per second, while the complete scene is still visible. The end user only is confronted with the high-level command interface to the imager: specific control of the actual focal plane array is performed on-chip.

Typical use of the IRIS involves a series of commands and arguments (each 8 bit words) to set the internal chip parameters to desired values, followed by an acquisition command. Commands are available to write all image parameters

(coordinates, exposure time etc.), set readout modes and perform image acquisitions. From 1 up to 127 images can be requested at once, while there is also an option to set the camera into continuous acquisition mode.

The delayed (or timeline) execution of one acquisition command is also included. This in-flight programmable timeline covers several hours, with a resolution of approximately one second. The timeline is used to trigger a camera action in situations where direct and instantaneous control is not feasible, e.g. because of unavailable communication between spacecraft and ground station.

5 TELECOMMAND AND TELEMETRY

The IRIS camera chip communicates to the outside world over a number of user-selectable interfaces. These interfaces have been designed to link directly to existing space and commercial components and protocols:

- serial and parallel command input, up to 3.125 Mbits/s;
- serial data output, up to 25 Mbits/s;
- synchronous parallel data output, up to 3.125 MBytes/s;
- analogue image output (with sync pulses).

The IRIS microcamera will accept CCSDS telecommand packets as commanding input (Ref. 3). The integrity of the packet will be protected by means of a cyclic redundancy code in the same ways as specified for command pulse distribution in the ESA telecommand decoder specification. Telecommands with detected errors are not executed. The user can at all times enquire about the error status of the most recently received command packet.

Eight digital output signals will be accessible via telecommand packets, with which flash lights, colour filter wheels, pan and tilt motors etc. can be operated. The input interface will allow direct connection to the Multiple Access Point (MAP) of the Packet Telecommand Decoder (PTCD), supporting the bit serial synchronous protocol also being compatible with data serial and memory load commands in the TTC-B-01 standard. It will also feature parallel and bit serial asynchronous interfaces.

The microcamera will packetise output data as CCSDS telemetry packets (Ref. 1), automatically selecting whether the full image frame should be contained in a single packet or whether each image line should be transmitted as a separate packet. The former approach is only suitable when sending a sub-sample or a sub-window of the full image array since the standard limits the number of octets per packet to 65536. In the latter case the image frame synchronisation is maintained using packet grouping. This allows the user to extract frame or line information directly from the telemetry transmission layer protocol, which drastically reduces the down-link overhead.

To increase the usefulness of IRIS, especially when used as a distributed sensing unit on spacecraft, up to three analogue inputs are available for local health monitoring purposes or similar. The analogue inputs will be observable in the housekeeping packets that can be transmitted on the same interface as the image data.

The output interface will allow direct connection to the Virtual Channel Assembler (VCA) that forms the front-end of the telemetry encoder. The microcamera will also allow direct connection to an IEEE-1355 high speed link interface component and to the Packetising Rice Data Compressor that will implement the CCSDS lossless data compression standard.

6 APPLICATION SCENARIOS

The IRIS sensor is suitable for low-to-medium-quality general purpose imaging tasks, such as:

- monitoring and visual telemetry;
- low-grade earth and planetary imaging;
- low-end image gathering on small platforms such as planetary probes lander and rover near imaging;
- robotics (high frame rates and windows);
- spacecraft optical guidance and navigation (low noise, high sensitivity, high readout rates). Until APS fully matures in the fields of noise, non-uniformity and dark signal level, and until it grows competitive with high-end high-cost CCDs, we have to exclude high-quality scientific imaging from the potential applications.

Among the multitude of potential commercial applications only a few are mentioned here: multimedia consumer electronics, surveillance, industrial vision, robotics etc.

Figure 4 illustrates how the IRIS microcamera can be interfaced with telemetry and the telecommand components. The input interface receives TC segments from the telecommand decoder MAP interface. The communication is performed using three signals; clock, data and strobe. As electrical line drivers, RS422 interface components can be used. Images and housekeeping data are packetised by the microcamera and transferred to the Virtual Channel Assembler (VCA) via a serial or parallel interface. Also for this part of the communication, RS422 interface components can be used. This scenario has a limitation, the buffer memory of the VCA can only hold a portion of the image data and subsampling or sub-windowing has to be used. The problem can be alleviated to a certain degree by letting TM packets be compressed by the PRDC component, located between the microcamera and the VCA. The PTCD, VCA and the Virtual Channel Multiplexer (VCM) are all available from MITEL Semiconductors (S).

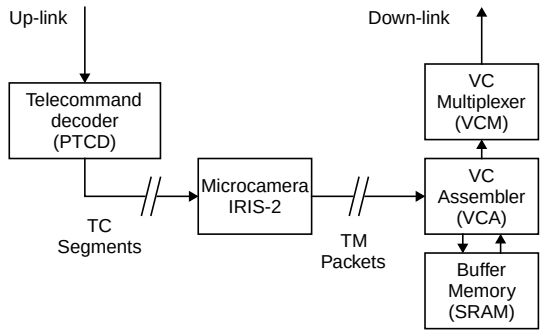

Figure 4: *Interfacing of the microcamera with packet telecommand decoder and telemetry encoder.*

To enable large images, the image frame needs to be buffered to allow low rate readout of pixel data. Frame buffering is currently not supported by the IRIS chips, but is planned for a future development. In meanwhile, the frame needs to be buffered using an external controller, which is being the case for the Visual Monitoring Camera (VMC). The flight-worthy VMC is currently being developed for the Scientific Projects Department and is proposed for missions such as XMM, Integral and Cluster-2. The VCM contains on-board memory for frame buffering and is controlled by a Field Programmable Gate Array (FPGA) (see figure 5 and figure 6).

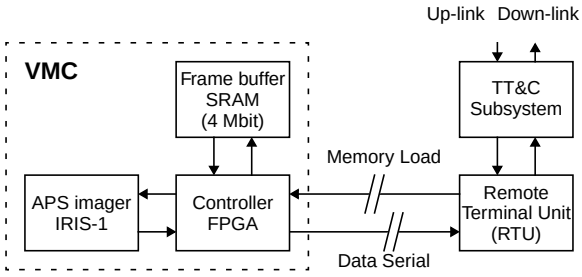

Figure 5: *Preliminary VMC architecture and usage.*

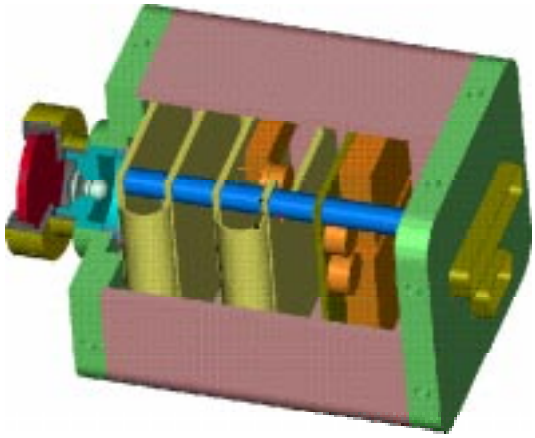

Figure 6: *Preliminary drawing of the VMC housing.*

7 DEVELOPMENT SCHEDULE

In Autumn 1997, the IRIS-1 version of the system, an imager to be used with an external component for control, went into production. At the sensor-level this chip has all the facilities of the full version. IRIS-1 was evaluated successfully at the time of writing this paper. The first demonstration breadboard to be developed with IRIS-1 will be based on this sensor with all externally logic required for the timing, control and interfaces implemented in an FPGA.

In Autumn 1998, IRIS-2 is to be designed, this time with on-chip integration of all logic for control and interfacing, forming the desired microcamera electronics. A demonstrator single-chip microcamera will be built. Extensive radiation testing of IRIS-2 is scheduled for 1999. The tests comprise total dose irradiation, and latch-up and single event upset assessment under heavy ion radiation.

After this, future versions of the IRIS chips will aim for higher resolution and a higher scan-rate. Also included will be an on-chip interface for a memory buffer, so that a compact two-chip imager and frame grabber can be built. Further interfaces will concentrate on linking the IRIS family directly to specific image compression chips, to yield a compressing microcamera.

The use of CMOS technology enables the sensor and the microcamera to be used as a versatile building-block in larger application-specific systems such as low end star trackers.

8 CONCLUSIONS

The IRIS general-purpose space monitoring microcamera combines CMOS Active Pixel Sensor technology and on-chip logic into a stand-alone system that easily interfaces with the spacecraft telemetry and the telecommand subsystem. The IRIS microcamera is being developed by IMEC (B), and is manufactured in the mixed-signal 0.7 µm CMOS process from Alcatel Mietec (B). The first demonstration camera is foreseen in 1998, comprising the IRIS-1 sensor. The fully integrated IRIS-2 microcamera chip is foreseen for spring 1999, with a demonstration camera in autumn 1999. Further development of the microcamera, featuring tight integration with a image compression chip etc., is being initiated, with results expected in early 2000.

9 ACKNOWLEDGEMENTS

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