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TM/TC interface glue logic for TeamSat spacecraft

Requirement and Functional Specification

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1. Introduction

1.1 Scope

This documents specifies the part of the TeamSat TM/TC interface glue logic that shall be implemented in FPGAs.

1.2 System overview

The FPGAs to be developed are to be used on two separate spacecraft with somewhat different functional requirements. The specification of the FPGAs has been made such that only one design needs to be developed, since it captures all requirements posed by the two spacecraft.

1.3 Schedule

The development of the FPGA related to the up-link should be completed within 3 weeks after this specification has been agreed upon.
The development of the FPGA related to the down-link should be completed within 5 weeks after this specification has been agreed upon.

Issue 2 of this specification was agreed upon on the 15 January 1997.

Any additions to the herein specified functions will require additional development time and potentially development of an additional FPGA.

1.4 Partitioning

The following three groups of functions have been identified:
- up-link interfaces;
- down-link interfaces;
- housekeeping data acquisition.

Since the TM/TC subsystems are to be implemented on different printed circuit boards, the three groups above shall be implemented in two FPGAs. However, the specification of the interfaces provides a total pin count which does not preclude the implementation of all functions in a single FPGA.

The up-link interfaces shall be implemented in the "TC-FPGA".
The down-link interfaces and the housekeeping data acquisition shall be implemented in the "TM-FPGA".

Both spacecraft require all three groups of functions listed above. The total number of FPGAs to be flown is therefore four.

1.5 Naming convention

Each signal is prefixed with an acronym of the equipment to which it interfaces. Note that some equipment interfaces with both the up and down-link, and the corresponding signals have therefore the same prefix. Each signal name is unique.

Signals with the suffix "_N" are active at logical 0.

Bit numbering is according to ESA PSS TM/TC numbering conventions, bit 0 is the most significant and is sent/received first.

For the asynchronous bit protocol (RS232 type, the least significant bit is sent/received first.

2. Interface overview

The different equipment to be interfaced are listed below. The total I/O pin count is 46+111=157.

2.1 Up-link interfaces

- MAP interface to the PTD TC decoder
- Bit asynchronous interfaces
  - GPS interface
  - Hitachi Processor interface
  - IBM PC Processor interface
  - AVS interface
  - Bandwidth Allocation Table (BAT) interface
- Synchronous TTC-B-01 interface
  - VTS interface
  - Redirected CPDU interface
- Delayed Command interface

2.2 Down-link interfaces

- Bit asynchronous interfaces
  - GPS interface
  - Hitachi Processor interface
  - FIPEX/IBM PC Processor interface
  - AVS interface
  - Bandwidth Allocation Table (BAT) interface
- Synchronous TTC-B-01 interfaces
  - VTS interface
- Housekeeping data acquisition
- Handshake signal conditioning

3. Specification of up-link interfaces

The total up-link pin count is 46.

3.1 MAP interface to the PTD TC decoder

User:	TEAM/YES
Inputs:	MAPCK (clock), MAPDSR (sample), MAPDATA (data)
Pin count:	3
Protocol:	as per PTD data sheet TC segments without packets. TC header used for routing: bit 0-1 ignored, bit 2-3 = "00", bit 4-7 used as address. ONLY SEGMENT DATA FIELD TRANSFERRED TO USER, FIRST OCTET OF A SEGMENT IS THUS DISCARDED SINCE USED FOR ROUTING. No checks. No flow control. No overrun protection.
Frequency:	F=fck/[2^x], x=9, fck=2.048 MHz, F=4000 Hz This assumption limits the up-link data rate to 4000 bits/s.

3.2 GPS interface

User:	TEAM/YES
Address:	MAP-1
Outputs:	GPSDATA (data)
Pin count:	1
Protocol:	Asynchronous bit protocol 9600 baud (RS232 type) 1 start, 8 data and 2 stop bits (no parity) No flow control

3.3 Hitachi Processor interface

User: TEAM/YES
Address: MAP-2
Outputs: HITDATA (data)
Pin count: 1
Commonality: as per 3.2

3.4 IBM PC Processor interface

User: YES
Address: MAP-3
Outputs: IBMDATA (data)
Pin count: 1
Commonality: as per 3.2

3.5 AVS interface

User: YES
Address: MAP-4
Outputs: AVSDATA (data)
Pin count: 1
Commonality: as per 3.2

3.6 VTS interface

User: TEAM
Address: MAP-5
Outputs: VTSHCS16 (clock), VTSMCS16 (sample), VTSDCS16 (data)
Pin count: 3
Protocol: TTC-B-01 type ML, effective output rate approximately 10k baud at bursts of 20k baud
No flow control
Note: the command description for the VTS numbers the MSB with 15 (to the left), and the LSB as 0 (to the right), when sent via the TTC-B-01 interfaces the MSB is sent first and the LSB last.

3.7 Redirected CPDU interface

User: TEAM/YES
Address: MAP-6
Outputs: RCPDCLK (clock), RCPDSAMPLE (sample), RCPDDATA (data)
Pin count: 3
Commonality: as per 3.6, but with RCPDSAMPLE asserted for the full segment

3.8 Spare interfaces

User: -
Address: MAP-7, MAP-8
Outputs: MAP7DATA, MAP8DATA (data)
Pin count: 2
Commonality: as per 3.2

3.9 Bandwidth Allocation Table (BAT) interface

User: TEAM/YES
Address: MAP-9
Outputs: BATDATA (data)
Pin count: 1
Commonality: as per 3.2

3.10 Delayed Command interface

User: TEAM/YES
Address: MAP-A for channel A, MAP-B for channel B, MAP-C for channel C
MAP-D for channel D, MAP-E for channel E, MAP-F for channel F
Outputs: CMDA[0:3], CMDB[0:3], CMDC[0:3],
CMDD[0:3], CMDE[0:3], CMDF[0:3] (commands)
CMDCLK (1 min clock), CMDCLK8 (8 sec clock)
Pin count: 26
Protocol: See further section 5.1
No flow control

3.11 System pins

This section defines the signals necessary for the operation of the FPGA and are not part of the requirements posed by the users.

Inputs: TCCLK (system clock), TCRESET_N (asynchronous reset)
TCCLK2 (2*1024*1024 Hz clock)
Outputs: TCCLK256 (256*1024 Hz clock)
Pin count: 4
Protocol: The TCRESET_N signal shall be clocked twice internally before fed to the core logic to avoid setup violations on flip-flops when de-asserted.
The TCCLK2 signal shall be divided to 262144 Hz = 2^18 Hz and output as TCCLK256. TCCLK256 shall be routed to the TCCLK input.

4. Specification of down-link interfaces

The total down-link pin count is 111.

4.1 GPS interface

User: TEAM/YES
Address: VCA-1/VCA-1
Inputs: GPSIN (data)
Outputs: GPSCLK (clock), GPSOUT (data) {VCA I/F}
Pin count: 3
Protocol: Asynchronous bit protocol 9600 baud (RS232 type)
1 start, 8 data and 1 stop bit (no parity)
No flow control
VC bit stream to VCA serial I/F

4.2 Hitachi processor interface

User: TEAM/YES
Address: VCA-2/VCA-2
Inputs: HITIN (data)
Outputs: HITCLK (clock), HITOUT (data) {VCA I/F}
Pin count: 3
Commonality: as per 4.1

4.3 FIPEX / IBM PC Processor interface

User: TEAM/YES
Address: VCA-3/VCA-3
Inputs: IBMIN (data)
Outputs: IBMCLK (clock, IBMXOUT (data) {VCA I/F}
Pin count: 3
Commonality: as per 4.1

4.4 AVS interface

User:	TEAM	
Address:	VCA-4	
Inputs:	AVSIN (data)	
Outputs:	AVSCLK (clock), AVSOUT (data)	{VCA I/F}
Pin count:	3	
Commonality:	as per 4.1, but with 19200 baud rate	

4.5 VTS interface

User:	TEAM	
Address:	VCA-5	
Inputs:	VTSDAS16 (data), VTSEMPTY (FIFO handshake)	{VTS I/F}
	VTSVCAR (VCA handshake)	{VCA I/F}
Outputs:	VTSHAS16 (clock), VTSMAS16 (sample)	{VTS I/F}
	VTSCLK (clock), VTSOUT (data)	{VCA I/F}
Pin count:	7	
Protocol:	TTC-B-01 type with flow control, effective throughput rate approximately 15 kbaud, VC bit stream (no knowledge/control of images etc.). See also section 3.6 regarding the MSB/LSB definition. The TM-FPGA shall generate clock and sample signals to retrieve data from the VTS and send it to the VCA when data is available and there is room in the VCA buffer. Data shall be retrieved as 16 bit words that are to be converted to a bit stream for the VCA serial input. The VTSVCAR signal indicates when there is room in the VCA buffer. The VTSEMPTY signal indicates when the VTS FIFO is empty and no data is available. VTSEMPTY is asserted when there is still 16 bits of data left in the FIFO, requiring one additional acquisition.	

4.6 Housekeeping

User:	TEAM/YES	
Address:	VCA-0/VCA-0	
Inputs:	HKDIGITAL[0:15] (digital inputs)	
	HKANALOG[0:7] (analogue data)	{ADC I/F}
	HKPERIODIC[0:15] (sun-sensor inputs)	
	HKTMD (data)	{PTD I/F}
	HKVCAR (VCA handshake), HKTIME (data)	
Outputs:	HKTIMELEVEL (data)	
	HKADDRESS[0:3] (address)	{ADC I/F}
	HKALE (latch address), HKSTART (convert)	{ADC I/F}
	HKTMC (clock), HKCPDUS, HKFAR1S, HKFAR2S (strobes)	{PTD I/F}
	HKCLK (clock), HKVALID (sample), HKOUT (data)	{VCA I/F}
	HKCYCLE (pulse)	
Pin count:	58	
Protocol:	See further section 5.2 TM packets to VCA serial I/F, flow control	

4.7 Handshake signal conditioning

User:	TEAM/YES
Inputs:	VCAR[0:7] (VCA ready), VCAON (TM system on)
Outputs:	VCARCON[0:7]
Pin count:	17
Protocol:	Each VCAR is and-ed with VCAON before output as VCARCON. These signals can be used by to accommodate flow control for the TM system. These signals are not used by the down-link interfaces above.

4.8 Bandwith Allocation Table (BAT) interface

User: TEAM/YES
Address: (to the VCM)
Inputs: BATIN (data)
Outputs: BATCS_N (chip select), BATWR_N (write strobe) {VCM I/F}
BATADDR[0:4] (address), BATDATA[0:2] (data) {VCM I/F}
Pin count: 11
Protocol: Asynchronous bit protocol 9600 baud (RS232 type)
1 start, 8 data and 1 stop bit (no parity)
No flow control. The received data is written to the VCM BAT interface. From the received data, bit 0-4 are output as address, and bit 5-7 are output as data. With a PTD MAP data rate of 4000 Hz, VCM frequencies from 2048 Hz and upwards can be supported without upsetting the VCM BAT interface timing.

4.8 TM clock generation

Outputs: TMCLK64 (64*1024 Hz clock)
TMCLK32 (32*1024 Hz clock)
Pin count: 2
Protocol: The TMCLK2 signal shall be divided to:
65536 Hz = 2^16 Hz and output as TMCLK64
(used for the Convolutional encoder)
32768 Hz = 2^15 Hz and output as TMCLK32
(used for the VCM and the RS encoder).
The maximum TM down-link data rate will thus be 32.7 kHz if using the above clock outputs.

4.9 System pins

This section defines the signals necessary for the operation of the FPGA and are not part of the requirements posed by the users.

Inputs: TMCLK (system clock), TMRESET_N (asynchronous reset)
TMCLK2 (2*1024*1024 Hz clock, 2^22 Hz)
Outputs: TMCLK256 (256*1024 Hz clock)
Pin count: 4
Protocol: The TMRESET_N signal shall be clocked twice before fed to the core logic to avoid setup violations on flip-flops when de-asserted.
The TMCLK2 signal shall be divided to 262144 Hz = 2^18 Hz and output as TMCLK256. TMCLK256 shall be routed to TMCLK.

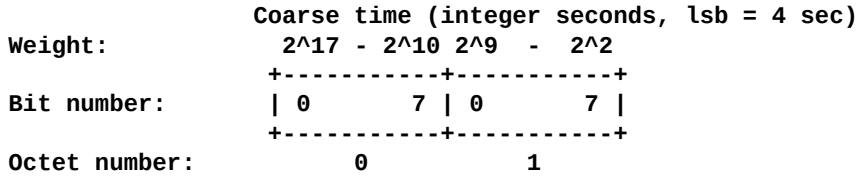
5 Detailed specifications

5.1 TC Delayed Command function

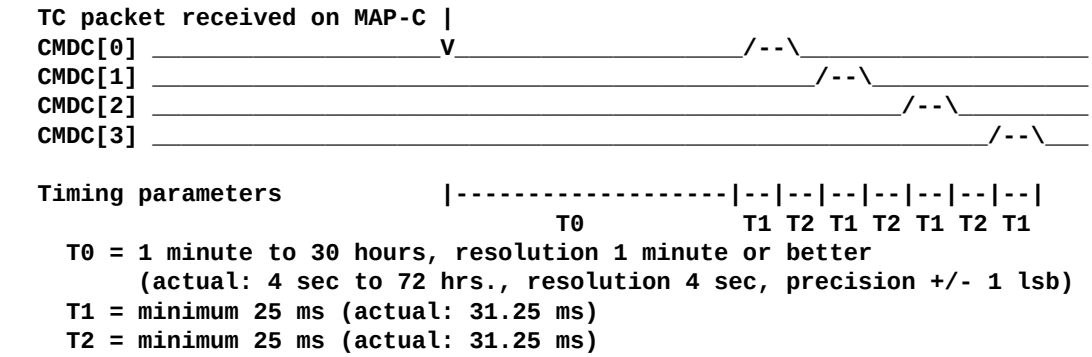
This function shall provide the user with six identical commanding channels. Each channel shall generate a fixed sequence of four pulses on four outputs after a delay that is programmable via the MAP interface. The delay code shall be 16 bits wide, allowing a resolution of at least 1 minute and a delay of up to 30 hours. The duration of each pulse shall be at least 25 ms, and the gap between each pulse on a channel shall be at least 25 ms. The delay code shall be sent in a separate TC packet for each channel and addressed to the corresponding MAP address, see further section 3.10.

The TC packet shall have the following structure:
6 octets packet header (which is ignored)
2 octets counter value

The uploadable counter value should have the following structure:



The following diagram illustrates the fixed pulse sequence for channel C:



T0 = 1 minute to 30 hours, resolution 1 minute or better
(actual: 4 sec to 72 hrs., resolution 4 sec, precision +/- 1 lsb)
T1 = minimum 25 ms (actual: 31.25 ms)
T2 = minimum 25 ms (actual: 31.25 ms)

A second TC packet sent while the counter is running shall re-initialise the counter without generating any immediate spurious pulses. A TC packet with the data filed all-zero shall reset and stop the generation without any spurious pulses. This block shall also provide a clock CMDCLK with the mean period of 1 minute, and a clock CMDCLK8 with the mean period of 8 seconds.

5.2 TM Housekeeping function

The housekeeping function samples digital inputs, acquires data from an ADC, retrieves CPDU and FAR status reports from the TC decoder, over samples sun-sensor inputs, provides a mission Elapsed Time counter and assembles a TM packet with the above information which is sent serially to a VCA.

The HK TM packet shall have the fixed length of 69 octets with the following contents:

- 6 octets packet header
- 4 octets fixed data
- 3 octets mission elapsed time counter (integer seconds)
- 2 octets 16 digital channels
- 6 octets telecommand status reports
- 16 blocks of:
  - 1 octet analogue channel data (8-bit resolution)
  - 2 octets 16 sun-sensor channels

The HK TM packet sampling and generation rate shall be 0.25 Hz, except for the sun-sensors which shall be over sampled at 4 Hz. The sampling shall be aligned with the Elapsed Time counter on integer seconds values.

In case HKVCAR is de-asserted when the generation of the HK packet is to begin, that packet shall not be generated and the acquisition shall be delayed until the next generation is due (i.e. 4 seconds later).

There shall be no explicit numeric requirement on the time accuracy of the sampling point. The implementation shall be made in a way that allows a low design complexity for the required accuracy.

5.2.1 TM packet header assembly

The TM packet header shall have the following format:

- Version: 100
- Type: 0
- Data Field Header Flag: 0
- Application Process ID: 11101110111 (777)hex
- Segmentation Flags: 11
- Source Sequence Count: ET coarse (bit 15-2, excluding other bits)
- Packet Length: 0000 0000 0011 1110 (003E)hex (63-1)dec

5.2.2 Fixed data

To allow ground segment operation without TM packet support, a fixed synchronisation pattern shall be included in the beginning of the TM packed data field. The following four octets shall be output:

Data Field Octet number:	Data: Fixed data
0	EB
1	90
2	C0
3	24

5.2.3 Elapsed Time counter

The mission Elapsed Time counter shall comply to the CUC standard with 24 bit coarse time and 2 bit fine time.

	Coarse time (integer seconds)				Fine time (sub-seconds)	
Weight:	2^23 - 2^16	2^15 -	2^8	2^7 -	2^0	2^-1 - 2^-2
ET bit:	23 - 16	15 - 8	7 - 0		-1	-2
Bit number:	0 - 7	0 - 7	0 - 7			

Data Field Octet number:	4	5	6

Only the coarse time shall be placed in the HK TM packet, giving a wrap around time of at least 10 days. Note: the ET MSB number is 23 and should be put in bit 0 of Data Field Octet number 4.

The fine time part shall generate an internal pulse suitable for initiating sampling of housekeeping data at 0.25 Hz and at 4 Hz. At the beginning of an actual housekeeping acquisition, a 125 ms (nominally) active high pulse shall be output on the HKCYCLE pin.

5.2.4 Digital channels

Each HKDIGITAL[0:15] input shall be clocked once before sampled into the HK TM packet.

Data Field Octet number:	Data: HKDIGITAL(index)
7	01234567
8	89ABCDEF

5.2.5 Telecommand status reports

The following telecommand status reports shall be read out from the PTD and included in the HK TM packet, the first bit received from the PTD shall be placed first in the HK TM packet:

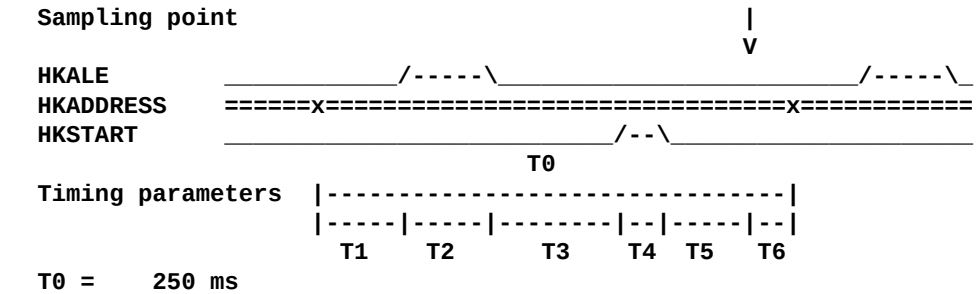
Data Field Octet number:	Data:	
9	CPDU	D0 - D7
10		D8 - D15
11	FAR1	D0 - D7
12		D8 - D15
13	FAR2	D16 - D23
14		D24 - D31

5.2.6 Analogue channels

The 16 analogue channels shall be sampled and the corresponding octet shall be placed in the TM HK packet in the following order:

Data Field Octet number:	Data: HKADDRESS[0:3]	Sampling time:
15	0000	T0=0.25 sec
18	0001	T0=0.50 sec
21	0010	T0=0.75 sec
24	0011	T0=1.00 sec
27	0100	T0=1.25 sec
30	0101	T0=1.50 sec
33	0110	T0=1.75 sec
36	0111	T0=2.00 sec
39	1000	T0=2.25 sec
42	1001	T0=2.50 sec
45	1010	T0=2.75 sec
48	1011	T0=3.00 sec
51	1100	T0=3.25 sec
54	1101	T0=3.50 sec
57	1110	T0=3.75 sec
60	1111	T0=4.00 sec

Waveform diagram:



T0 = 250 ms
T1 = +/- 50 ms (actual 47.85 ms)
T2 = +/- 50 ms (actual 46.875 ms)
T3 = +/- 50 ms (actual 78.125 ms)(minimum 10 ms)
T4 = +/- 50 ms (actual 31.25 ms)
T5 = +/- 50 ms (actual 40 ms)
T6 = +/- 0 ms (actual 5.9 ms)

Bit 0 is the MSB for the HKANALOG[0:7] data bus, and bit 7 is the LSB.

The ADC0816 "8-Bit Microprocessor Compatible A/D Converter with 16-Channel Multiplexer" analogue to digital converter from National Semiconductor shall be interfaced.

5.2.7 Sun-sensor channels

The sun-sensor inputs HKPERIODIC[0:15] shall be sampled four times per second, resulting in 16 bits per input and HK TM packet. Each input shall be clocked once before sampled. For each sampling moment, all 16 inputs shall be sampled and placed consecutively in the HK TM packet. Therefore, the sun-sensor data shall have the following format:

Data Field Octet number:	Data: HKPERIODIC[index]	Sampling time:
16	01234567	T0+0.25 sec
17	89ABCDEF	
19	01234567	T0+0.50 sec
20	89ABCDEF	
22	01234567	T0+0.75 sec
23	89ABCDEF	
25	01234567	T0+1.00 sec
26	89ABCDEF	
..	....	
61	01234567	T0+4.00 sec
62	89ABCDEF	

5.2.8 VCA Time strobe conditioning

The Time strobe from the VCA is asserted for a small number of clock cycles and it is therefore not possible to sample it by the digital input interface described above. To overcome this limitation, a flip-flop shall be provided that shall toggle on each 0-to-1 transition on the HKTIME input. The flip-flop output HKTIMELEVEL will make it possible to sample on one of the digital inputs above if required. The resolution with which the occurrence of the Time strobe pulse can be measured will then be 4 seconds.

6. Clock frequencies

6.1 TC-FPGA operating frequency

The following requirements shall be met:
- the up-link interfaces shall have a data output rate higher than the MAP interface (9600 bit per second is the lowest output data rate)
- the MAP interface input data rate depends on the PTD system clock Fck (assumed to be 2.048 MHz)
- the MAP bit clock can be programmed as F=fck/[2^x] where x={1:13}
- MAP data rate shall be less than the lowest output: rate x=9, F=4000 Hz
- if possible, the same crystal type shall be used for the two FPGAs
- the CMD counters require the base frequency to be a power of 2;

Therefore, the frequency for the TC-FPGA system clock TCCLK shall be 2^18 Hz = 262144 Hz = 262 kHz = 256*1024 Hz.

6.2 TM-FPGA operating frequency

The following requirements shall be met:
- the ET counter requires the base frequency to be a power of 2;
- shall allow 3 times over sampling of any input data: f > 57600 = 19200*3

Therefore, the frequency for the TM-FPGA system clock TMCLK shall be 2^18 Hz = 262144 Hz = 262 kHz = 256*1024 Hz.
For all down-link interfaces, the bit serial interface of the VCA shall be used. The down-link data rate for the VCM is assumed to be 32768 Hz. The VCA operating frequency is assumed to be 65536 Hz or higher. The highest input data rate to the TM-FPGA is 19.2 kbit/s, making it sufficient to output data to the VCA at 2^15 = 32768 = 32.8 kbit/s, without violating the input rate requirements for the VCA or saturating the TM-FPGA.

7. Electrical specification

7.1 Absolute maximum ratings

Supply voltage	Vcc:	-0.5 to +7.0 V
Input voltage	Vi:	-0.5 to VCC+0.5 V
Output voltage	Vo:	-0.5 to VCC+0.5 V
Storage temperature	Tstg:	-65 to +150 degrees Celsius

7.2 Recommended operating conditions

Nominal power supply voltage Vcc: 5.0 V

	Commercial	Industrial	Military	
Ambient temperature range:	0 to +70	-40 to +85	-55 to +125	degrees Celsius
Power supply tolerance:	+/-5	+/-10	+/-10	%Vcc

7.3 Input voltage (TTL type)

	Min	Max	Comment
VIL:	-0.3 V	0.8 V	commercial
VIH:	2.0 V	Vcc+0.3 V	commercial

7.4 Output voltage (CMOS type)

	Min	Max	Comment
VOL:		0.5 V	at Vcc min, IOL = 10 mA, commercial
VOH:	3.84 V		at Vcc min, IOH = -6 mA, commercial

7.5 Reliability

It shall be noted that the suggested ACTEL 1280A FPGA is not radiation tolerant and is sensitive to Single Event Upsets (SEU), potentially resulting in loss of services.

8. Mechanical specification

8.1 Component type and package specification

The ACTEL 1280A FPGA shall be used in a 176-pin CPGA package. It is preferred that components of military or better quality are used, since commercial ACTEL components have a limited operating temperature range.

8.2 Pin assignment

8.2.1 TC-FPGA pinout

Number	Name	I/O	Type	Description
A13	MAPCK	I	TTL	Clock from PTD serial MAP I/F
A14	MAPDSR	I	TTL	Sample from PTD serial MAP I/F
A15	MAPDATA	I	TTL	Data from PTD serial MAP I/F
A2	GPSDATA	O	CMOS	Asynchronous bit serial data to GPS
A3	HITDATA	O	CMOS	Asynchronous bit serial data to Hitachi
A4	IBMDATA	O	CMOS	Asynchronous bit serial data to IBM PC
A5	VTSHCS16	O	CMOS	Clock to VTS TTC-B-01 ML I/F
A6	VTSMCS16	O	CMOS	Sample to VTS TTC-B-01 ML I/F
A7	VTSDCS16	O	CMOS	Data to VTS TTC-B-01 ML I/F
A10	RCDPCLK	O	CMOS	Clock to Redirected CPDU TTC-B-01 ML I/F
A11	RCPDSAMPLE	O	CMOS	Sample to Redirected CPDU TTC-B-01 ML I/F
A12	RCPDDATA	O	CMOS	Data to Redirected CPDU TTC-B-01 ML I/F
B1	AVSDATA	O	CMOS	Asynchronous bit serial data to AVS
E1	MAP7DATA	O	CMOS	Asynchronous bit serial data
F1	MAP8DATA	O	CMOS	Asynchronous bit serial data
G1	BATDATA	O	CMOS	Asynchronous bit serial data
R3	CMDA[0]	O	CMOS	Pulse for CMD channel A
R4	CMDA[1]	O	CMOS	Pulse for CMD channel A
R5	CMDA[2]	O	CMOS	Pulse for CMD channel A
R6	CMDA[3]	O	CMOS	Pulse for CMD channel A
R7	CMDB[0]	O	CMOS	Pulse for CMD channel B
R8	CMDB[1]	O	CMOS	Pulse for CMD channel B
R9	CMDB[2]	O	CMOS	Pulse for CMD channel B
R10	CMDB[3]	O	CMOS	Pulse for CMD channel B
R11	CMDC[0]	O	CMOS	Pulse for CMD channel C
R12	CMDC[1]	O	CMOS	Pulse for CMD channel C
R13	CMDC[2]	O	CMOS	Pulse for CMD channel C
R14	CMDC[3]	O	CMOS	Pulse for CMD channel C
R15	CMDD[0]	O	CMOS	Pulse for CMD channel D
P15	CMDD[1]	O	CMOS	Pulse for CMD channel D
N15	CMDD[2]	O	CMOS	Pulse for CMD channel D
M15	CMDD[3]	O	CMOS	Pulse for CMD channel D
L15	CMDE[0]	O	CMOS	Pulse for CMD channel E
K15	CMDE[1]	O	CMOS	Pulse for CMD channel E
J15	CMDE[2]	O	CMOS	Pulse for CMD channel E
H15	CMDE[3]	O	CMOS	Pulse for CMD channel E
G15	CMDF[0]	O	CMOS	Pulse for CMD channel F
F15	CMDF[1]	O	CMOS	Pulse for CMD channel F
E15	CMDF[2]	O	CMOS	Pulse for CMD channel F
D15	CMDF[3]	O	CMOS	Pulse for CMD channel F
R1	CMDCLK	O	CMOS	1 minute clock for CMD
R2	CMDCLK8	O	CMOS	8 sec clock for CMD
A9	TCCLK	I	TTL	System clock at 256*1024 Hz
A1	TCRESET_N	I	TTL	Asynchronous reset
B8	TCCLK2	I	TTL	Clock at 2*1024*1024 Hz
B9	TCCLK256	O	TTL	Clock at 256*1024 Hz (connect to TCCLK)

8.2.2 TM-FPGA pinout

Number	Name	I/O	Type	Description
D1	GPSIN	I	TTL	Asynchronous bit serial data from GPS
D2	GPSCLK	O	CMOS	Clock to VCA bit serial I/F
D3	GPSOUT	O	CMOS	Data to VCA bit serial I/F
E1	HITIN	I	TTL	Asynchronous bit serial data from Hitachi
E2	HITCLK	O	CMOS	Clock to VCA bit serial I/F
E3	HITOUT	O	CMOS	Data to VCA bit serial I/F
F1	IBMIN	I	TTL	Asynchronous bit serial data FIPEX/IBM
F2	IBMCLK	O	CMOS	Clock to VCA bit serial I/F
F3	IBMOUT	O	CMOS	Data to VCA bit serial I/F
G1	AVSIN	I	TTL	Asynchronous bit serial data from AVS
G2	AVSCLK	O	CMOS	Clock to VCA bit serial I/F
G3	AVSOUT	O	CMOS	Data to VCA bit serial I/F
J1	VTSDAS16	I	TTL	Data from VTS TTC-B-01 SD I/F
H1	VTSEMPTY	I	TTL	FIFO empty from VTS
K13	VTSVCAR	I	TTL	Ready to receive from VCA
K1	VTSHAS16	O	CMOS	Clock to VTS TTC-B-01 SD I/F
K2	VTSMAS16	O	CMOS	Sample to VTS TTC-B-01 SD I/F
J2	VTSCLK	O	CMOS	Clock to VCA bit serial I/F
J3	VTSOUT	O	CMOS	Data to VCA bit serial I/F
M7	BATIN	I	TTL	Asynchronous bit serial data for BAT
N4	BATCS_N	O	CMOS	Chip select for VCM BAT I/F
N10	BATWR_N	O	CMOS	Write strobe for VCM BAT I/F
N11	BATADDR[0]	O	CMOS	Address for VCM BAT I/F (MSB)
N12	BATADDR[1]	O	CMOS	Address for VCM BAT I/F
N13	BATADDR[2]	O	CMOS	Address for VCM BAT I/F
N14	BATADDR[3]	O	CMOS	Address for VCM BAT I/F
N15	BATADDR[4]	O	CMOS	Address for VCM BAT I/F (LSB)
N5	BATDATA[0]	O	CMOS	Data for VCM BAT I/F (MSB)
N6	BATDATA[1]	O	CMOS	Data for VCM BAT I/F
N7	BATDATA[2]	O	CMOS	Data for VCM BAT I/F (LSB)
P1	HKDIGITAL[0]	I	TTL	Digital channel input
P2	HKDIGITAL[1]	I	TTL	Digital channel input
P3	HKDIGITAL[2]	I	TTL	Digital channel input
P4	HKDIGITAL[3]	I	TTL	Digital channel input
P5	HKDIGITAL[4]	I	TTL	Digital channel input
P6	HKDIGITAL[5]	I	TTL	Digital channel input
P7	HKDIGITAL[6]	I	TTL	Digital channel input
P8	HKDIGITAL[7]	I	TTL	Digital channel input
R1	HKDIGITAL[8]	I	TTL	Digital channel input
R2	HKDIGITAL[9]	I	TTL	Digital channel input
R3	HKDIGITAL[10]	I	TTL	Digital channel input
R4	HKDIGITAL[11]	I	TTL	Digital channel input
R5	HKDIGITAL[12]	I	TTL	Digital channel input
R6	HKDIGITAL[13]	I	TTL	Digital channel input
R7	HKDIGITAL[14]	I	TTL	Digital channel input
R8	HKDIGITAL[15]	I	TTL	Digital channel input
L1	HKANALOG[0]	I	TTL	Analogue channel input (MSB)
L2	HKANALOG[1]	I	TTL	Analogue channel input
L3	HKANALOG[2]	I	TTL	Analogue channel input
M1	HKANALOG[3]	I	TTL	Analogue channel input
M2	HKANALOG[4]	I	TTL	Analogue channel input
M3	HKANALOG[5]	I	TTL	Analogue channel input
N1	HKANALOG[6]	I	TTL	Analogue channel input
N2	HKANALOG[7]	I	TTL	Analogue channel input (LSB)

Number	Name	I/O	Type	Description
M9	HKPERIODIC[0]	I	TTL	Sun-sensor channel input
N9	HKPERIODIC[1]	I	TTL	Sun-sensor channel input
P9	HKPERIODIC[2]	I	TTL	Sun-sensor channel input
P10	HKPERIODIC[3]	I	TTL	Sun-sensor channel input
P11	HKPERIODIC[4]	I	TTL	Sun-sensor channel input
P12	HKPERIODIC[5]	I	TTL	Sun-sensor channel input
P13	HKPERIODIC[6]	I	TTL	Sun-sensor channel input
P14	HKPERIODIC[7]	I	TTL	Sun-sensor channel input
P15	HKPERIODIC[8]	I	TTL	Sun-sensor channel input
R9	HKPERIODIC[9]	I	TTL	Sun-sensor channel input
R10	HKPERIODIC[10]	I	TTL	Sun-sensor channel input
R11	HKPERIODIC[11]	I	TTL	Sun-sensor channel input
R12	HKPERIODIC[12]	I	TTL	Sun-sensor channel input
R13	HKPERIODIC[13]	I	TTL	Sun-sensor channel input
R14	HKPERIODIC[14]	I	TTL	Sun-sensor channel input
R15	HKPERIODIC[15]	I	TTL	Sun-sensor channel input
A3	HKTMC	O	CMOS	Clock to PTD serial status report I/F
A4	HKCPDUS	O	CMOS	Sample to PTD serial status report I/F
B4	HKFAR1S	O	CMOS	Sample to PTD serial status report I/F
C4	HKFAR2S	O	CMOS	Sample to PTD serial status report I/F
A2	HKTMD	I	TTL	Data from PTD serial status report I/F
B15	HKVCAR	I	TTL	Ready to receive from VCA
A15	HKTIME	I	TTL	Time strobe from VCA
A11	HKTIMELEVEL	O	CMOS	Conditioned Time strobe
A5	HKADDRESS[0]	O	CMOS	Address to analogue multiplexer (MSB)
A6	HKADDRESS[1]	O	CMOS	Address to analogue multiplexer
A7	HKADDRESS[2]	O	CMOS	Address to analogue multiplexer
A8	HKADDRESS[3]	O	CMOS	Address to analogue multiplexer (LSB)
B5	HKALE	O	CMOS	Latch address in analogue multiplexer
B6	HKSTART	O	CMOS	Start analogue conversion
A14	HKCLK	O	CMOS	Clock to VCA bit serial I/F
A12	HKVALID	O	CMOS	Sample to VCA bit serial I/F
A13	HKOUT	O	CMOS	Data to VCA bit serial I/F
A10	HKCYCLE	O	CMOS	Indication of HK acquisition start
C14	VCAR[0]	I	TTL	Ready to receive from VCA
D14	VCAR[1]	I	TTL	Ready to receive from VCA
E14	VCAR[2]	I	TTL	Ready to receive from VCA
F14	VCAR[3]	I	TTL	Ready to receive from VCA
G14	VCAR[4]	I	TTL	Ready to receive from VCA
K14	VCAR[5]	I	TTL	Ready to receive from VCA
L14	VCAR[6]	I	TTL	Ready to receive from VCA
M14	VCAR[7]	I	TTL	Ready to receive from VCA
H15	VCAON	I	TTL	TM sub-system powered-on signal
C15	VCARCON[0]	O	CMOS	Conditioned VCAR[0]
D15	VCARCON[1]	O	CMOS	Conditioned VCAR[1]
E15	VCARCON[2]	O	CMOS	Conditioned VCAR[2]
F15	VCARCON[3]	O	CMOS	Conditioned VCAR[3]
G15	VCARCON[4]	O	CMOS	Conditioned VCAR[4]
K15	VCARCON[5]	O	CMOS	Conditioned VCAR[5]
L15	VCARCON[6]	O	CMOS	Conditioned VCAR[6]
M15	VCARCON[7]	O	CMOS	Conditioned VCAR[7]
A9	TMCLK	I	TTL	System clock
A1	TMRESET_N	I	TTL	Asynchronous reset
B8	TMCLK2	I	TTL	Clock at 2*1024*1024 Hz
B9	TMCLK256	O	CMOS	Clock at 256*1024 Hz (connect to TMCLK)
B11	TMCLK64	O	CMOS	Clock at 64*1024 Hz
B12	TMCLK32	O	CMOS	Clock at 32*1024 Hz

8.2.3 Fixed ACTEL pinout

Number	Name	I/O	Type	Description
D4	GND	P		Ground
E4	GND	P		Ground
G4	GND	P		Ground
H4	GND	P		Ground
K4	GND	P		Ground
L4	GND	P		Ground
M4	GND	P		Ground
M6	GND	P		Ground
M8	GND	P		Ground
M10	GND	P		Ground
M12	GND	P		Ground
K12	GND	P		Ground
J12	GND	P		Ground
H12	GND	P		Ground
F12	GND	P		Ground
E12	GND	P		Ground
D12	GND	P		Ground
D10	GND	P		Ground
C8	GND	P		Ground
D6	GND	P		Ground
F4	VCC	P		Power
H3	VCC	P		Power
J4	VCC	P		Power
M5	VCC	P		Power
N8	VCC	P		Power
M11	VCC	P		Power
H13	VCC	P		Power
G12	VCC	P		Power
D11	VCC	P		Power
D8	VCC	P		Power
D5	VCC	P		Power
C3	MODE	I	TTL	tie to GND (normal operation)
J13	VKS	P		tie to GND
J14	VPP	P		tie to VCC
H2	VSV	P		tie to VCC
H14	VSV	P		tie to VCC

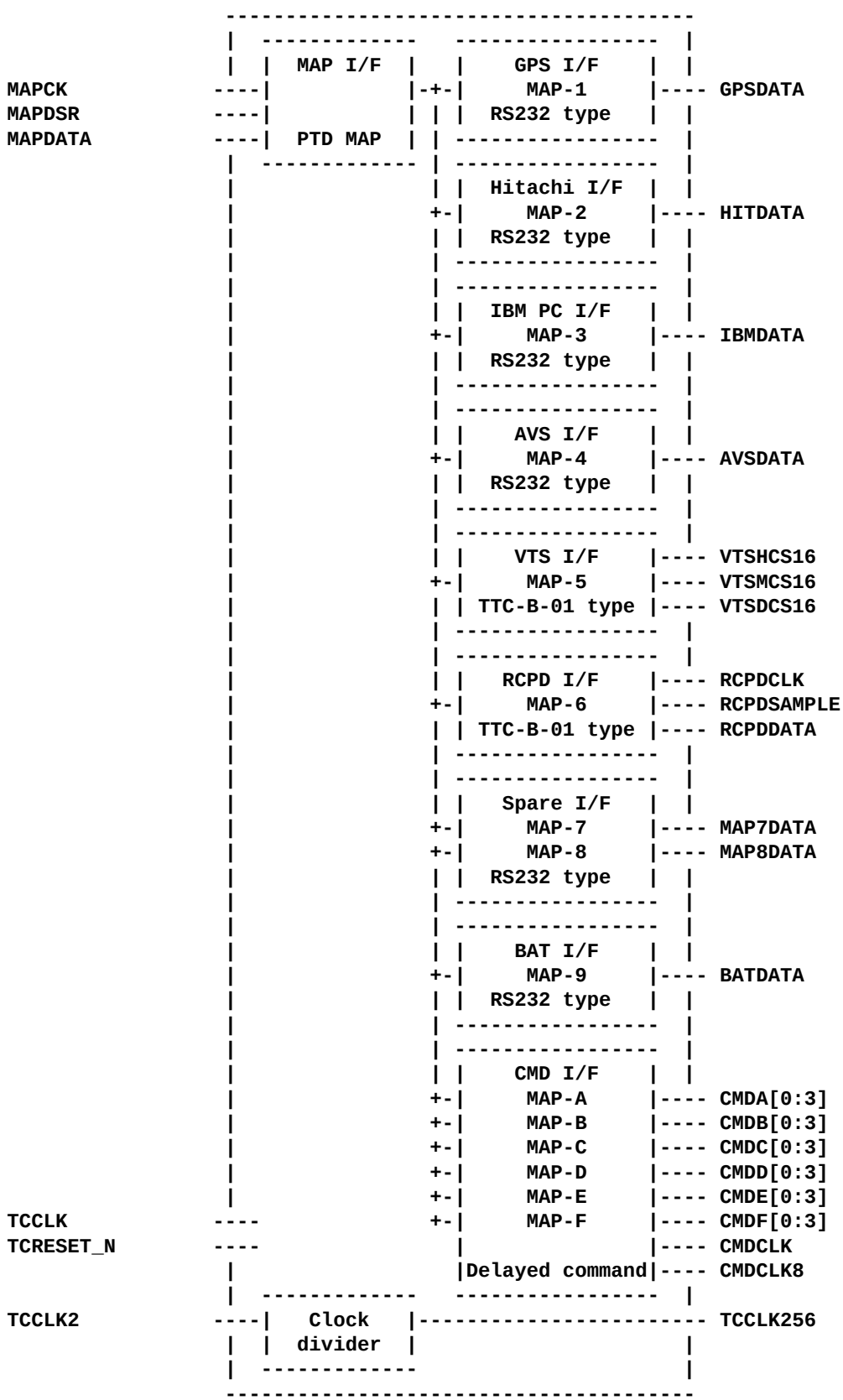
The following pins shall be left unconnected on the printed circuit board, and will drive a logic 0.

B3	DCLK	O	CMOS	(programmed as output)
C9	PRA	O	CMOS	(programmed as output)
D7	PRB	O	CMOS	(programmed as output)
B14	SDI	O	CMOS	(programmed as output)

All unused I/O pins shall be programmed as outputs and be left unconnected on the printed circuit board, allowing them to be used for potential patches. These pins will drive a logic 0.

9. Block diagrams

9.1 TC-FPGA block diagram



9.2 TM-FPGA block diagram