VHDL Modeling, Test, and Distribution

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Abstract

This paper presents the ongoing effort of the Mississippi State University / Microsystems Prototyping Laboratory (MSU/MPL) executed as part of the RASSP Technology Base Program. The research underway includes: VHDL model development, VHDL test bench synthesis, and utilization of the World Wide Web (WWW) to document and distribute models, tools, and information.

To date, modeling guide lines have been implemented for PROMs, SRAMs, Dual–Port SRAMs, FIFOs, and PLDs. Successful models have been developed using these guidelines. Guidelines for CPLDs and FPGAs are currently being developed.

A VHDL Test Bench Synthesis Tool has been developed and is scheduled for beta testing in July 1995. This tool automatically generates VHDL test benches and allows for vendor independent testing methodologies of VHDL designs.

The World Wide Web (WWW) is being used to document and release the VHDL models developed. Complete datasheets for sample models have been developed and posted to the Web as an example of hierarchical electronic datasheets.

1 Overview

Mississippi State University's Microsystems Prototyping Laboratory (MPL) has been contracted as part of the RASSP Technology Base to develop VHDL models of selected Cypress Semiconductor standard integrated circuits. Mississippi State and Cypress have entered into an agreement whereby Cypress will provide timing information necessary to create VHDL models of high quality and accuracy to be released as part of the RASSP program. MPL is also under contract to deliver VHDL–based tools which will assist the model developer in testing created VHDL models. Finally, MPL will be participating in the RASSP Educator/Facilitator (E/F) through the development and release of an HTML–based VHDL course (*this effort is currently non–funded*). The VHDL course can be accessed from the URL ***http://WWW.ERC.MsState.Edu/mpl/rassp/html/overview.html***

2 VHDL Modeling at MSU

MSU has been tasked to provide VHDL models for standard Off–The–Shelf (OTS) logic devices. Initial models chosen are parts provided by Cypress Semiconductor, Inc. Cypress has a design division located in Starkville, MS where many of the components targeted for modeling were designed. This affords ready access to internal data which may be needed to insure the accuracy and performance of developed models. Cypress has entered an agreement to work with MSU to provide all component information necessary to deliver to the RASSP program the highest quality of models possible.

2.1 Modeling Overview

The program calls for MSU to address the following part types:

1. PROM
2. SRAM
3. Dual–Port SRAM
4. FIFO
5. PLD
6. CPLD
7. FPGA

MSU's modeling strategy consists of developing baseline methodologies for each part type listed above. After the baseline methodology is developed for a part type, a sample part model is constructed and verified. These sample part models are then used to expand the part

models horizontally (across the same part type). The following subsections describe the development strategy for differing part types.

2.1.1 PROMs and Single Port SRAMs

Large PROMs and SRAMS can require excessive amounts of memory for simulation, especially in large system level simulations. Avoiding this presents many modeling challenges. To help address some of these challenges, two approaches were taken. One approach, suitable for ROM and small RAM models, was to use a general memory package which statically allocates all model storage. The second approach was to develop a general memory package which dynamically allocates all model storage and provides user–controlled options for swapping memory pages to disk. This second approach is suitable for small and large RAM models. Also, packages were used to implement the basic RAM functions. These packages help yield RAM models with approximately 98% common code with timing packages accounting for most of the non–shared code.

2.1.2 Dual–Port SRAMs

Dual–Port SRAMS inherit many of the same challenges as the PROMs and SRAMS. They therefore can use many of the same solutions. Additional modeling challenges include complex timing issues. These timing issues were handled in the traditional manner.

2.1.3 FIFOs

FIFOs also present complex timing issues. These were readily handled in the traditional manner. This includes utilizing common packages for timing violation checks and the ability to control generation of assertion messages and 'X' propagation through generics.

2.1.4 PLDs

PLDs present some interesting challenges for modeling. The main challenge is to provide a model that is reasonable in performance. This was done by making extensive use of VHDL's generate statements and the JEDEC fuse map. A package (jedec_reader) has been written that will read a valid JEDEC file and extract the following fields from the JEDEC file: QF (Number of Fuses in Device), F (Default Fuse State), C (Fuse Map Checksum), and L (Fuse List). The jedec_reader package then performs the checksum calculation and returns the fuse list as a Bit_Vector. This Bit_Vector is then used in models to generate the AND/OR plane and the configuration of macrocells for the PLD. By making extensive use of VHDL's generate statements, only the needed logic is generated and this generation occurs at elaboration time. This methodology provides models with reasonable simulation performance. Successful models have been developed using this methodology.

2.1.5 CPLDs and FPGAs

CPLDs and FPGAs present even greater modeling challenges. These challenges include providing highly accurate timing models with reasonable simulation performance. To accurately model timing for these devices, internal details and timing of these complex parts from the vendor is a must. Our CPLD modeling plans center around the Cypress MAX340 and FLASH370 families, while the FPGA modeling plans center around the Cypress pASIC380 family. At this time we have held only preliminary discussions with Cypress concerning possible modeling approaches. Modeling of these part types is to begin with the second year funding beginning in July.

2.2 VHDL Component Modeling Issues

The quantity of VHDL component models available today is still relatively small. Therefore, there are and will be a number of modeling issues with regard to VHDL component models. Several guidelines and standards exist to help solve many of the modeling related issues. These include the IEEE Standard 1164 VHDL package (std_logic_1164), VHDL Initiative Toward ASIC Libraries (VITAL), Die Information Exchange for Timing (DIET), and VHDL Hardware Component Modeling and Interface Standard (EIA–567). Std_logic_1164 is an IEEE standard VHDL package that defines a standard describing the interconnection data types used in vhdl modeling. VITAL is a Model Development Specification for ASIC libraries. DIET is a format for describing timing information about digital Integrated Circuits. EIA–567 is a guideline for component modeling. Of these, the std_logic_1164 package and EIA–567 are directly related to component modeling. Some modeling related issues are discussed below.

2.2.1 EIA–567A

The EIA–567A specification is being used as a guideline for model development. The EIA–567A (VHDL Hardware Component Modeling and Interface Standard) was developed to "provide guidelines for the production of VHDL models for hardware descriptions that conform to a common signal interface convention; possess common simulation capabilities; are reusable as library elements of

other designs; support multiple source procurement; support technology independent reprocurement." To help accomplish this, the EIA–567A defines three packages to help represent "views" of a model. These views are the electrical view, physical view, and timing view. To date, the timing view package has been utilized to a limited extent.

There are some deviations when the standard is lacking or unclear. The EIA–567A specifies methods for input wire delays, output load delays, and for controlling 'X'–value and message generation on timing violations via the use of generics. These methods are observed by these models. Different speed grades of parts is one issue not addressed by the EIA–567A. This was handled by adding another dimension (speed_grade) to the timing arrays in the timing view package. The EIA–567A makes the assumption that for a given component you have Minimum, Nominal, and Maximum timing data. This is not always the case. The EIA–567A does provide some guidelines for estimating these values, but this distracts from the accuracy of the models. Also, the suggested naming conventions of EIA–567A were not used. Instead, databook timing parameter names were used. Also, some complex timing guidelines are not set forth in EIA–567A. Not using databook timing parameter names puts a burden on the model writer to deal with timing parameter name translation which can be error–prone. This also makes the model source code more obtuse to external readers who know the databook timing parameters and are not familiar with the EIA–567A specification.

2.2.2 Model Portability and Interoperability

MSU has tested the models on many different simulation platforms to ensure portability. Simulation platforms available included Leapfrog (Cadence Design Systems), Voyager (Ikos Systems), QuickVHDL (Mentor Graphics), VSS (Synopsys), and Optium (Vantage Analysis Systems).

As per EIA–567A, the models utilize the IEEE–1164 standard logic package for the state/strength value system of the models. MSU will utilize the MSU–RASSP developed TestView environment to automatically create testbenches for help in verification. In addition, MSU plans to work with other RASSP Technology Base contractors to create VHDL simulations which demonstrate the viability of VHDL as a simulation media throughout the RASSP design process.

3 VHDL Tool Development and Beta Release

VHDL support tools, i.e., TestView — a VHDL testbench synthesis tool, are being developed at MSU and will be released and beta tested via the Web. Realizing the importance of high quality software, MSU is making an effort to define a software development process. An integral part of this process is the beta test – redesign loop which assures that the release product is relatively error free. In an attempt to mirror efforts by the modeling group, the beta release and bug feedback will be performed via the Web. The URL for the beta release is ***http://www.erc.msstate.edu/mpl/rassp/tools/html/index.html***

3.1 TestView Development

TestView was developed at MSU to provide vendor independence for distributed testbenches. In an attempt to facilitate platform independence, TestView's original OpenLook interface has been redesigned and implemented in Motif, the industry standard for X. Before the redesign effort began, MSU developed an initial software development process in an attempt to provide quality control on all further software efforts.

The redesign began with translating all of the original TestView's functionality and menus into the Motif environment. Once this task is completed and verified by the testing team, TestView will be released as a beta test. Beta test sites, updates to the beta, and the resulting bug reports will all be managed via the WWW.

3.2 Beta Release and Bug Feedback Mechanism

TestView beta release and bug feedback will be managed via the WWW. Beta testers must register their sites in order to acquire the TestView beta. This information is databased for future analysis and update retrieval control. The procedure for beta test site registration is as follows:

1. Beta test registration and release is an extension of the RASSP Tools page.
2. Test site information is databased according to email address for future analysis:
   - full name,
   - email address,
   - company/organization and its type (educational, military, commercial, other),
   - platforms requested,
   - projected TestView usage.
3. Successful completion of site registration process used to access beta release
   - single file for the beta release (contains all platforms requested),
   - ftp transfer to user site,
   - each transfer and subsequent updates logged.

A bug feedback mechanism will also be implemented via the Web. This will allow for a controlled manner with

which to submit bugs to the developers of TestView. The procedure for reporting a bug in the TestView beta is as follows:

1. Bug reporting is an extension of the RASSP Tools page.
2. Bug information is databased according to current bug number for developers to fix
   - version of TestView,
   - type of bug (Fatal, Generated Testbench doesn't work, etc.),
   - description of bug,
   - description of procedure that caused the bug.

4 Model Documentation and Release

VHDL component models developed by MSU are being documented and released via the World Wide Web (WWW). MSU has obtained permission from Cypress to post Web versions of the three component datasheets representing part of the initial model release. The model release mechanism will be built into the electronic datasheet for each part. Because of export restrictions on RASSP deliverables, VHDL model release will be available for all models produced by MSU but limited to RASSP program participants. The URL for the VHDL model library is ***http://www.erc.msstate.edu/mpl/rassp/cgi/cypress.pl***.

4.1 WWW Component Datasheets

The WWW component datasheets are viewable from the URL listed above. This presents the overall Cypress BiCMOS/CMOS Databook from which the datasheets for the parts to be modeled are contained. Traversal of the databook homepage reveals sections for part types (STATIC RAMS, PROMS, PLDS, FIFOS). Each listing in these part types document represents a part that is either modeled or is projected to be modeled. Those which are complete are hyperlinked to the homepage for the individual circuit. Full electronic datasheets are available for the CY7C199 STATIC RAM, CY7C256 EPROM, and the PAL22V10D PLD.

4.2 WWW Component Model Release

RASSP VHDL models are export restricted. For initial releases from the RASSP Technology Base programs, the models are being released via the WWW utilizing restricted access and data encryption. There will be a single point of contact for model release per RASSP contractor or government organization. The procedure for release of RASSP VHDL models is as follows:

1. Model release is an extension of the WWW component datasheet.
2. VHDL Model portion of the WWW component datasheet is http access protected with user/password required for access.
3. Data encryption (*des*) is utilized with user key assigned by MSU.
4. User/passwd/deskey authentication required:
   - single point RASSP contractor release,
   - phone call authentication required,
   - user/passwd/deskey assigned over phone.
5. WWW user/passwd used to access release for in component datasheet:
   - single file for each model,
   - des encryption prior to transfer,
   - ftp transfer to user site,
   - des decryption by user with deskey,
   - each transfer logged.

The VHDL model portion of the WWW component datasheet features a source code review section along with the model release section. The source code review section allows users to view the source code of models prior to download. The model release section features an application which reads the head of each model informing the user of the version number, functionality, platforms tested, and other useful information which is extracted directly from the source code.

5 Models Released to Date (06–01–95)

PROMs	
cy7c256	32K x 8 Power–Switched and Reprogrammable PROM
cy7c266	8K x 8 Power–Switched and Reprogrammable PROM
cy7c276	16K x 16 Reprogrammable PROM
cy7c285	64K x 8 Reprogrammable Fast Column Access PROM
SRAMs	
cy7b195	64K x 4 Static R/W RAM with Output Enable
cy7c195	64K x 4 Static R/W RAM with Output Enable
cy7b199	32K x 8 Static RAM
cy7c199	32K x 8 Static RAM
DUAL–PORT RAMs	
cy7b134	4K x 8 Dual–Port Static RAM
cy7b138	4K x 8 Dual–Port Static RAM with Semaphores, INT, and BUSY
FIFOs	
cy7c401	64 x 4 Cascadeable FIFO
cy7c402	64 x 5 Cascadeable FIFO
cy7c403	64 x 4 Cascadeable FIFO with Output Enable
cy7c404	64 x 5 Cascadeable FIFO with Output Enable
cy7c429	2K x 9 High–Speed Cascadeable FIFO
PLDs	
palc22v10d	Flash Erasable, Reprogrammable CMOS PAL Device
CPLDs	
NONE	
FPGAs	
NONE	