

## Annex F<sup>1</sup>

### Features under consideration for removal

(informative)

The following features are being considered for removal from a future version of the language. Accordingly, modelers should refrain from using them when possible:

- Ports of mode **linkage** (1.1.1.2 and 4.3.2)
- Replacement characters (13.10)

To comment on these, or any other features of VHDL, please visit <http://vhdl.org/vasg/>.

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1. LCS 25. This annex is new with P1076-2000/D1. All annotations are elided.

