

ProASIC^{PLUS}[®]

Macro Library Guide

R1-2002



Actel Corporation, Sunnyvale, CA 94086

© 2002 Actel Corporation. All rights reserved.

Part Number: 5579016-1

Release: June 2002

No part of this document may be copied or reproduced in any form or by any means without prior written consent of Actel.

Actel makes no warranties with respect to this documentation and disclaims any implied warranties of merchantability or fitness for a particular purpose. Information in this document is subject to change without notice. Actel assumes no responsibility for any errors that may appear in this document.

This document contains confidential proprietary information that is not to be disclosed to any unauthorized person without prior written consent of Actel Corporation.

Trademarks

Actel is a trademark of Actel Corporation.

All other products or brand names mentioned are trademarks or registered trademarks of their respective holders.

Table of Contents

1 Combinational Cells

Naming Conventions for Combinational Cells.	7
Truth Table Symbol Descriptions.	7

Macros

AND2	9
AND2FT	9
AND3	10
AND3FFT.	10
AND3FTT	11
AO21.	11
AO21FTF	12
AO21FTT.	12
AO21TTF.	13
AOI21	13
AOI21FTF	14
AOI21FTT	14
AOI21TTF	15
BFR	15
BUBBLE	16
GND	16
INV	17
MUX2H	17
MUX2L	18
NAND2	18
NAND2FT	19
NAND3	19
NAND3FFT	20
NAND3FTT	20
NOR2	21
NOR2FT	21
NOR3	22
NOR3FFT.	22
NOR3FTT	23
NUBBLE	23
OA21.	24
OA21FTF	24
OA21FTT.	25
OA21TTF.	25
OAI21	26
OAI21FTF	26
OAI21FTT	27
OAI21TTF	27
OR2	28
OR2FT.	28
OR3	29
OR3FFT.	29
OR3FTT.	30
PWR	30
XNOR2	31
XNOR2FT	31
XOR2	32
XOR2FT.	32

2 Storage Cells

Naming Conventions for Flip-Flops	33
Naming Conventions for Latches	33
Truth Table Symbol Descriptions	34

Macros

DFF	35
DFFB	35
DFFBI	36
DFFC	36
DFFCI	37
DFFI	37
DFFL	38
DFFLB	38
DFFLBI	39
DFFLC	39
DFFLCI	40
DFFLI	40
DFFLS	41
DFFLSI	41
DFFS	42
DFFSI	42
LD	43
LDB	43
LDBI	44
LDC	44
LDCI	45
LDI	45
LDL	46
LDLB	46
LDLBI	47
LDLC	47
LDLCI	48
LDLI	48
LDLS	49
LDLSI	49
LDS	50
LDSI	50

3 Input/Output Cells

Input Buffers	51
Global Buffers	51
Output Buffers	52
Bidirectional Buffers	53
Truth Table Symbol Descriptions	54

Macros

GLx	55
GLxU	55
GLINT	56
GLIBx	56
GLIBxU	57
GLMIBx	58
GLMIBxU	59
GLMIBLx	60

GLMIBLxU	61
IBx	62
IBxU	62
IOB25x	63
IOB25xU	63
IOB25LPx	64
IOB25LPxU	64
IOB33x	65
IOB33xU	65
IOBL25x	66
IOBL25xU	66
IOBL25LPx	67
IOBL25LPxU	67
IOBL33x	68
IOBL33xU	68
OB25x	69
OB25LPx	69
OB33x	70
OTB25x	70
OTB25LPx	71
OTB33x	71
OTBL25x	72
OTBL25LPx	72
OTBL33x	73
GLMIOBx	74
GLMIOBLx	75
GLMXx	76
GLMXLx	77
GLPE	78
GLPEMIB	78

4 Memory Cells

Naming Convention for RAMs	79
Naming Convention for FIFOs	80

Macros

RAM256x9AA	83
RAM256x9AAP	83
RAM256x9ASR	84
RAM256x9ASRP	84
RAM256x9AST	85
RAM256x9ASTP	85
RAM256x9SA	86
RAM256x9SAP	86
RAM256x9SSR	87
RAM256x9SSRP	87
RAM256x9SST	88
RAM256x9SSTP	88
FIFO256x9AA	89
FIFO256x9AAP	89
FIFO256x9ASR	90
FIFO256x9ASRP	90
FIFO256x9AST	91
FIFO256x9ASTP	91
FIFO256x9SA	92

FIFO256x9SAP	92
FIFO256x9SSR	93
FIFO256x9SSRP	93
FIFO256x9SST	94
FIFO256x9SSTP	94
PLLCORE	95

A Product Support

Actel U.S. Toll-Free Line	97
Customer Service	97
Customer Applications Center	98
Guru Automated Technical Support	98
Web Site	98
FTP Site	99
Contacting the Customer Applications Center	99
Worldwide Sales Offices	100

Combinational Cells

The A500K and APA combinational cells implement all basic logic functions and have the following features:

- Inversion available on all inputs.
- Optimized for synthesis applications.

Naming Conventions for Combinational Cells

Names for combinational cells are composed of two parts:

- A name identifying the logic function (AND2, NOR3, XOR2, BFR, etc.).
- A 2- or 3-character code describing the pin inversions such as TFF. Capital T (true) indicates not inverted and capital F (false) indicates inverted. When no inputs are inverted, the inversion code is omitted.

Note: Not all combinations of inverted inputs are available. We have limited the number to avoid redundancy (e.g. AND2FF is logical equal to NOR2).

For Example:

AND2FT - The cell is a 2-input AND gate. The pin inversion code FT indicates that the A input pin is inverted, and the B input pin is not inverted.

AOI21FTF - The cell is a 3-input AND-OR-INVERT gate into a 2-input NOR gate. Pin A and C are inverted, pin B is not.

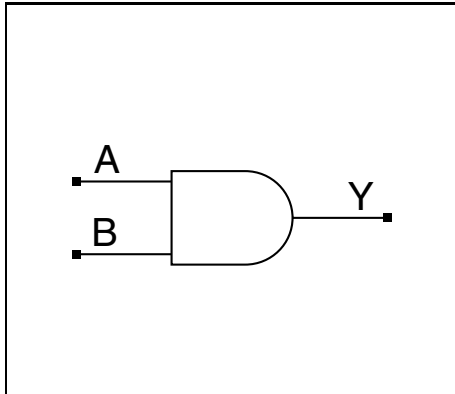
Truth Table Symbol Descriptions

Combinational truth tables use the following symbols:

- 1 - indicates logic level one.
- 0 - indicates logic level zero.
- X - indicates either logic level one or zero (don't care).

AND2

A500K, APA

**Function**

2 Input AND

Truth Table

A	B	Y
1	1	1
0	X	0
X	0	0

Tile Usage

Family	Tiles
All listed	1

Input

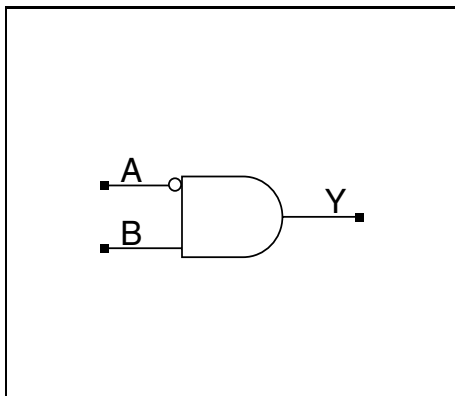
A, B

Output

Y

AND2FT

A500K, APA

**Function**

2 Input AND with Active Low A Input

Truth Table

A	B	Y
X	0	0
0	1	1
1	X	0

Tile Usage

Family	Tiles
All listed	1

Input

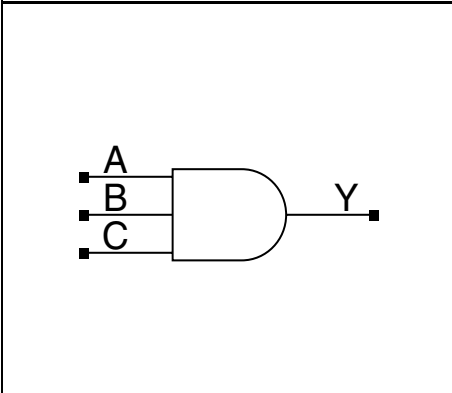
A, B

Output

Y

AND3

A500K, APA

**Function**

3 Input AND

Truth Table

A	B	C	Y
1	1	1	1
X	X	0	0
X	0	X	0
0	X	X	0

Tile Usage

Family	Tiles
All listed	1

Input

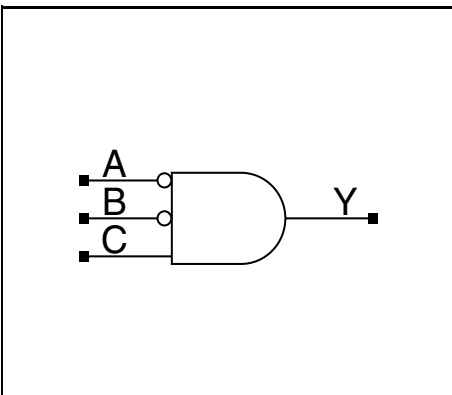
A, B, C

Output

Y

AND3FFT

A500K, APA

**Function**

3 Input AND with Active Low A and B Inputs

Truth Table

A	B	C	Y
X	X	0	0
0	0	1	1
X	1	X	0
1	X	X	0

Tile Usage

Family	Tiles
All listed	1

Input

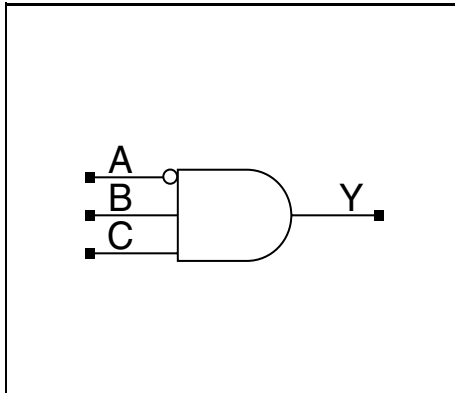
A, B, C

Output

Y

AND3FTT

A500K, APA

**Input**

A, B, C

Output

Y

Function

3 Input AND with Active Low A Input

Truth Table

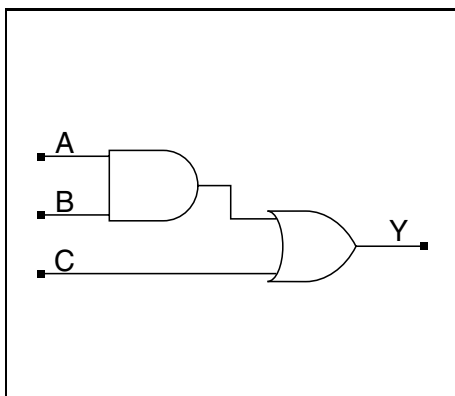
A	B	C	Y
X	X	0	0
X	0	X	0
0	1	1	1
1	X	X	0

Tile Usage

Family	Tiles
All listed	1

A021

A500K, APA

**Input**

A, B, C

Output

Y

Function

3 Input AND-OR

Truth Table

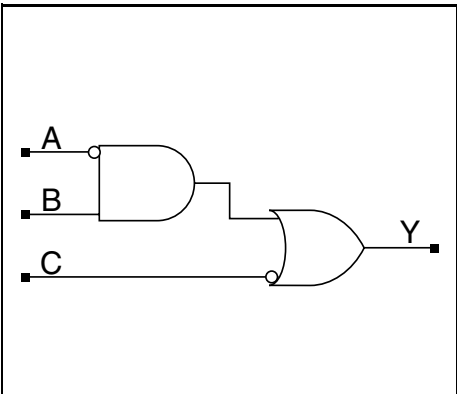
A	B	C	Y
0	X	0	0
X	0	0	0
X	X	1	1
1	1	X	1

Tile Usage

Family	Tiles
All listed	1

A021FF

A500K, APA

**Function**

3 Input AND-OR with Active Low A and C Inputs

Truth Table

A	B	C	Y
X	X	0	1
X	0	1	0
0	1	X	1
1	X	1	0

Tile Usage

Family	Tiles
All listed	1

Input

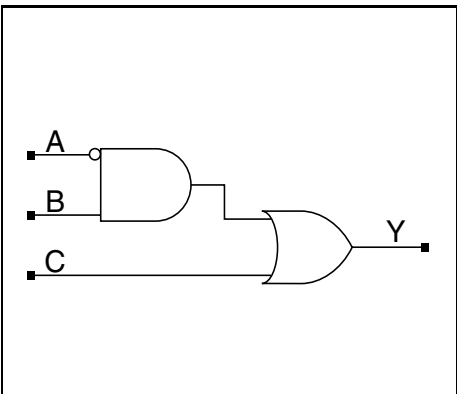
A, B, C

Output

Y

A021FT

A500K, APA

**Function**

3 Input AND-OR with Active Low A Input

Truth Table

A	B	C	Y
X	0	0	0
X	X	1	1
0	1	X	1
1	X	0	0

Tile Usage

Family	Tiles
All listed	1

Input

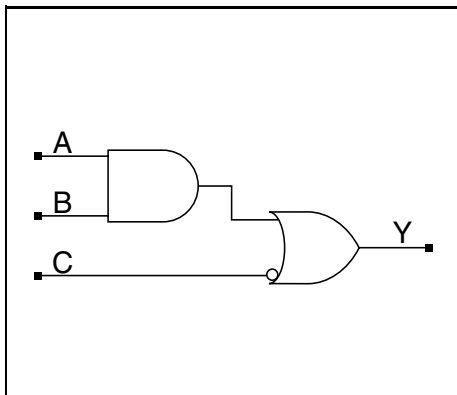
A, B, C

Output

Y

A021TTF

A500K, APA

**Input**

A, B, C

Output

Y

Function

3 Input AND-OR with Active Low C Input

Truth Table

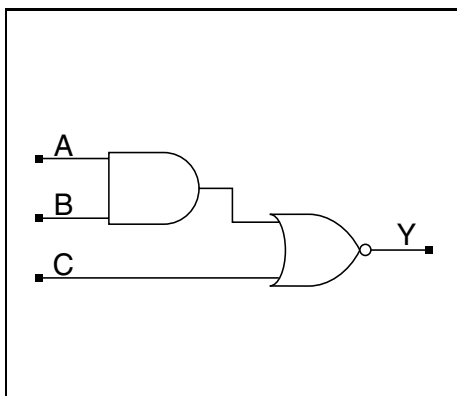
A	B	C	Y
X	X	0	1
X	0	1	0
0	X	1	0
1	1	X	1

Tile Usage

Family	Tiles
All listed	1

A0I21

A500K, APA

**Input**

A, B, C

Output

Y

Function

3 Input AND-OR-INVERT

Truth Table

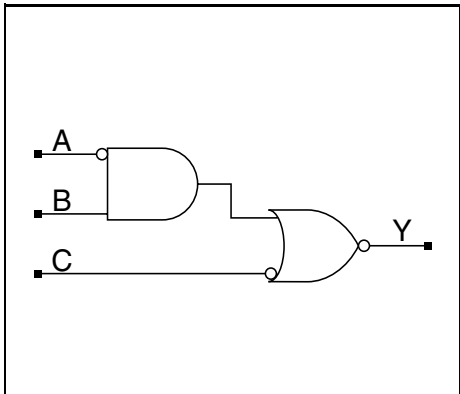
A	B	C	Y
0	X	0	1
X	0	0	1
X	X	1	0
1	1	X	0

Tile Usage

Family	Tiles
All listed	1

A0I21TF

A500K, APA

**Function**

3 Input AND-OR-INVERT with Active Low A and C Inputs

Truth Table

A	B	C	Y
X	X	0	0
X	0	1	1
0	1	X	0
1	X	1	1

Tile Usage

Family	Tiles
All listed	1

Input

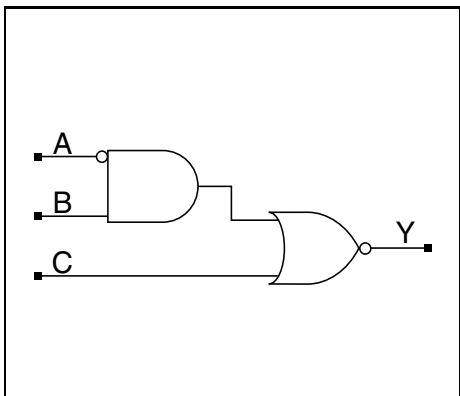
A, B, C

Output

Y

A0I21FT

A500K, APA

**Function**

3 Input AND-OR-INVERT with Active Low A Input

Truth Table

A	B	C	Y
X	0	0	1
X	X	1	0
0	1	X	0
1	X	0	1

Tile Usage

Family	Tiles
All listed	1

Input

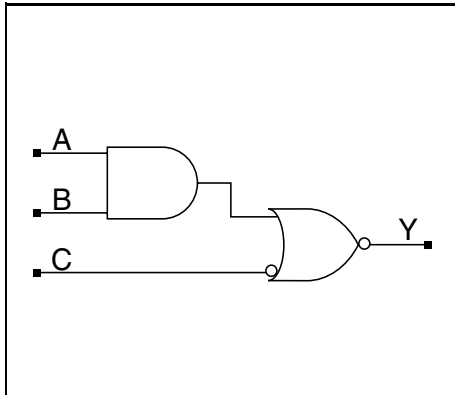
A, B, C

Output

Y

A0I21TTF

A500K, APA

**Input**

A, B, C

Output

Y

Function

3 Input AND-OR-INVERT with Active Low C Input

Truth Table

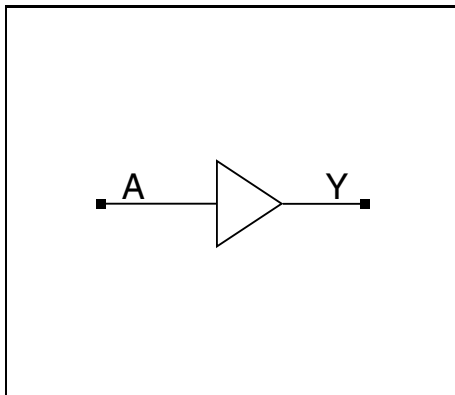
A	B	C	Y
X	X	0	0
X	0	1	1
0	X	1	1
1	1	X	0

Tile Usage

Family	Tiles
All listed	1

BFR

A500K, APA

**Input**

A

Output

Y

Function

Buffer

Truth Table

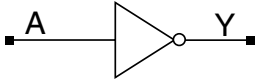
A	Y
0	0
1	1

Tile Usage

Family	Tiles
All listed	1

BUBBLE

A500K, APA

**Function**

Inverter (Only for internal embedded memory)

Truth Table

A	Y
0	1
1	0

Tile Usage

Family	Tiles
All listed	1

Input

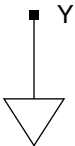
A

Output

Y

GND

A500K, APA

**Function**

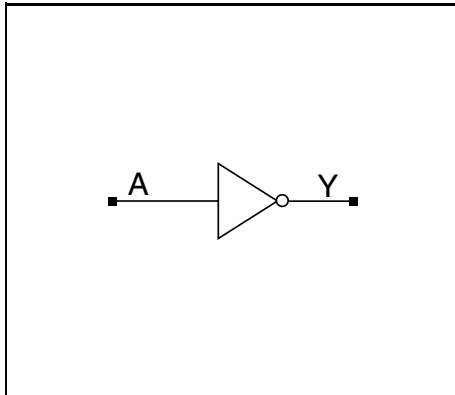
Ground

Input**Output**

Y

INV

A500K, APA

**Function**

Inverter

Truth Table

A	Y
0	1
1	0

Tile Usage

Family	Tiles
All listed	1

Input

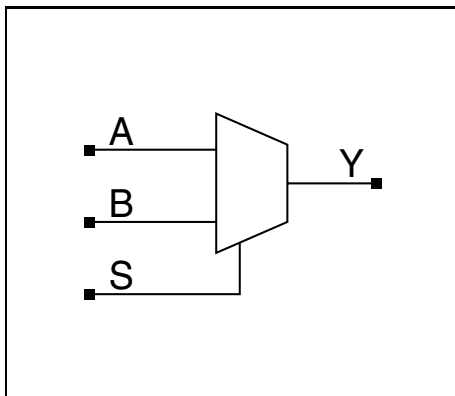
A

Output

Y

MUX2H

A500K, APA

**Function**

2 to 1 Multiplexer

Truth Table

S	Y
0	A
1	B

Tile Usage

Family	Tiles
All listed	1

Input

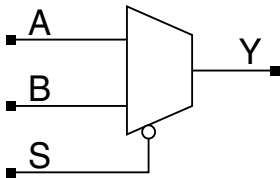
A, B, S

Output

Y

MUX2L

A500K, APA

**Function**

2 to 1 Multiplexer with Active Low Select

Truth Table

S	Y
0	B
1	A

Tile Usage

Family	Tiles
All listed	1

Input

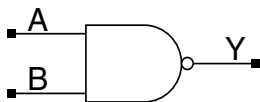
A, B, S

Output

Y

NAND2

A500K, APA

**Function**

2 Input NAND

Truth Table

A	B	Y
1	1	0
0	X	1
X	0	1

Tile Usage

Family	Tiles
All listed	1

Input

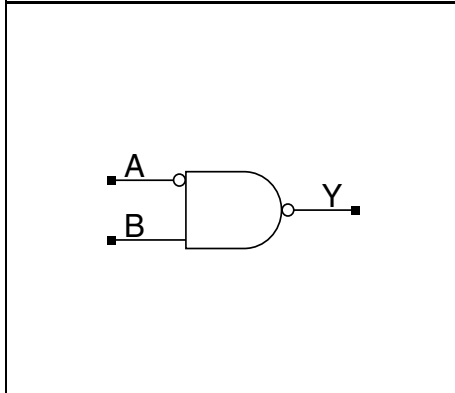
A, B

Output

Y

NAND2FT

A500K, APA

**Input**

A, B

Output

Y

Function

2 Input NAND with Active Low A Input

Truth Table

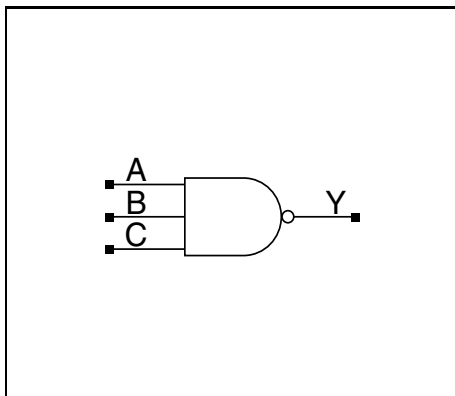
A	B	Y
1	X	1
0	1	0
X	0	1

Tile Usage

Family	Tiles
All listed	1

NAND3

A500K, APA

**Input**

A, B, C

Output

Y

Function

3 Input NAND

Truth Table

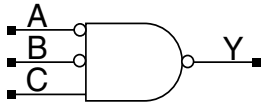
A	B	C	Y
1	1	1	0
0	X	X	1
X	X	0	1
X	0	X	1

Tile Usage

Family	Tiles
All listed	1

NAND3FTT

A500K, APA

**Function**

3 Input NAND with Active Low A and B Inputs

Truth Table

A	B	C	Y
X	X	0	1
0	0	1	0
X	1	X	1
1	X	X	1

Tile Usage

Family	Tiles
All listed	1

Input

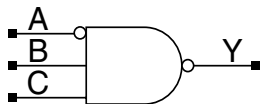
A, B, C

Output

Y

NAND3FTT

A500K, APA

**Function**

3 Input NAND with Active Low A Input

Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	1	1	0
1	X	X	1

Tile Usage

Family	Tiles
All listed	1

Input

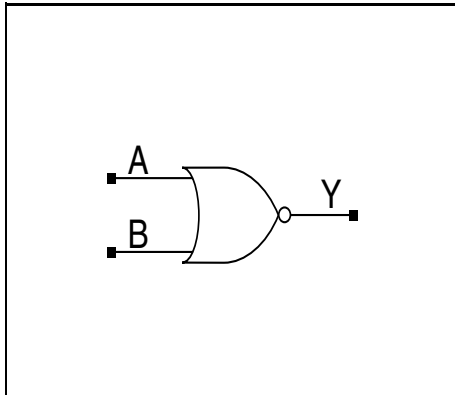
A, B, C

Output

Y

NOR2

A500K, APA

**Function**

2 Input NOR

Truth Table

A	B	Y
0	0	1
1	X	0
X	1	0

Tile Usage

Family	Tiles
All listed	1

Input

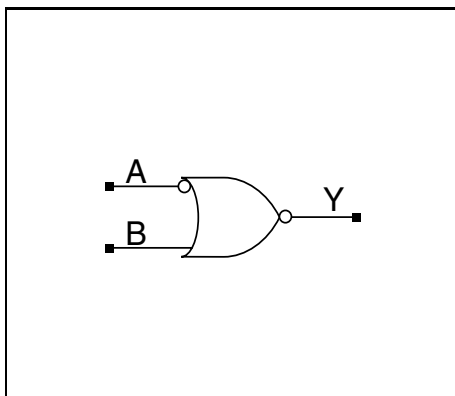
A, B

Output

Y

NOR2FT

A500K, APA

**Function**

2 Input NOR with Active Low A Input

Truth Table

A	B	Y
0	X	0
1	0	1
X	1	0

Tile Usage

Family	Tiles
All listed	1

Input

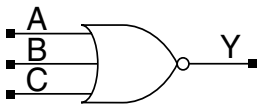
A, B

Output

Y

NOR3

A500K, APA

**Function**

3 Input NOR

Truth Table

A	B	C	Y
0	0	0	1
1	X	X	0
X	X	1	0
X	1	X	0

Tile Usage

Family	Tiles
All listed	1

Input

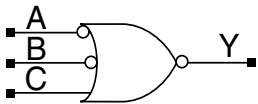
A, B, C

Output

Y

NOR3FFT

A500K, APA

**Function**

3 Input NOR with Active Low A and B Inputs

Truth Table

A	B	C	Y
X	0	X	0
0	X	X	0
1	1	0	1
X	X	1	0

Tile Usage

Family	Tiles
All listed	1

Input

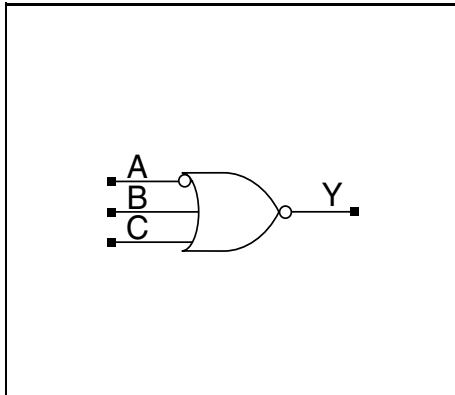
A, B, C

Output

Y

NOR3FTT

A500K, APA

**Input**

A, B, C

Output

Y

Function

3 Input NOR with Active Low A Input

Truth Table

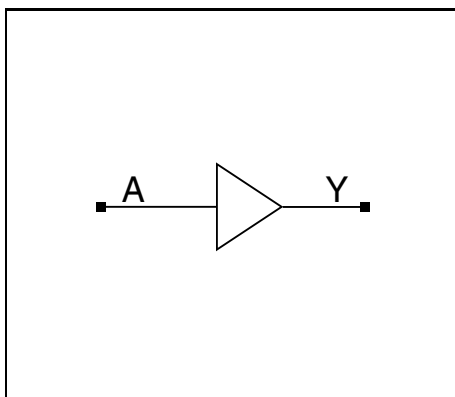
A	B	C	Y
0	X	X	0
1	0	0	1
X	X	1	0
X	1	X	0

Tile Usage

Family	Tiles
All listed	1

NUBBLE

A500K, APA

**Input**

A

Output

Y

Function

Buffer (Only for internal embedded memory)

Truth Table

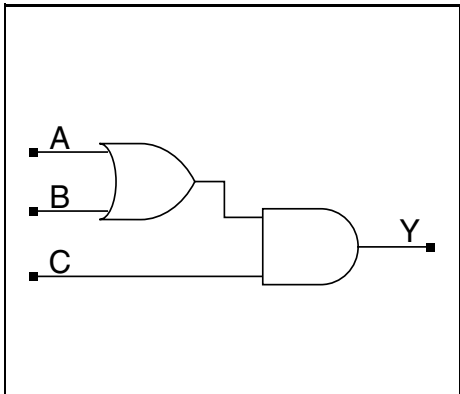
A	Y
0	0
1	1

Tile Usage

Family	Tiles
All listed	1

OA21

A500K, APA

**Function**

3 Input OR-AND

Truth Table

A	B	C	Y
1	X	1	1
X	1	1	1
X	X	0	0
0	0	X	0

Tile Usage

Family	Tiles
All listed	1

Input

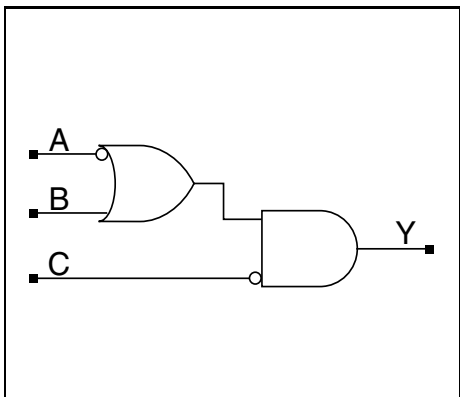
A, B, C

Output

Y

OA21FF

A500K, APA

**Function**

3 Input OR-AND with Active Low A and C Inputs

Truth Table

A	B	C	Y
0	X	0	1
X	X	1	0
1	0	X	0
X	1	0	1

Tile Usage

Family	Tiles
All listed	1

Input

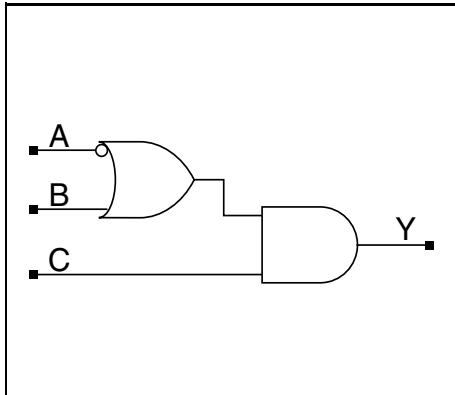
A, B, C

Output

Y

OA21FT

A500K, APA

**Input**

A, B, C

Output

Y

Function

3 Input OR-AND with Active Low A Input

Truth Table

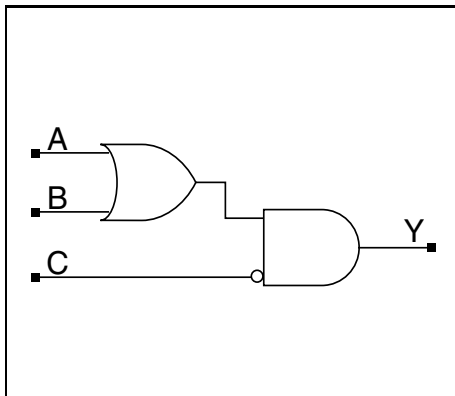
A	B	C	Y
X	X	0	0
0	X	1	1
1	0	X	0
X	1	1	1

Tile Usage

Family	Tiles
All listed	1

OA21TF

A500K, APA

**Input**

A, B, C

Output

Y

Function

3 Input OR-AND with Active Low C Input

Truth Table

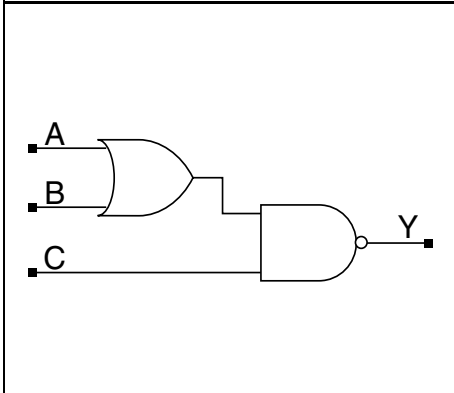
A	B	C	Y
0	0	X	0
X	1	0	1
X	X	1	0
1	X	0	1

Tile Usage

Family	Tiles
All listed	1

OAI21

A500K, APA

**Function**

3 Input OR-NAND

Truth Table

A	B	C	Y
1	X	1	0
X	1	1	0
X	X	0	1
0	0	X	1

Tile Usage

Family	Tiles
All listed	1

Input

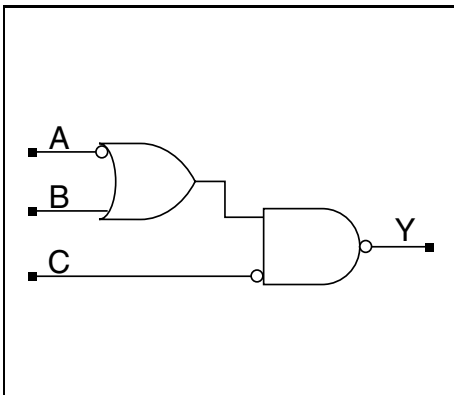
A, B, C

Output

Y

OAI21FTF

A500K, APA

**Function**

3 Input OR-NAND with Active Low A and C Inputs

Truth Table

A	B	C	Y
0	X	0	0
X	X	1	1
1	0	X	1
X	1	0	0

Tile Usage

Family	Tiles
All listed	1

Input

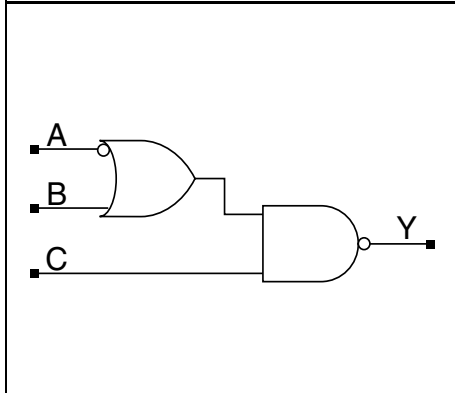
A, B, C

Output

Y

OAI21FTT

A500K, APA

**Input**

A, B, C

Output

Y

Function

3 Input OR-NAND with Active Low A Input

Truth Table

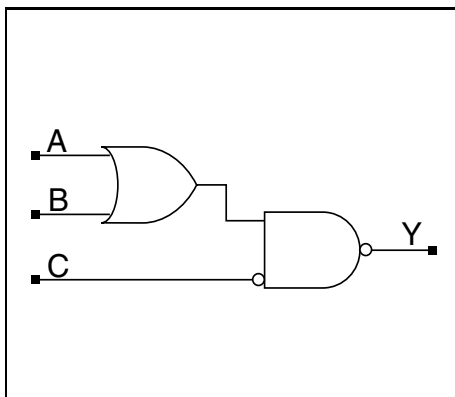
A	B	C	Y
X	X	0	1
0	X	1	0
1	0	X	1
X	1	1	0

Tile Usage

Family	Tiles
All listed	1

OAI21TTF

A500K, APA

**Input**

A, B, C

Output

Y

Function

3 Input OR-NAND with Active Low C Input

Truth Table

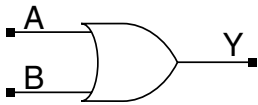
A	B	C	Y
0	0	X	1
X	1	0	0
X	X	1	1
1	X	0	0

Tile Usage

Family	Tiles
All listed	1

OR2

A500K, APA

**Function**

2 Input OR

Truth Table

A	B	Y
1	X	1
X	1	1
0	0	0

Tile Usage

Family	Tiles
All listed	1

Input

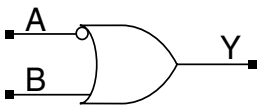
A, B

Output

Y

OR2FT

A500K, APA

**Function**

2 Input OR with Active Low A Input

Truth Table

A	B	Y
0	X	1
1	0	0
X	1	1

Tile Usage

Family	Tiles
All listed	1

Input

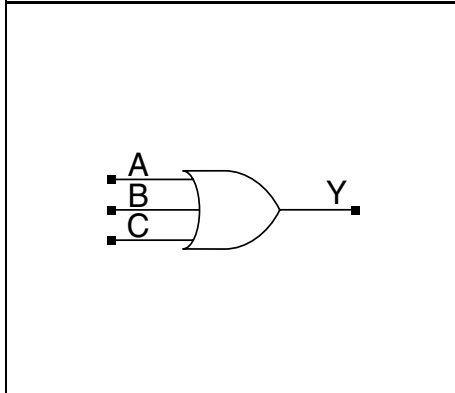
A, B

Output

Y

OR3

A500K, APA

**Input**

A, B, C

Output

Y

Function

3 Input OR

Truth Table

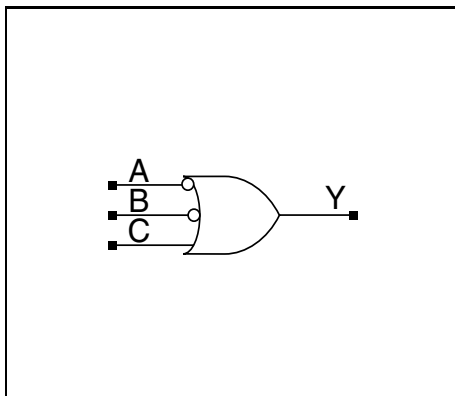
A	B	C	Y
1	X	X	1
X	1	X	1
X	X	1	1
0	0	0	0

Tile Usage

Family	Tiles
All listed	1

OR3FFT

A500K, APA

**Input**

A, B, C

Output

Y

Function

3 Input OR with Active Low A and B Inputs

Truth Table

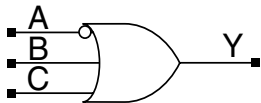
A	B	C	Y
X	0	X	1
0	X	X	1
1	1	0	0
X	X	1	1

Tile Usage

Family	Tiles
All listed	1

OR3FTT

A500K, APA

**Function**

3 Input OR with Active Low A Input

Truth Table

A	B	C	Y
0	X	X	1
1	0	0	0
X	X	1	1
X	1	X	1

Tile Usage

Family	Tiles
All listed	1

Input

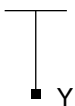
A, B, C

Output

Y

PWR

A500K, APA

**Function**

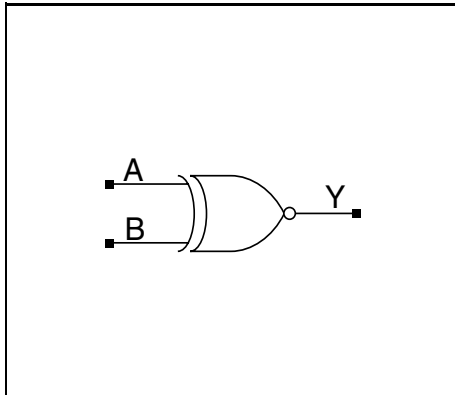
Power

Input**Output**

Y

XNOR2

A500K, APA

**Input**

A, B

Output

Y

Function

2 Input Exclusive NOR

Truth Table

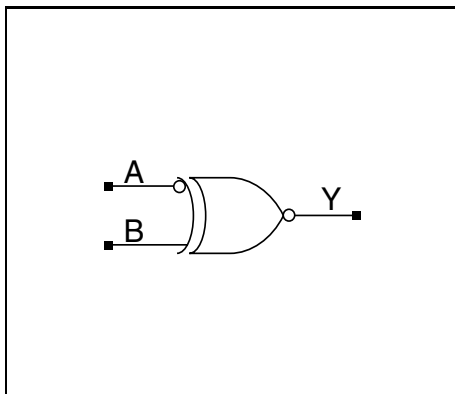
A	B	Y
0	0	1
1	1	1
1	0	0
0	1	0

Tile Usage

Family	Tiles
All listed	1

XNOR2FT

A500K, APA

**Input**

A, B

Output

Y

Function

2 Input Exclusive NOR with Active Low A Input

Truth Table

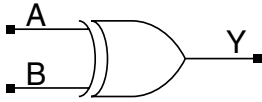
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Tile Usage

Family	Tiles
All listed	1

XOR2

A500K, APA

**Function**

2 Input Exclusive OR

Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Tile Usage

Family	Tiles
All listed	1

Input

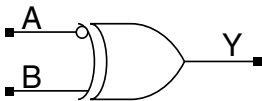
A, B

Output

Y

XOR2FT

A500K, APA

**Function**

2 Input Exclusive OR with Active Low A Input

Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Tile Usage

Family	Tiles
All listed	1

Input

A, B

Output

Y

Storage Cells

The A500K storage cells implement transparent latch and D-type flip-flop functions and have the following features:

- Inversion available on Enable pin on all latches.
- Optimized for synthesis flows.
- Asynchronous CLR and SET pins.

Naming Conventions for Flip-Flops

Names for the flip-flop cells are composed of four parts:

- A base name identifying the cell as a D-type flip-flop (DFF).
- An optional 1-character code describing the clock pin. L indicates negative edge triggered. No code indicates positive edge triggered.
- Asynchronous input type and polarity: an optional 1-character code designating the control pins as follows:

B = Active high, **both** set and clear

C = Active high **clear**

S = Active high **set**

When omitted, the cell has neither SET nor CLEAR input.

- An optional 1-character code describing the output. I indicates output is inverted. No code indicates output is not inverted.

For Example:

DFFC - The cell is a positive edge triggered D-type flip-flop with active high CLEAR.

DFFLB - The cell is a negative edge triggered D-type flip-flop with active high SET and CLEAR.

Naming Conventions for Latches

Names for the latch cells are composed of four parts:

- A name identifying the logic function as a latch (LD).
- An optional 1-character code describing the Enable pin. L indicates active low. No code indicates active high.

- Asynchronous input type: an optional 1-character code designating the control pins as follows:
 - B = Active high, **both** set and clear
 - C = Active high **clear**
 - S = Active high **set**
- When the latch has neither SET nor CLEAR pins, this code is omitted.
- An optional 1-character code describing the output polarity. I indicates output is inverted. No code indicates output is not inverted.

For Example:

LDL - The cell is a transparent latch with active low enable and neither SET nor CLEAR pins.

LDLSI - The cell is a transparent latch with active low enable, active high SET pin and inverted output pin named QBAR.

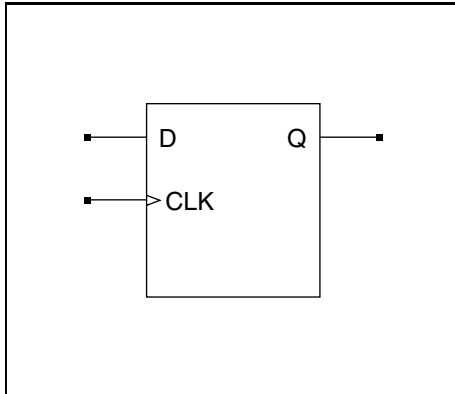
Truth Table Symbol Descriptions

Combinational truth tables use the following symbols:

- 1 - indicates logic level one.
- 0 - indicates logic level zero.
- \uparrow - indicates positive (rising) edge.
- \downarrow - indicates negative (falling) edge.
- D - indicates input port.
- !D - indicates inverted input port.
- Q - indicates output port.
- QBAR - indicates inverted output port.
- X - indicates either logic level one or zero (don't care).

DFF

A500K, APA

**Input**

D, CLK

Output

Q

Function

Positive Edge Triggered D-Type Flip-Flop

Truth Table

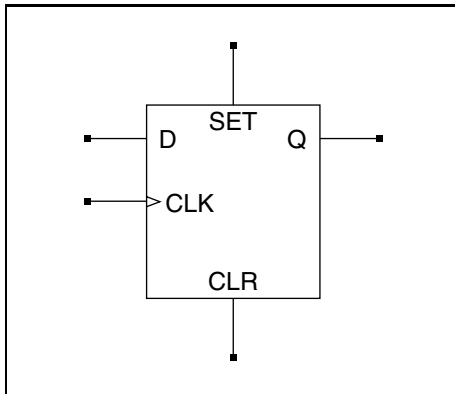
CLK	Q_{n+1}
↑	D

Tile Usage

Family	Tiles
All listed	1

DFFB

A500K, APA

**Input**

CLR, SET, CLK, D

Output

Q

Function

Positive Edge Triggered D-Type Flip-Flop with Active High Set and Clear

Truth Table

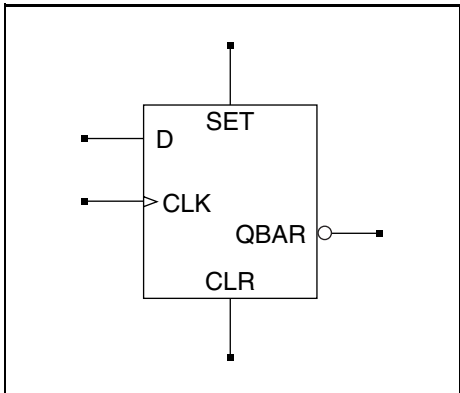
CLK	SET	CLR	Q_{n+1}
X	1	0	1
X	X	1	0
↑	0	0	D

Tile Usage

Family	Tiles
All listed	4

DFFBI

A500K, APA

**Function**

Positive Edge Triggered D-Type Flip-Flop with Active High Set and Clear and Active Low Output

Truth Table

CLK	SET	CLR	QBAR _{n+1}
X	1	0	1
X	X	1	0
↑	0	0	!D

Tile Usage

Family	Tiles
All listed	4

Input

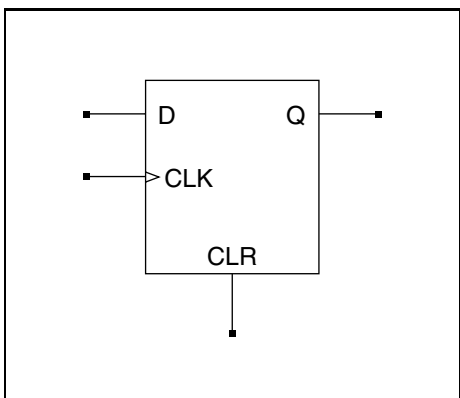
CLR, SET, CLK, D

Output

QBAR

DFFC

A500K, APA

**Function**

Positive Edge Triggered D-Type Flip-Flop with Active High Clear

Truth Table

CLK	CLR	Q _{n+1}
X	1	0
↑	0	D

Tile Usage

Family	Tiles
All listed	1

Input

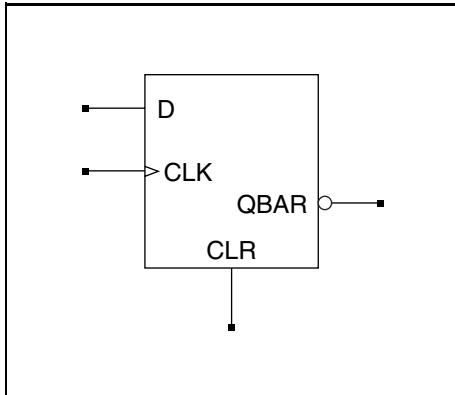
CLR, CLK, D

Output

Q

DFFCI

A500K, APA

**Function**

Positive Edge Triggered D-Type Flip-Flop with Active High Clear and Active Low Output

Truth Table

CLK	CLR	QBAR _{n+1}
X	1	1
↑	0	!D

Tile Usage

Family	Tiles
All listed	1

Input

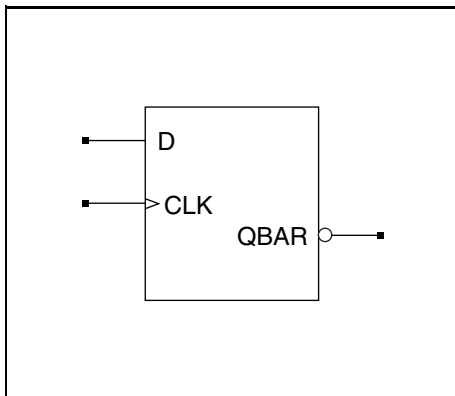
CLR, CLK, D

Output

QBAR

DFFI

A500K, APA

**Function**

Positive Edge Triggered D-Type Flip-Flop with Active Low Output

Truth Table

CLK	QBAR _{n+1}
↑	!D

Tile Usage

Family	Tiles
All listed	1

Input

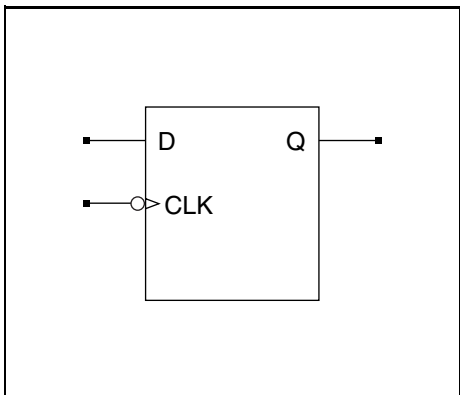
CLK, D

Output

QBAR

DFFL

A500K, APA

**Function**

Negative Edge Triggered D-Type Flip-Flop

Truth Table

CLK	Q_{n+1}
↓	D

Tile Usage

Family	Tiles
All listed	1

Input

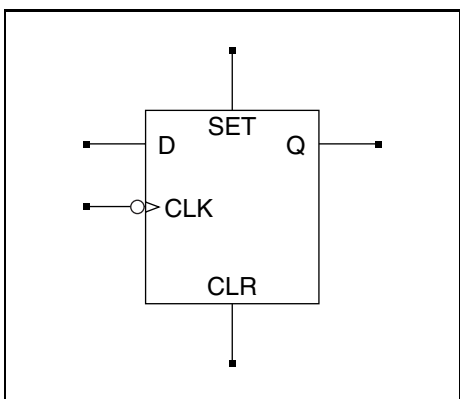
CLK, D

Output

Q

DFFLB

A500K, APA

**Function**

Negative Edge Triggered D-Type Flip-Flop with Active High Set and Clear

Truth Table

CLK	SET	CLR	Q_{n+1}
X	1	0	1
X	X	1	0
↓	0	0	D

Tile Usage

Family	Tiles
All listed	4

Input

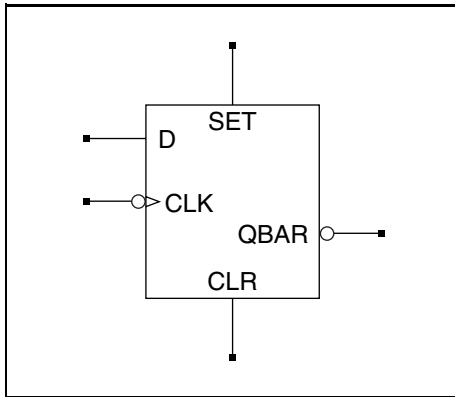
CLR, SET, CLK, D

Output

Q

DFFLBI

A500K, APA

**Input**

CLR, SET, CLK, D

Output

QBAR

Function

Negative Edge Triggered D-Type Flip-Flop with Active High Set and Clear and Active Low Output

Truth Table

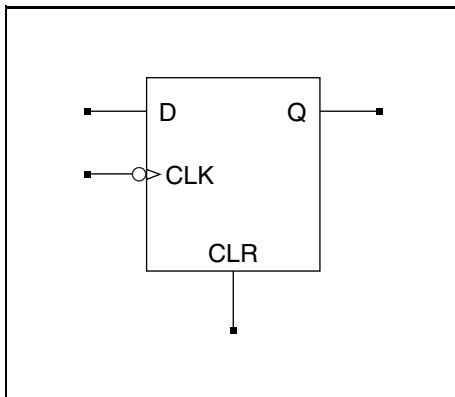
CLK	SET	CLR	QBAR _{n+1}
X	1	0	0
X	X	1	1
↓	0	0	!D

Tile Usage

Family	Tiles
All listed	4

DFFLC

A500K, APA

**Input**

CLR, CLK, D

Output

Q

Function

Negative Edge Triggered D-Type Flip-Flop with Active High Clear

Truth Table

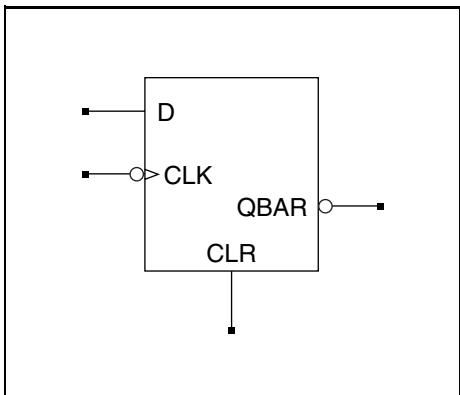
CLK	CLR	Q _{n+1}
X	1	0
↓	0	D

Tile Usage

Family	Tiles
All listed	1

DFFLCI

A500K, APA

**Function**

Negative Edge Triggered D-Type Flip-Flop with Active High Clear and Active Low Output

Truth Table

CLK	CLR	QBAR _{n+1}
X	1	1
↓	0	!D

Tile Usage

Family	Tiles
All listed	1

Input

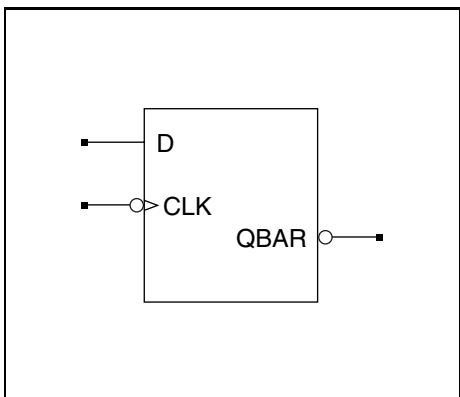
CLR, CLK, D

Output

QBAR

DFFLI

A500K, APA

**Function**

Negative Edge Triggered D-Type Flip-Flop with Active Low Output

Truth Table

CLK	QBAR _{n+1}
↓	!D

Tile Usage

Family	Tiles
All listed	1

Input

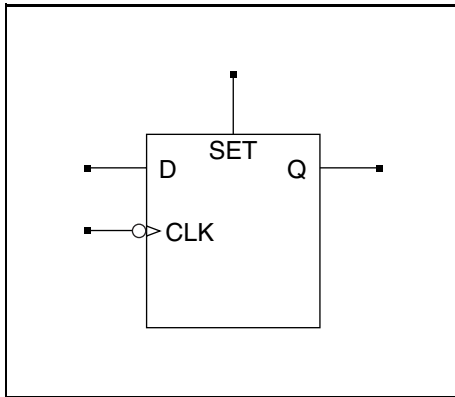
CLK, D

Output

QBAR

DFFLS

A500K, APA

**Input**

SET, CLK, D

Output

Q

Function

Negative Edge Triggered D-Type Flip-Flop with Active High Set

Truth Table

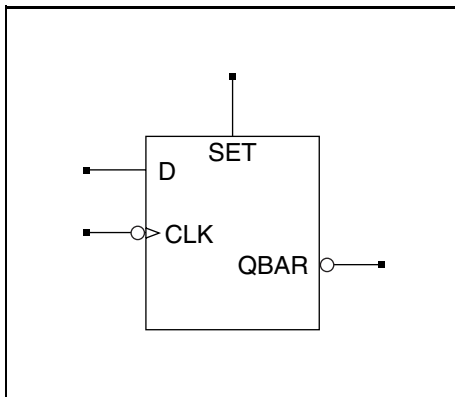
CLK	SET	Q_{n+1}
X	1	1
↓	0	D

Tile Usage

Family	Tiles
All listed	1

DFFLSI

A500K, APA

**Input**

SET, CLK, D

Output

QBAR

Function

Negative Edge Triggered D-Type Flip-Flop with Active High Set and Active Low Output

Truth Table

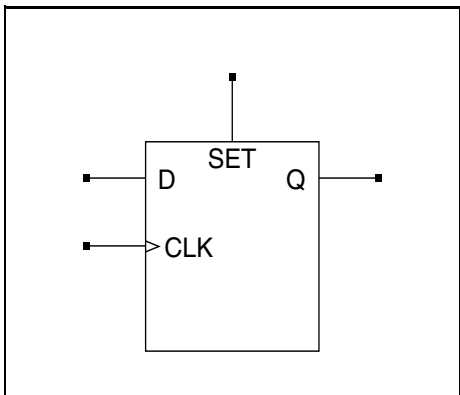
CLK	SET	$QBAR_{n+1}$
X	1	0
↓	0	!D

Tile Usage

Family	Tiles
All listed	1

DFFS

A500K, APA

**Function**

Positive Edge Triggered D-Type Flip-Flop with Active High Set

Truth Table

CLK	SET	Q_{n+1}
X	1	1
↑	0	D

Tile Usage

Family	Tiles
All listed	1

Input

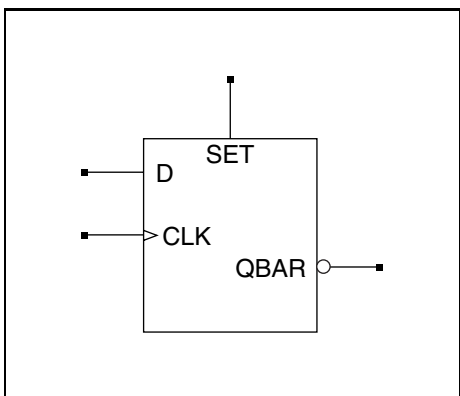
SET, CLK, D

Output

Q

DFFSI

A500K, APA

**Function**

Positive Edge Triggered D-Type Flip-Flop with Active High Set and Active Low Output

Truth Table

CLK	SET	$QBAR_{n+1}$
X	1	0
↑	0	!D

Tile Usage

Family	Tiles
All listed	1

Input

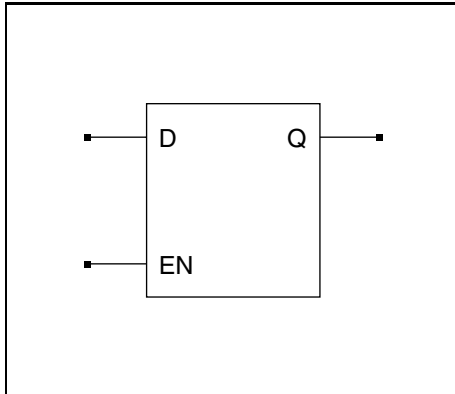
SET, CLK, D

Output

QBAR

LD

A500K, APA

**Function**

Active High Latch

Truth Table

EN	Q_{n+1}
0	Q
1	D

Tile Usage

Family	Tiles
All listed	1

Input

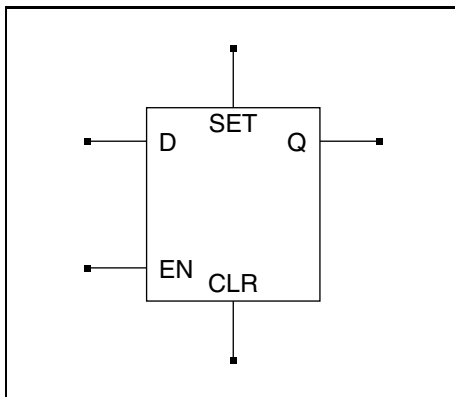
EN, D

Output

Q

LDB

A500K, APA

**Function**

Active High Latch with Active High Set and Clear

Truth Table

EN	SET	CLR	Q_{n+1}
X	1	0	1
X	X	1	0
1	0	0	D
0	0	0	Q

Tile Usage

Family	Tiles
All listed	2

Input

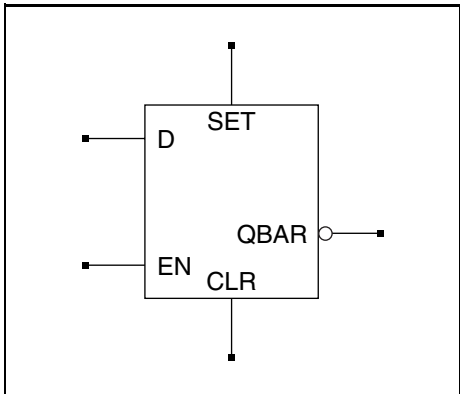
CLR, SET, EN, D

Output

Q

LDBI

A500K, APA

**Function**

Active High Latch with Active High Set and Clear and Active Low Output

Truth Table

EN	SET	CLR	QBAR _{n+1}
X	1	0	0
X	X	1	1
1	0	0	!D
0	0	0	QBAR

Tile Usage

Family	Tiles
All listed	2

Input

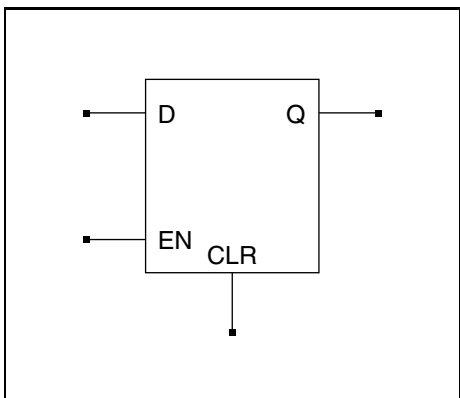
CLR, SET, EN, D

Output

QBAR

LDC

A500K, APA

**Function**

Active High Latch with Active High Clear

Truth Table

EN	CLR	Q _{n+1}
X	1	0
1	0	D
0	0	Q

Tile Usage

Family	Tiles
All listed	1

Input

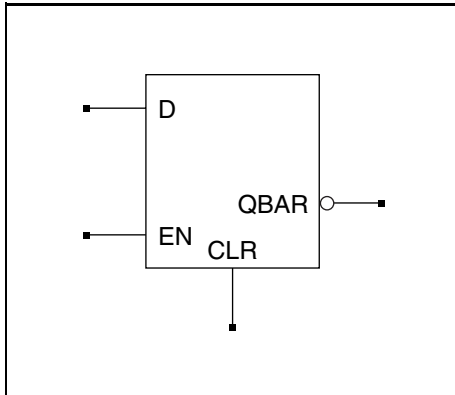
CLR, EN, D

Output

Q

LDCI

A500K, APA

**Input**

CLR, EN, D

Output

QBAR

Function

Active High Latch with Active High Clear and Active Low Output

Truth Table

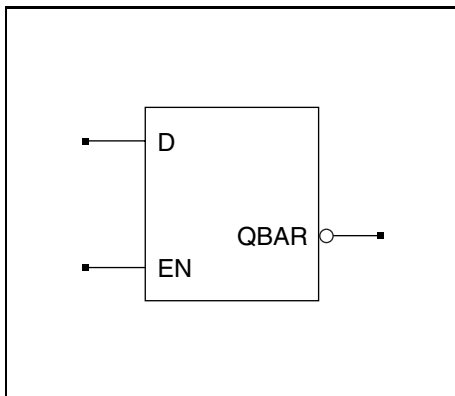
EN	CLR	QBAR _{n+1}
X	1	1
1	0	!D
0	0	QBAR

Tile Usage

Family	Tiles
All listed	1

LDI

A500K, APA

**Input**

EN, D

Output

QBAR

Function

Active High Latch with Active Low Output

Truth Table

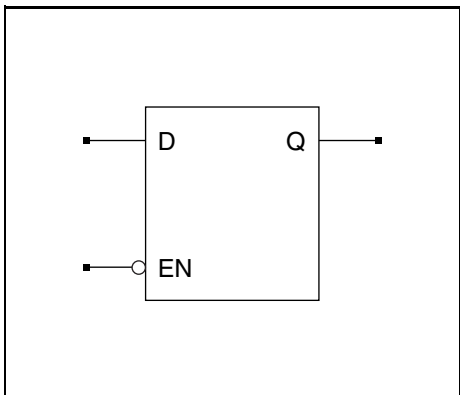
EN	QBAR _{n+1}
0	QBAR
1	!D

Tile Usage

Family	Tiles
All listed	1

LDL

A500K, APA

**Function**

Active Low Latch

Truth Table

EN	Q_{n+1}
0	D
1	Q

Tile Usage

Family	Tiles
All listed	1

Input

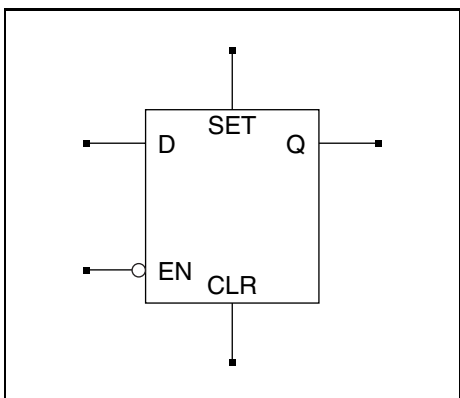
EN, D

Output

Q

LDLB

A500K, APA

**Function**

Active Low Latch with Active High Set and Clear

Truth Table

EN	SET	CLR	Q_{n+1}
X	1	0	1
X	X	1	0
0	0	0	D
1	0	0	Q

Tile Usage

Family	Tiles
All listed	2

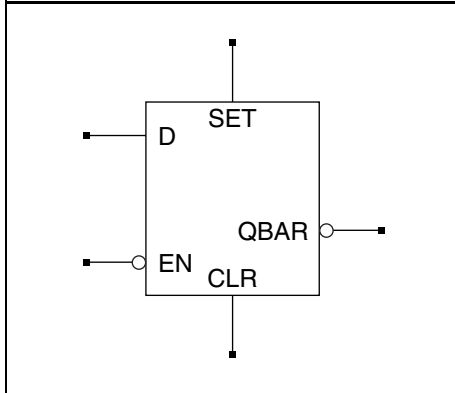
Input

CLR, SET, EN, D

Output

Q

LDLBI



Input

CLR, SET, EN, D

Output

QBAR

Function

Active Low Latch with Active High Set and Clear and Active Low Output

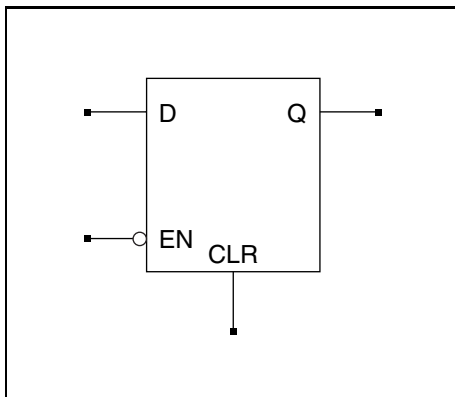
Truth Table

EN	SET	CLR	QBAR _{n+1}
X	1	0	0
X	X	1	1
0	0	0	!D
1	0	0	QBAR

Tile Usage

Family	Tiles
All listed	2

LDLC



Input

CLR, EN, D

Output

Q

Function

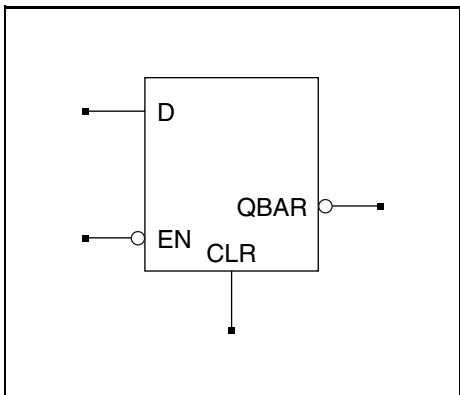
Active Low Latch with Active High Clear

Truth Table

EN	CLR	Q _{n+1}
X	1	0
0	0	D
1	0	Q

LDLCI

A500K, APA

**Function**

Active Low Latch with Active High Clear and Active Low Output

Truth Table

EN	CLR	QBAR _{n+1}
X	1	1
0	0	!D
1	0	QBAR

Tile Usage

Family	Tiles
All listed	1

Input

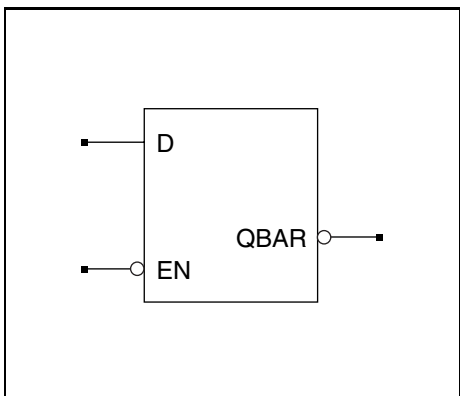
CLR, EN, D

Output

QBAR

LDLI

A500K, APA

**Function**

Active Low Latch with Active Low Output

Truth Table

EN	QBAR _{n+1}
0	!D
1	QBAR

Tile Usage

Family	Tiles
All listed	1

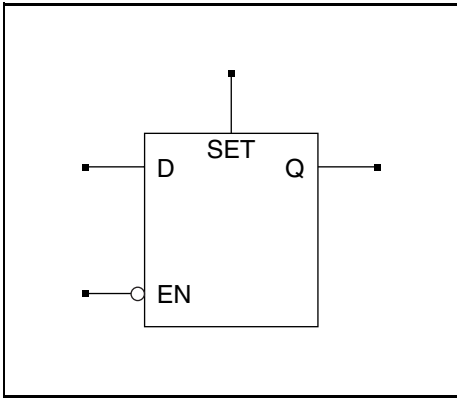
Input

EN, D

Output

QBAR

LDLS **A500K, APA**



Function
Active Low Latch with Active High Set

Truth Table

EN	SET	Q _{n+1}
X	1	1
0	0	D
1	0	Q

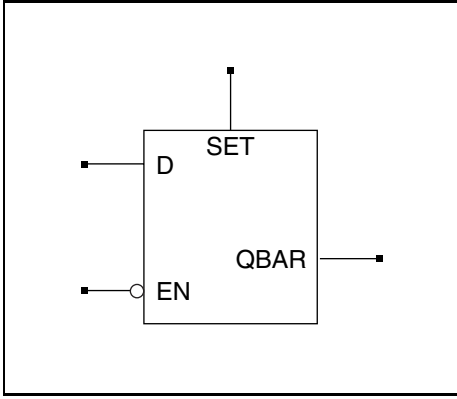
Tile Usage

Family	Tiles
All listed	1

Input
SET, EN, D

Output
Q

LDLSI **A500K, APA**



Function
Active Low Latch with Active High Set and Active Low Output

Truth Table

EN	SET	QBAR _{n+1}
X	1	0
0	0	!D
1	0	QBAR

Tile Usage

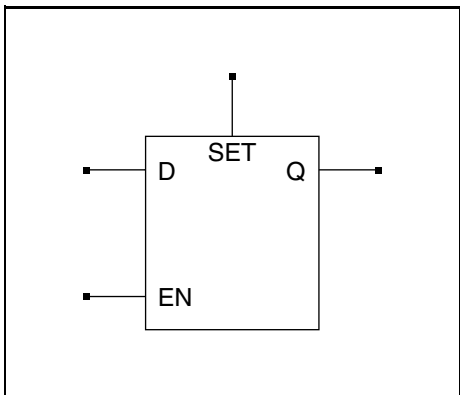
Family	Tiles
All listed	1

Input
SET, EN, D

Output
QBAR

LDS

A500K, APA

**Function**

Active High Latch with Active High Set

Truth Table

EN	SET	Q_{n+1}
X	1	1
0	0	Q
1	0	D

Tile Usage

Family	Tiles
All listed	1

Input

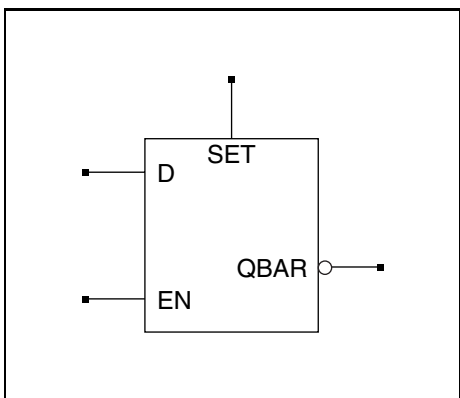
SET, EN, D

Output

Q

LDSI

A500K, APA

**Function**

Active High Latch with Active High Set and Active Low Output

Truth Table

EN	SET	$QBAR_{n+1}$
X	1	0
0	0	QBAR
1	0	!D

Tile Usage

Family	Tiles
All listed	1

Input

SET, EN, D

Output

QBAR

Input/Output Cells

This section describes input buffers, global buffers, output buffers and bidirectional buffers.

Input Buffers

A500K input buffers have the following features:

- CMOS voltage levels for 2.5 V and 3.3 V.
- Optional pull-up resistor.
- ESD protection circuitry.
- Latch-up protection circuitry.

Input Buffer Naming Conventions

Names for the input buffers are composed of up to 4 parts:

- A base name indicating the type of input buffer (IB for input with positive pad logic, IBN with negative pad logic).
- The number code 25 or 33 indicating a 2.5 or 3.3 voltage level.
- A two character code indicating low power pad voltage (LP).
- An optional one character code (U) designating a pull-up resistor. When the buffer has no resistor, this code is omitted.

For Example:

IB25 - An input buffer with 2.5 CMOS voltage levels and no pull-up resistor.

IB33U - An input buffer with 3.3 CMOS voltage levels and pull-up resistor.

Global Buffers

Global buffers are provided for use with low skew, high fanout nets, such as, clock and reset. They can be either driven from a pad or internally. If a global buffer is used internally, the pad can be used for other input signals.

A500K global buffers have the following features:

- 2.5 or 3.3 CMOS voltage levels.
- Optional pull-up resistor.
- ESD protection circuitry.

- Latch-up protection circuitry.
- Multiplexed input for external or internal drive.

Global Buffer Naming Conventions

Four types of global buffers are available: standard global input buffers (GL), global buffers with independent input buffers (GLIB), global multiplexed input buffers (GLMIB) and global buffers with internal connection only (GLINT).

Global buffer names are composed of up to four parts:

- The name base indicating the type of buffer (GL, GLIB, GLMIB for external buffers, GLINT for an internal connected global buffer).
- The number code 25 or 33 indicating a 2.5 or 3.3 voltage level.
- A two character code indicating low power pad voltage (LP).
- An optional one character code (U) designating a pull-up resistor (except GLINT). When there is no resistor, this code is omitted.

For Example:

GL25U - Global input buffer with 2.5 CMOS voltage levels and pull-up resistor.

GLIB33 - Global buffer with 3.3 CMOS voltage levels input buffer and global buffer with input A.

GLMIBL33U - Global multiplexed input buffer with 3.3 CMOS voltage levels, active low enable and pull-up resistor.

Output Buffers

A500K output buffers have the following features:

- Optional PCI compliance with PCI 2.1 Component Specification (3.3 Voltage pad only).
- Selectable drive strengths.
- Selectable slew rates.
- Optional three-state functionality.
- ESD protection circuitry.
- Latch-up protection circuitry.

Output Buffer Naming Conventions

Names for the output buffers are composed of up to five parts:

- The name base indicating the type of output buffer (OB for output buffer, OTB for three-state output buffer).
- An optional one character code (L) designating an active low enable input for the OTB output buffer. The code is omitted for the active high enable input.
- The number code 25 or 33 indicating a 2.5 or 3.3 voltage level.

- A code indicating the drive strength (2.5 Volt pad: L for 1 mA, H for 3.5 mA; 3.3 Volt pad: L for 5 mA and P for PCI compliant 10 mA).
- A one character code indicating the slew rate (L for low 25 mA/ns, N for nominal 50 mA/ns, and H for high 100 mA/ns).

For Example:

OB25HN - 2.5 Volt output buffer, high drive strengths and nominal slew rate.

OTB33LH - Three-state output buffer, low drive strengths, high slew rate.

OB33PL - PCI compliant output buffer (= high drive strengths) and low slew rate.

Bidirectional Buffers

A500K bidirectional buffers have all the features of both the input buffers and the output buffers:

- 2.5 and 3.3 CMOS input voltage levels.
- Optional pull-up resistor.
- Optional PCI compliance with PCI 2.1 Component Specification (3.3 Voltage pad only).
- Selectable drive strengths.
- Selectable slew rates.
- Three-state functionality.
- ESD protection circuitry.
- Latch-up protection circuitry.

Bidirectional Buffer Naming Conventions

Names for the bidirectional buffers are composed of up to seven parts:

- The name base IOB identifying the buffer as a bidirectional buffer.
- An optional one character code (L) designating an active low enable input for the IOB output buffer part. The code is omitted for the active high enable input.
- The number code 25 or 33 indicating a 2.5 or 3.3 voltage level.
- A two character code indicating low power pad voltage (LP).
- A code indicating the drive strength (2.5 Volt pad: L for 1 mA, H for 3.5 mA; 3.3 Volt pad: L for 5 mA and P for PCI compliant 10 mA).
- A one character code indicating the slew rate (L for low 25 mA/ns, N for nominal 50 mA/ns, and H for high 100 mA/ns).
- An optional one character code (U) designating a pull-up resistor. When there is no resistor, this code is omitted.

For Example:

IOB25LLU - A 2.5 Volt bidirectional buffer with low drive strength, low slew rate and a pull-up resistor.

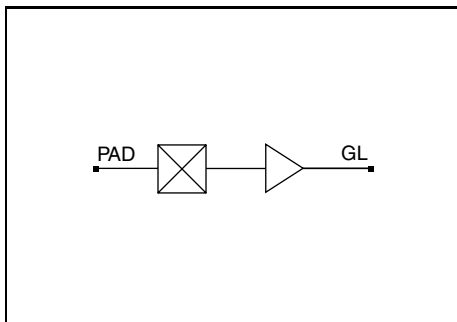
IOB33PHU - A 3.3 Volt PCI compliant bidirectional buffer with high slew rate and a pull-up resistor.

IOBL33LN - A 3.3 Volt bidirectional buffer with active low enable input, low drive strength and normal slew rate.

Truth Table Symbol Descriptions

Combinational truth tables use the following symbols:

- 1 - indicates logic level one.
- 0 - indicates logic level zero.
- A - indicates internal input port.
- NC - indicates not connected.
- PAD - indicates external port.
- X - indicates either logic level one or zero (don't care).
- Z - indicates three-state logic level (high resistance).

GLx**A500K, APA****Input**

PAD

Output

GL

Function

Global Input Buffer

This macro is available with a Schmitt Trigger for APA devices.

Truth Table

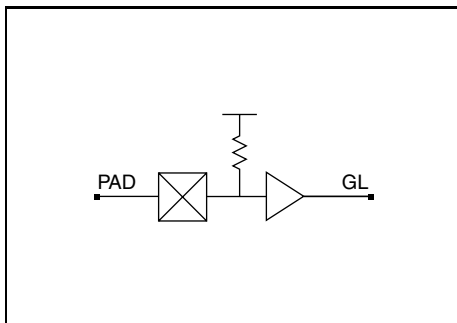
Input	Output
PAD	GL
0	0
1	1

Tile Usage

Family	I/O Tiles
All listed	2

Available GLx Macro Types

Name	Description
GL25	2.5 Volt CMOS input levels
GL33	3.3 Volt CMOS input levels
GL25LP	2.5 Volt CMOS input levels, low power
GL25S	2.5 Volt CMOS input levels, Schmitt Trigger
GL33S	3.3 Volt CMOS input levels, Schmitt Trigger
GL25LPS	2.5 Volt CMOS input levels, low power, Schmitt Trigger

GLxU**A500K, APA****Input**

PAD

Output

GL

Function

Global Input Buffer with Pull-up Resistor;

This macro is available with a Schmitt Trigger for APA devices.

Truth Table

Input	Output
PAD	GL
0	0
1	1
NC	1

Tile Usage

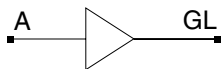
Family	I/O Tiles
All listed	2

Available GLxU Macro Types

Name	Description
GL25U	2.5 Volt CMOS input levels, with pull-up resistor
GL33U	3.3 Volt CMOS input levels, with pull-up resistor
GL25LPU	2.5 Volt CMOS input levels, low power, with pull-up resistor
GL25US	2.5 Volt CMOS input levels, with pull-up resistor, Schmitt Trigger
GL33US	3.3 Volt CMOS input levels, with pull-up resistor, Schmitt Trigger
GL25LPUS	2.5 Volt CMOS input levels, low power, with pull-up resistor, Schmitt Trigger

GLINT

A500K, APA

**Function**

Global Buffer with Internal Connection

Truth Table

Input	Output
A	GL
1	1
0	0

Tile Usage

Family	I/O Tiles
All listed	1

Input

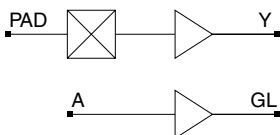
A

Output

GL

GLIBx

A500K, APA

**Function**Global Input Buffer with Independent Input Buffer;
This macro is available with a Schmitt Trigger for APA devices.**Truth Table**

Input	Output	Input	Output
PAD	Y	A	GL
1	1	1	1
0	0	0	0

Tile Usage

Family	I/O Tiles
All listed	2

Input

PAD, A

Output

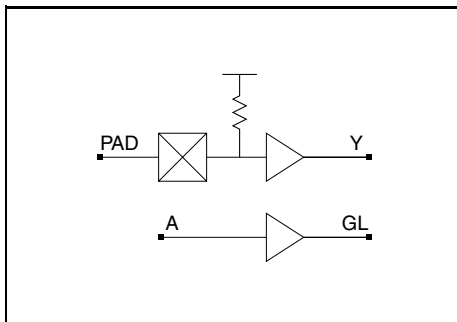
Y, GL

Available GLIBx Macro Types

Name	Description
GLIB25	2.5 Volt CMOS input levels
GLIB33	3.3 Volt CMOS input levels
GLIB25LP	2.5 Volt CMOS input levels, low power
GLIB25S	2.5 Volt CMOS input levels, Schmitt Trigger
GLIB33S	3.3 Volt CMOS input levels, Schmitt Trigger
GLIB25LPS	2.5 Volt CMOS input levels, low power, Schmitt Trigger

GLIBxU

A500K, APA

**Input**

PAD, A

Output

Y, GL

Function

Global Input Buffer with Independent Input Buffer and Pull-up Resistor. This macro is available with a Schmitt Trigger for APA devices.

Truth Table

Input	Output	Input	Output
PAD	Y	A	GL
1	1	1	1
0	0	0	0
NC	1		

Tile Usage

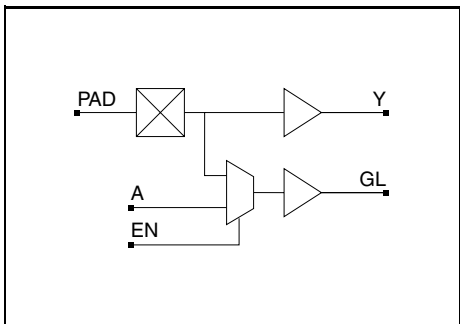
Family	I/O Tiles
All listed	2

Available GLIBxU Macro Types

Name	Description
GLIB25U	2.5 Volt CMOS input levels, with pull-up resistor
GLIB33U	3.3 Volt CMOS input levels, with pull-up resistor
GLIB25LPU	2.5 Volt CMOS input levels, low power, with pull-up resistor
GLIB25US	2.5 Volt CMOS input levels, with pull-up resistor and Schmitt Trigger
GLIB33US	3.3 Volt CMOS input levels, with pull-up resistor and Schmitt Trigger
GLIB25LPUS	2.5 Volt CMOS input levels, low power, with pull-up resistor and Schmitt Trigger

GLMIBx

A500K, APA

**Function**

Global Multiplexed Input Buffer
This macro is available with a Schmitt Trigger for APA devices.

Truth Table

Input	Output
PAD	Y
1	1
0	0

Truth Table

Input			Output
PAD	A	EN	GL
0	X	0	0
1	X	0	1
X	1	1	1
X	0	1	0

Input

PAD, A, EN

Output

Y, GL

Tile Usage

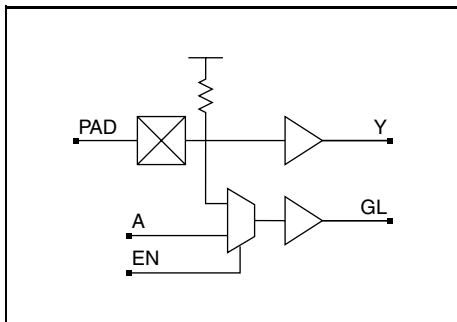
Family	I/O Tiles
All listed	2

Available GLMIBx Macro Types

Name	Description
GLMIB25	2.5 Volt CMOS input levels
GLMIB33	3.3 Volt CMOS input levels
GLMIB25LP	2.5 Volt CMOS input levels, low power
GLMIB25S	2.5 Volt CMOS input levels, Schmitt Trigger
GLMIB33S	3.3 Volt CMOS input levels, Schmitt Trigger
GLMIB25LPS	2.5 Volt CMOS input levels, low power, Schmitt Trigger

GLMIBxU

A500K, APA

**Function**

Global Multiplexed Input Buffer with Pull-up Resistor; this macro is available with a Schmitt Trigger for APA devices.

Truth Table

Input	Output
PAD	Y
1	1
0	0
NC	1

Truth Table

Input			Output
PAD	A	EN	GL
0	X	0	0
1	X	0	1
X	1	1	1
X	0	1	0
NC	X	0	1

Input

PAD, A, EN

Output

Y, GL

Tile Usage

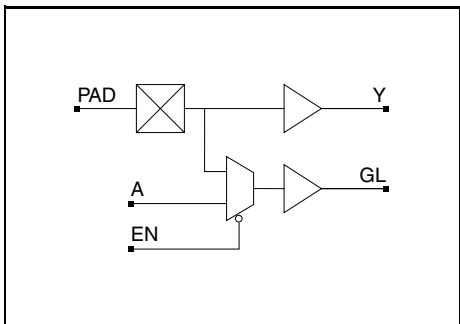
Family	I/O Tiles
All listed	2

Available GLMIBxU Macro Types

Name	Description
GLMIB25U	2.5 Volt CMOS input levels, with pull-up resistor
GLMIB33U	3.3 Volt CMOS input levels, with pull-up resistor
GLMIB25LPU	2.5 Volt CMOS input levels, low power, with pull-up resistor
GLMIB25US	2.5 Volt CMOS input levels, with pull-up resistor and Schmitt Trigger
GLMIB33US	3.3 Volt CMOS input levels, with pull-up resistor and Schmitt Trigger
GLMIB25LPUS	2.5 Volt CMOS input levels, low power, with pull-up resistor and Schmitt Trigger

GLMIBLx

A500K, APA

**Function**

Global Multiplexed Input Buffer with Active Low Enable; this macro is available with a Schmitt Trigger for APA devices.

Truth Table

Input	Output
PAD	Y
1	1
0	0

Truth Table

Input			Output
PAD	A	EN	GL
X	0	0	0
X	1	0	1
1	X	1	1
0	X	1	0

Input

PAD, A, EN

Output

Y, GL

Tile Usage

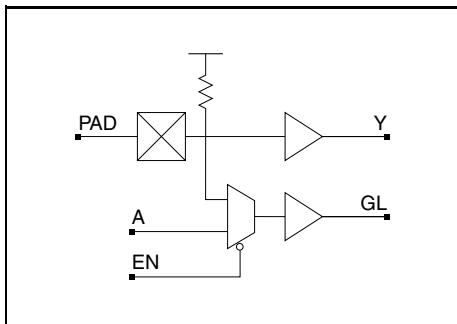
Family	I/O Tiles
All listed	2

Available GLMIBLxU Macro Types

Name	Description
GLMIBL25	2.5 Volt CMOS input levels
GLMIBL33	3.3 Volt CMOS input levels
GLMIBL25LP	2.5 Volt CMOS input levels, low power
GLMIBL25S	2.5 Volt CMOS input levels, Schmitt Trigger
GLMIBL33S	3.3 Volt CMOS input levels, Schmitt Trigger
GLMIBL25LPS	2.5 Volt CMOS input levels, low power, Schmitt Trigger

GLMIBLxU

A500K, APA

**Function**

Global Multiplexed Input Buffer with Active Low Enable and Pull-up Resistor. This macro is available with a Schmitt Trigger for APA devices.

Truth Table

Input	Output
PAD	Y
0	0
1	1
NC	1

Input

PAD, A, EN

Output

Y, GL

Tile Usage

Family	I/O Tiles
All listed	2

Truth Table

PAD	Input			Output
	A	EN	GL	
X	0	0	0	
X	1	0	1	
1	X	1	1	
0	X	1	0	
NC	X	1	1	

Available GLMIBLxU Macro Types

Name	Description
GLMIBL25U	2.5 Volt CMOS input levels, with pull-up resistor
GLMIBL33U	3.3 Volt CMOS input levels, with pull-up resistor
GLMIBL25LPU	2.5 Volt CMOS input levels, low power, with pull-up resistor
GLMIBL25US	2.5 Volt CMOS input levels, with pull-up resistor and Schmitt Trigger
GLMIBL33US	3.3 Volt CMOS input levels, with pull-up resistor and Schmitt Trigger
GLMIBL25LPUS	2.5 Volt CMOS input levels, low power, with pull-up resistor and Schmitt Trigger

IBx

A500K, APA

**Function**

Input Buffer
This macro is available with a Schmitt Trigger for APA devices.

Truth Table

Input	Output
PAD	Y
0	0
1	1

Tile Usage

Family	I/O Tiles
All listed	1

Input

PAD

Output

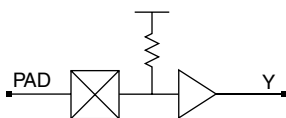
Y

Available IBx Macro Types

Name	Description
IB25	2.5 Volt CMOS input levels
IB33	3.3 Volt CMOS input levels
IB25LP	2.5 Volt CMOS input levels, low power
IB25S	2.5 Volt CMOS input levels, Schmitt Trigger
IB33S	3.3 Volt CMOS input levels, Schmitt Trigger
IB25LPS	2.5 Volt CMOS input levels, low power, Schmitt Trigger

IBxU

A500K, APA

**Function**

Input Buffer with Pull-up Resistor
This macro is available with a Schmitt Trigger for APA devices.

Truth Table

Input	Output
PAD	Y
0	0
1	1
NC	1

Tile Usage

Family	I/O Tiles
All listed	1

Input

PAD

Output

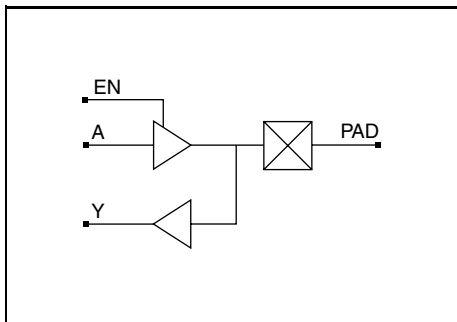
Y

Available IBxU Macro Types

Name	Description
IB25U	2.5 Volt CMOS input levels, with pull-up resistor
IB33U	3.3 Volt CMOS input levels, with pull-up resistor
IB25LPU	2.5 Volt CMOS input levels, low power, with pull-up resistor
IB25US	2.5 Volt CMOS input levels, with pull-up resistor and Schmitt Trigger
IB33US	3.3 Volt CMOS input levels, with pull-up resistor and Schmitt Trigger
IB25LPUS	2.5 Volt CMOS input levels, low power, with pull-up resistor and Schmitt Trigger

IOB25x

A500K, APA

**Input**

EN, A, PAD

Output

PAD, Y

Function

Bi-Directional Buffer

Truth Table

Input			Output	
EN	A	PAD	PAD	Y
1	X	X	A	A
0	X	X	X	PAD

Tile Usage

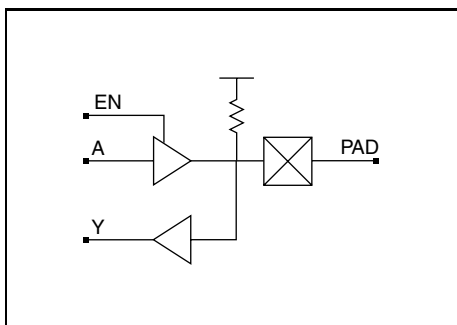
Family	I/O Tiles
All listed	1

Available IOB25x Macro Types

Name	Description
IOB25HH	2.5 Volt CMOS input levels, high drive strength, high slew rate
IOB25HL	2.5 Volt CMOS input levels, high drive strength, low slew rate
IOB25HN	2.5 Volt CMOS input levels, high drive strength, normal slew rate
IOB25LH	2.5 Volt CMOS input levels, low drive strength, high slew rate
IOB25LL	2.5 Volt CMOS input levels, low drive strength, low slew rate
IOB25LN	2.5 Volt CMOS input levels, low drive strength, normal slew rate

IOB25xU

A500K, APA

**Input**

EN, A, PAD

Output

PAD, Y

Function

Bi-Directional Buffer with Pull-up Resistor

Truth Table

Input			Output	
EN	A	PAD	PAD	Y
1	X	X	A	A
0	X	X	X	PAD
0	X	NC	NC	1

Tile Usage

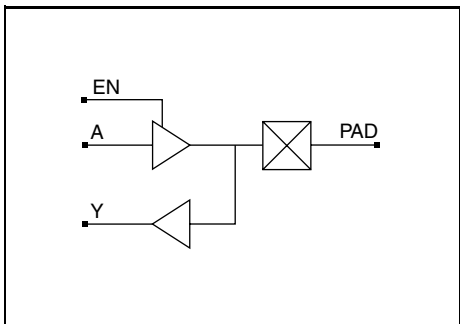
Family	I/O Tiles
All listed	1

Available IOB25xU Macro Types

Name	Description
IOB25HHU	2.5 Volt CMOS input levels, high drive strength, high slew rate, with pull-up resistor
IOB25HLU	2.5 Volt CMOS input levels, high drive strength, low slew rate, with pull-up resistor
IOB25HNU	2.5 Volt CMOS input levels, high drive strength, normal slew rate, with pull-up resistor
IOB25LHU	2.5 Volt CMOS input levels, low drive strength, high slew rate, with pull-up resistor
IOB25LLU	2.5 Volt CMOS input levels, low drive strength, low slew rate, with pull-up resistor
IOB25LNU	2.5 Volt CMOS input levels, low drive strength, normal slew rate, with pull-up resistor

IOB25LPx

A500K, APA

**Function**

Bi-Directional Buffer (Low Power)

Truth Table

Input			Output	
EN	A	PAD	PAD	Y
1	X	X	A	A
0	X	X	X	PAD

Tile Usage

Family	I/O Tiles
All listed	1

Input

EN, A, PAD

Output

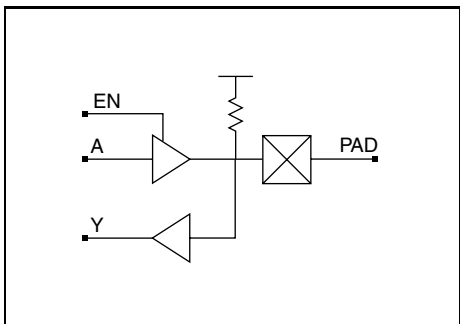
PAD, Y

Available IOB25LPx Macro Types

Name	Description
IOB25LPHH	2.5 Volt CMOS input levels, low power, high drive strength, high slew rate
IOB25LPHL	2.5 Volt CMOS input levels, low power, high drive strength, low slew rate
IOB25LPHN	2.5 Volt CMOS input levels, low power, high drive strength, normal slew rate
IOB25LPLH	2.5 Volt CMOS input levels, low power, low drive strength, high slew rate
IOB25LPLL	2.5 Volt CMOS input levels, low power, low drive strength, low slew rate
IOB25LPLN	2.5 Volt CMOS input levels, low power, low drive strength, normal slew rate

IOB25LPxU

A500K, APA

**Function**

Bi-Directional Buffer with Low Power and Pull-up Resistor

Truth Table

Input			Output	
EN	A	PAD	PAD	Y
1	X	X	A	A
0	X	X	X	PAD
0	X	NC	NC	1

Tile Usage

Family	I/O Tiles
All listed	1

Input

EN, A, PAD

Output

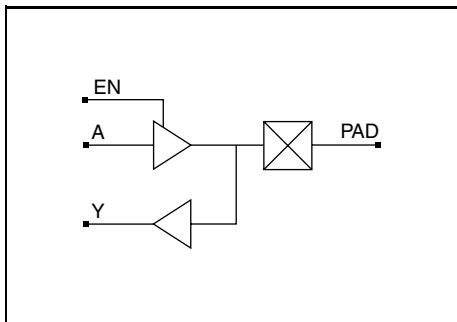
PAD, Y

Available IOB25LPxU Macro Types

Name	Description
IOB25LPHHU	2.5 Volt CMOS input levels, low power, high drive strength, high slew rate, with pull-up resistor
IOB25LPHLU	2.5 Volt CMOS input levels, low power, high drive strength, low slew rate, with pull-up resistor
IOB25LPHNU	2.5 Volt CMOS input levels, low power, high drive strength, normal slew rate, with pull-up resistor
IOB25LPLHU	2.5 Volt CMOS input levels, low power, low drive strength, high slew rate, with pull-up resistor
IOB25LPLLU	2.5 Volt CMOS input levels, low power, low drive strength, low slew rate, with pull-up resistor
IOB25LPLNU	2.5 Volt CMOS input levels, low power, low drive strength, normal slew rate, with pull-up resistor

IOB33x

A500K, APA

**Function**

Bi-Directional Buffer

Truth Table

Input			Output	
EN	A	PAD	PAD	Y
1	X	X	A	A
0	X	X	X	PAD

Tile Usage

Family	I/O Tiles
All listed	1

Input

EN, A, PAD

Output

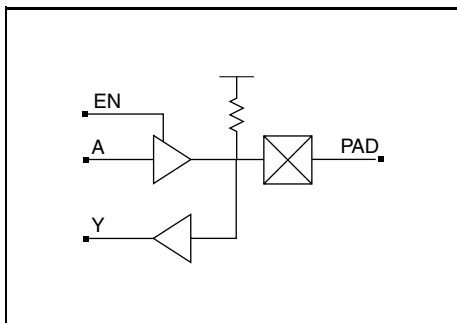
PAD, Y

Available IOB33x Macro Types

Name	Description
IOB33LH	3.3 Volt CMOS input levels, low strength drive, high slew rate
IOB33LL	3.3 Volt CMOS input levels, low strength drive, low slew rate
IOB33LN	3.3 Volt CMOS input levels, low strength drive, normal slew rate
IOB33PH	3.3 Volt CMOS input levels, PCI compliant, high slew rate
IOB33PL	3.3 Volt CMOS input levels, PCI compliant, low slew rate
IOB33PN	3.3 Volt CMOS input levels, PCI compliant, normal slew rate

IOB33xU

A500K, APA

**Function**

Bi-Directional Buffer with Pull-up Resistor

Truth Table

Input			Output	
EN	A	PAD	PAD	Y
1	X	X	A	A
0	X	X	X	PAD
0	X	NC	NC	1

Tile Usage

Family	I/O Tiles
All listed	1

Input

EN, A, PAD

Output

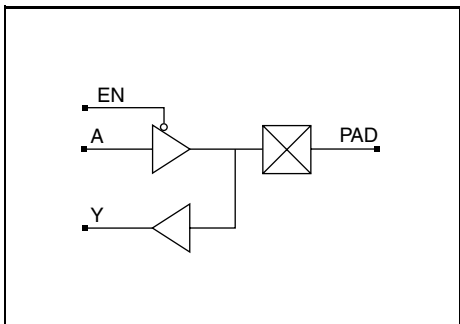
PAD, Y

Available IOB33xU Macro Types

Name	Description
IOB33LHU	3.3 Volt CMOS input levels, low strength drive, high slew rate, with pull-up resistor
IOB33LLU	3.3 Volt CMOS input levels, low strength drive, low slew rate, with pull-up resistor
IOB33LNU	3.3 Volt CMOS input levels, low strength drive, normal slew rate, with pull-up resistor
IOB33PHU	3.3 Volt CMOS input levels, PCI compliant, high slew rate, with pull-up resistor
IOB33PLU	3.3 Volt CMOS input levels, PCI compliant, low slew rate, with pull-up resistor
IOB33PNU	3.3 Volt CMOS input levels, PCI compliant, normal slew rate, with pull-up resistor

IOBL25x

A500K, APA

**Function**

Bi-Directional Buffer with Active Low Enable

Truth Table

Input			Output	
EN	A	PAD	PAD	Y
1	X	X	X	PAD
0	X	X	A	A

Tile Usage

Family	I/O Tiles
All listed	1

Input

EN, A, PAD

Output

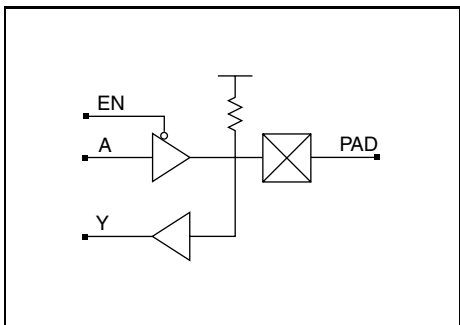
PAD, Y

Available IOBL25x Macro Types

Name	Description
IOBL25HH	2.5 Volt CMOS input levels, high drive strength, high slew rate
IOBL25HL	2.5 Volt CMOS input levels, high drive strength, low slew rate
IOBL25HN	2.5 Volt CMOS input levels, high drive strength, normal slew rate
IOBL25LH	2.5 Volt CMOS input levels, low drive strength, high slew rate
IOBL25LL	2.5 Volt CMOS input levels, low drive strength, low slew rate
IOBL25LN	2.5 Volt CMOS input levels, low drive strength, normal slew rate

IOBL25xU

A500K, APA

**Function**

Bi-Directional Buffer with Active Low Enable and Pull-up Resistor

Truth Table

Input			Output	
EN	A	PAD	PAD	Y
1	X	X	X	PAD
0	X	X	A	A
1	X	NC	NC	1

Tile Usage

Family	I/O Tiles
All listed	1

Input

EN, A, PAD

Output

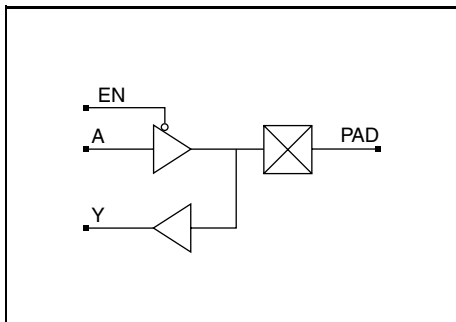
PAD, Y

Available IOBL25xU Macro Types

Name	Description
IOBL25HHU	2.5 Volt CMOS input levels, high drive strength, high slew rate, with pull-up resistor
IOBL25HLU	2.5 Volt CMOS input levels, high drive strength, low slew rate, with pull-up resistor
IOBL25HNU	2.5 Volt CMOS input levels, high drive strength, normal slew rate, with pull-up resistor
IOBL25LHU	2.5 Volt CMOS input levels, low drive strength, high slew rate, with pull-up resistor
IOBL25LLU	2.5 Volt CMOS input levels, low drive strength, low slew rate, with pull-up resistor
IOBL25LNU	2.5 Volt CMOS input levels, low drive strength, normal slew rate, with pull-up resistor

IOBL25LPx

A500K, APA

**Function**

Bi-Directional Buffer with Active Low Enable (Low Power)

Truth Table

Input			Output	
EN	A	PAD	PAD	Y
1	X	X	X	PAD
0	X	X	A	A

Tile Usage

Family	I/O Tiles
All listed	1

Input

EN, A, PAD

Output

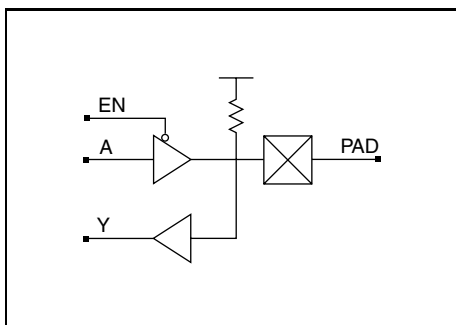
PAD, Y

Available IOBL25LPx Macro Types

Name	Description
IOBL25LPHH	2.5 Volt CMOS input levels, low power, high drive strength, high slew rate
IOBL25LPHL	2.5 Volt CMOS input levels, low power, high drive strength, low slew rate
IOBL25LPHN	2.5 Volt CMOS input levels, low power, high drive strength, normal slew rate
IOBL25LPLH	2.5 Volt CMOS input levels, low power, low drive strength, high slew rate
IOBL25LPLL	2.5 Volt CMOS input levels, low power, low drive strength, low slew rate
IOBL25LPLN	2.5 Volt CMOS input levels, low power, low drive strength, normal slew rate

IOBL25LPxU

A500K, APA

**Function**

Bi-Directional Buffer with Active Low Enable, Low Power, and Pull-up Resistor

Truth Table

Input			Output	
EN	A	PAD	PAD	Y
1	X	X	X	PAD
0	X	X	A	A
1	X	NC	NC	1

Tile Usage

Family	I/O Tiles
All listed	1

Input

EN, A, PAD

Output

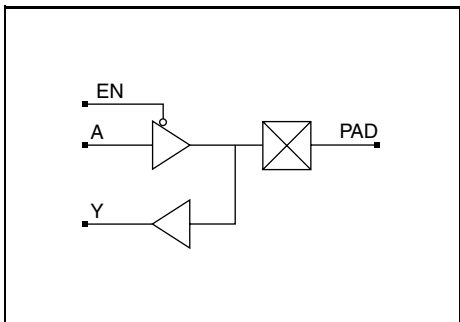
PAD, Y

Available IOBL25LPxU Macro Types

Name	Description
IOBL25LPHHU	2.5 Volt CMOS input levels, low power, high drive strength, high slew rate, with pull-up resistor
IOBL25LPHLU	2.5 Volt CMOS input levels, low power, high drive strength, low slew rate, with pull-up resistor
IOBL25LPHNU	2.5 Volt CMOS input levels, low power, high drive strength, normal slew rate, with pull-up resistor
IOBL25LPLHU	2.5 Volt CMOS input levels, low power, low drive strength, high slew rate, with pull-up resistor
IOBL25LPLLU	2.5 Volt CMOS input levels, low power, low drive strength, low slew rate, with pull-up resistor
IOBL25LPLNU	2.5 Volt CMOS input levels, low power, low drive strength, normal slew rate, with pull-up resistor

IOBL33x

A500K, APA

**Function**

Bi-Directional Buffer with Active Low Enable

Truth Table

Input			Output	
EN	A	PAD	PAD	Y
1	X	X	X	PAD
0	X	X	A	A

Tile Usage

Family	I/O Tiles
All listed	1

Input
EN, PAD, A

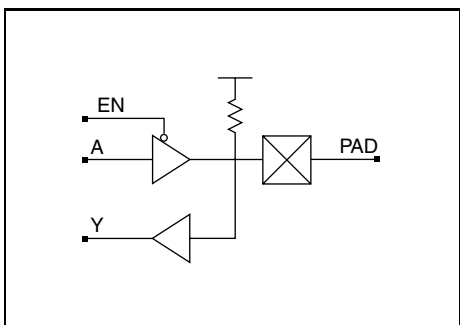
Output
PAD, Y

Available IOBL33x Macro Types

Name	Description
IOBL33LH	3.3 Volt CMOS input levels, low strength drive, high slew rate
IOBL33LL	3.3 Volt CMOS input levels, low strength drive, low slew rate
IOBL33LN	3.3 Volt CMOS input levels, low strength drive, normal slew rate
IOBL33PH	3.3 Volt CMOS input levels, PCI compliant, high slew rate
IOBL33PL	3.3 Volt CMOS input levels, PCI compliant, low slew rate
IOBL33PN	3.3 Volt CMOS input levels, PCI compliant, normal slew rate

IOBL33xU

A500K, APA

**Function**

Bi-Directional Buffer with Active Low Enable and Pull-up Resistor

Truth Table

Input			Output	
EN	A	PAD	PAD	Y
1	X	X	X	PAD
0	X	X	A	A
1	X	NC	NC	1

Tile Usage

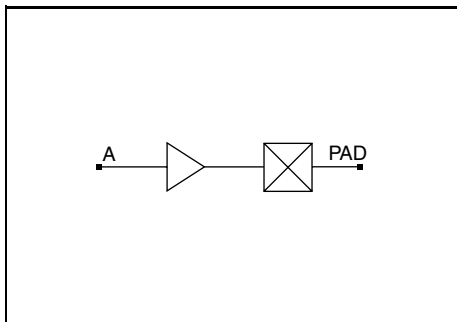
Family	I/O Tiles
All listed	1

Input
EN, PAD, A

Output
PAD, Y

Available IOBL33xU Macro Types

Name	Description
IOBL33LHU	3.3 Volt CMOS input levels, low strength drive, high slew rate, with pull-up resistor
IOBL33LLU	3.3 Volt CMOS input levels, low strength drive, low slew rate, with pull-up resistor
IOBL33LNU	3.3 Volt CMOS input levels, low strength drive, normal slew rate, with pull-up resistor
IOBL33PHU	3.3 Volt CMOS input levels, PCI compliant, high slew rate, with pull-up resistor
IOBL33PLU	3.3 Volt CMOS input levels, PCI compliant, low slew rate, with pull-up resistor
IOBL33PNU	3.3 Volt CMOS input levels, PCI compliant, normal slew rate, with pull-up resistor

OB25x**A500K, APA****Function**

Output Buffer

Truth Table

Input	Output
A	PAD
0	0
1	1

Tile Usage

Family	I/O Tiles
All listed	1

Input

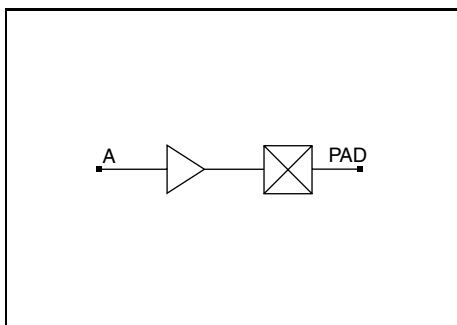
A

Output

PAD

Available OB25x Macro Types

Name	Description
OB25HH	2.5 Volt CMOS input levels, high strength drive, high slew rate
OB25HL	2.5 Volt CMOS input levels, high strength drive, low slew rate
OB25HN	2.5 Volt CMOS input levels, high strength drive, normal slew rate
OB25LH	2.5 Volt CMOS input levels, low strength drive, high slew rate
OB25LL	2.5 Volt CMOS input levels, low strength drive, low slew rate
OB25LN	2.5 Volt CMOS input levels, low strength drive, normal slew rate

OB25LPx**A500K, APA****Function**

Output Buffer (Low Power)

Truth Table

Input	Output
A	PAD
0	0
1	1

Tile Usage

Family	I/O Tiles
All listed	1

Input

A

Output

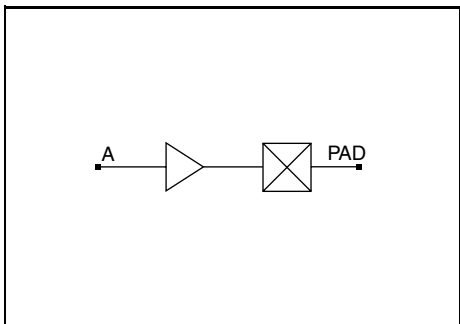
PAD

Available OB25LPx Macro Types

Name	Description
OB25LPHH	2.5 Volt CMOS input levels, low power, high strength drive, high slew rate
OB25LPHL	2.5 Volt CMOS input levels, low power, high strength drive, low slew rate
OB25LPHN	2.5 Volt CMOS input levels, low power, high strength drive, normal slew rate
OB25LPLH	2.5 Volt CMOS input levels, low power, low strength drive, high slew rate
OB25LPLL	2.5 Volt CMOS input levels, low power, low strength drive, low slew rate
OB25LPLN	2.5 Volt CMOS input levels, low power, low strength drive, normal slew rate

OB33x

A500K, APA

**Function**

Output Buffer

Truth Table

Input	Output
A	PAD
0	0
1	1

Tile Usage

Family	I/O Tiles
All listed	1

Input

A

Output

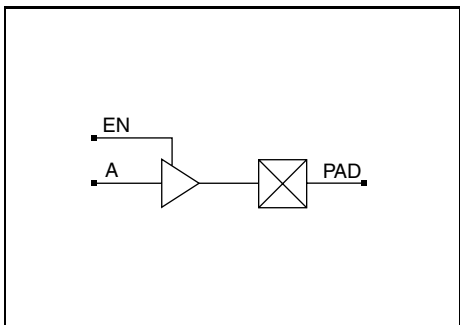
PAD

Available OB33x Macro Types

Name	Description
OB33LH	3.3 Volt CMOS input levels, low strength drive, high slew rate
OB33LL	3.3 Volt CMOS input levels, low strength drive, low slew rate
OB33LN	3.3 Volt CMOS input levels, low strength drive, normal slew rate
OB33PH	3.3 Volt CMOS input levels, PCI compliant, high slew rate
OB33PL	3.3 Volt CMOS input levels, PCI compliant, low slew rate
OB33PN	3.3 Volt CMOS input levels, PCI compliant, normal slew rate

OTB25x

A500K, APA

**Function**

Three State Output Buffer

Truth Table

Input		Output
EN	A	PAD
0	X	Z
1	1	1
1	0	0

Tile Usage

Family	I/O Tiles
All listed	1

Input

EN, A

Output

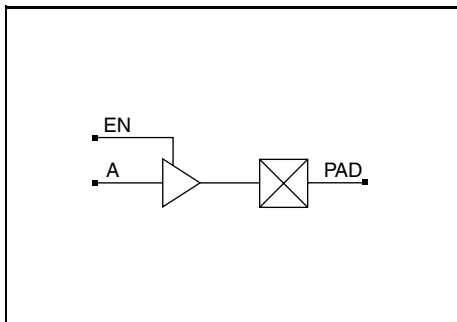
PAD

Available OTB25x Macro Types

Name	Description
OTB25HH	2.5 Volt CMOS input levels, high strength drive, high slew rate
OTB25HL	2.5 Volt CMOS input levels, high strength drive, low slew rate
OTB25HN	2.5 Volt CMOS input levels, high strength drive, normal slew rate
OTB25LH	2.5 Volt CMOS input levels, low strength drive, high slew rate
OTB25LL	2.5 Volt CMOS input levels, low strength drive, low slew rate
OTB25LN	2.5 Volt CMOS input levels, low strength drive, normal slew rate

OTB25LPx

A500K, APA

**Function**

Three State Output Buffer (Low Power)

Truth Table

Input		Output
EN	A	PAD
0	X	Z
1	1	1
1	0	0

Tile Usage

Family	I/O Tiles
All listed	1

Input

EN, A

Output

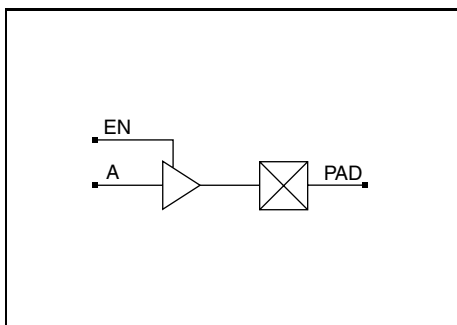
PAD

Available OTB25LPx Macro Types

Name	Description
OTB25LPLH	2.5 Volt CMOS input levels, low power, high strength drive, high slew rate
OTB25LPLL	2.5 Volt CMOS input levels, low power, high strength drive, low slew rate
OTB25LPLN	2.5 Volt CMOS input levels, low power, high strength drive, normal slew rate
OTB25LPLH	2.5 Volt CMOS input levels, low power, low strength drive, high slew rate
OTB25LPLL	2.5 Volt CMOS input levels, low power, low strength drive, low slew rate
OTB25LPLN	2.5 Volt CMOS input levels, low power, low strength drive, normal slew rate

OTB33x

A500K, APA

**Function**

Three State Output Buffer

Truth Table

Input		Output
EN	A	PAD
0	X	Z
1	1	1
1	0	0

Tile Usage

Family	I/O Tiles
All listed	1

Input

EN, A

Output

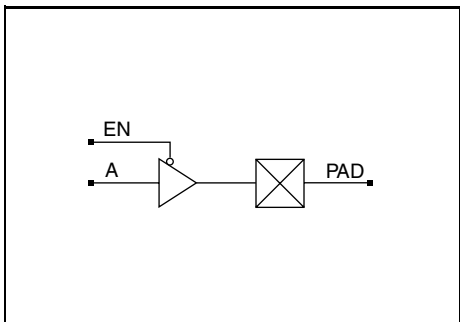
PAD

Available OTB33x Macro Types

Name	Description
OTB33LH	3.3 Volt CMOS input levels, low strength drive, high slew rate
OTB33LL	3.3 Volt CMOS input levels, low strength drive, low slew rate
OTB33LN	3.3 Volt CMOS input levels, low strength drive, normal slew rate
OTB33PH	3.3 Volt CMOS input levels, PCI compliant, high slew rate
OTB33PL	3.3 Volt CMOS input levels, PCI compliant, low slew rate
OTB33PN	3.3 Volt CMOS input levels, PCI compliant, normal slew rate

OTBL25x

A500K, APA

**Function**

Three State Output Buffer with Active Low Enable

Truth Table

Input		Output
EN	A	PAD
0	0	0
0	1	1
1	X	Z

Tile Usage

Family	I/O Tiles
All listed	1

Input

EN, A

Output

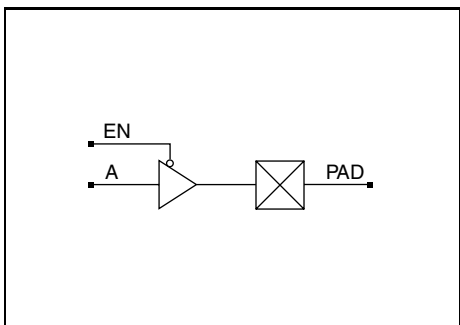
PAD

Available OTBL25x Macro Types

Name	Description
OTBL25HH	2.5 Volt CMOS input levels, high strength drive, high slew rate
OTBL25HL	2.5 Volt CMOS input levels, high strength drive, low slew rate
OTBL25HN	2.5 Volt CMOS input levels, high strength drive, normal slew rate
OTBL25LH	2.5 Volt CMOS input levels, low strength drive, high slew rate
OTBL25LL	2.5 Volt CMOS input levels, low strength drive, low slew rate
OTBL25LN	2.5 Volt CMOS input levels, low strength drive, normal slew rate

OTBL25LPx

A500K, APA

**Function**

Three State Output Buffer with Active Low Enable

Truth Table

Input		Output
EN	A	PAD
0	0	0
0	1	1
1	X	Z

Tile Usage

Family	I/O Tiles
All listed	1

Input

EN, A

Output

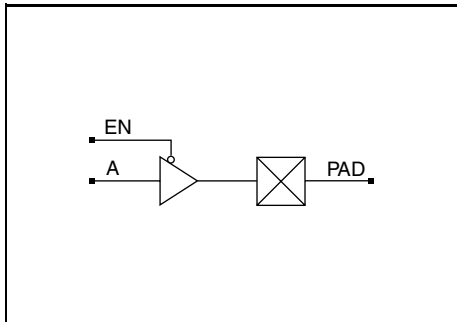
PAD

Available OTBL25LPx Macro Types

Name	Description
OTBL25LPLH	2.5 Volt CMOS input levels, low power, high strength drive, high slew rate
OTBL25LPLL	2.5 Volt CMOS input levels, low power, high strength drive, low slew rate
OTBL25LPLN	2.5 Volt CMOS input levels, low power, high strength drive, normal slew rate
OTBL25LPPH	2.5 Volt CMOS input levels, low power, low strength drive, high slew rate
OTBL25LPPL	2.5 Volt CMOS input levels, low power, low strength drive, low slew rate
OTBL25LPPN	2.5 Volt CMOS input levels, low power, low strength drive, normal slew rate

OTBL33x

A500K, APA

**Function**

Three State Output Buffer with Active Low Enable

Truth Table

Input		Output
EN	A	PAD
0	0	0
0	1	1
1	X	Z

Tile Usage

Family	I/O Tiles
All listed	1

Input

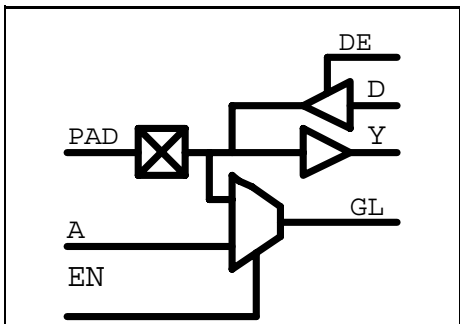
EN, A

Output

PAD

Available OTBL33X Macro Types

Name	Description
OTBL33LH	3.3 Volt CMOS input levels, low strength drive, high slew rate
OTBL33LL	3.3 Volt CMOS input levels, low strength drive, low slew rate
OTBL33LN	3.3 Volt CMOS input levels, low strength drive, normal slew rate
OTBL33PH	3.3 Volt CMOS input levels, PCI compliant, high slew rate
OTBL33PL	3.3 Volt CMOS input levels, PCI compliant, low slew rate
OTBL33PN	3.3 Volt CMOS input levels, PCI compliant, normal slew rate

**Input**

DE, D, PAD, A, EN

Output

PAD, Y, GL

Function

Bi-directional IO buffer and global connection

Truth Table

Input					Output		
DE	D	PAD	A	EN	PAD	Y	GL
1	X	N/A	X	0	D	D	D
1	X	N/A	X	1	D	D	A
0	X	X	X	0	N/A	PAD	PAD
0	X	X	X	1	N/A	PAD	A

Tile Usage

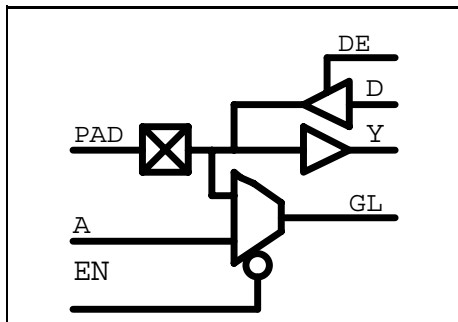
Family	I/O Tiles
All listed	1

Available GLMIOBx Macro Types

Name	Description
GLMIOB25LLU	2.5 Volt CMOS input levels, low power, low slew, w/ pull-up resistor
GLMIOB25LL	2.5 Volt CMOS input levels, low power, low slew
GLMIOB25LNU	2.5 Volt CMOS input levels, low power, normal slew, w/ pull up resistor
GLMIOB25LN	2.5 Volt CMOS input levels, low power, normal slew
GLMIOB25LHU	2.5 Volt CMOS input levels, low power, high slew, w/ pull-up resistor
GLMIOB25LH	2.5 Volt CMOS input levels, low power, high slew
GLMIOB25HLU	2.5 Volt CMOS input levels, high power, low slew, w/ pull-up resistor
GLMIOB25HL	2.5 Volt CMOS input levels, high power, low slew
GLMIOB25HNU	2.5 Volt CMOS input levels, high power, normal slew, w/ pull-up resistor
GLMIOB25HN	2.5 Volt CMOS input levels, high power, normal slew
GLMIOB25HHU	2.5 Volt CMOS input levels, high power, high slew, w/ pull-up resistor
GLMIOB25HH	2.5 Volt CMOS input levels, high power, high slew
GLMIOB25LPLU	2.5 Volt CMOS input levels, low power, low strength, low slew, w/ pull-up resistor
GLMIOB25LPLL	2.5 Volt CMOS input levels, low power, low strength, low slew
GLMIOB25LPLNU	2.5 Volt CMOS input levels, low power, low strength, normal slew, w/ pull-up resistor
GLMIOB25LPLN	2.5 Volt CMOS input levels, low power, low strength, normal slew
GLMIOB25LPLHU	2.5 Volt CMOS input levels, low power, low strength, high slew, w/ pull-up resistor
GLMIOB25LPLH	2.5 Volt CMOS input levels, low power, low strength, high slew
GLMIOB25LPHLU	2.5 Volt CMOS input levels, low power, high strength, low slew, w/ pull-up resistor
GLMIOB25LPHL	2.5 Volt CMOS input levels, low power, high strength, low slew
GLMIOB25LPHN	2.5 Volt CMOS input levels, low power, high strength, normal slew
GLMIOB25LPHNU	2.5 Volt CMOS input levels, low power, high strength, normal slew, w/ pull-up resistor
GLMIOB25LPHHU	2.5 Volt CMOS input levels, low power, high strength, high slew, w/ pull-up resistor
GLMIOB25LPHH	2.5 Volt CMOS input levels, low power, high strength, high slew
GLMIOB33LLU	3.3 Volt CMOS input levels, low power, low slew, w/ pull-up resistor
GLMIOB33LL	3.3 Volt CMOS input levels, low power, low slew
GLMIOB33LNU	3.3 Volt CMOS input levels, low power, normal slew, w/ pull up resistor
GLMIOB33LN	3.3 Volt CMOS input levels, low power, normal slew
GLMIOB33LHU	3.3 Volt CMOS input levels, low power, high slew, w/ pull-up resistor
GLMIOB33LH	3.3 Volt CMOS input levels, low power, high slew
GLMIOB33PLU	3.3 Volt CMOS input levels, PCI compliant, low slew, w/ pull-up resistor
GLMIOB33PL	3.3 Volt CMOS input levels, PCI compliant, low slew
GLMIOB33PNU	3.3 Volt CMOS input levels, PCI compliant, normal slew, w/ pull-up resistor
GLMIOB33PN	3.3 Volt CMOS input levels, PCI compliant, normal slew
GLMIOB33PHU	3.3 Volt CMOS input levels, PCI compliant, high slew, w/ pull-up resistor
GLMIOB33PH	3.3 Volt CMOS input levels, PCI compliant, high slew

GLMIOBLx

APA

**Input**

DE, D, PAD, A, EN

Output

PAD, Y, GL

Function

Bi-directional IO buffer and global connection, with active low enable

Truth Table

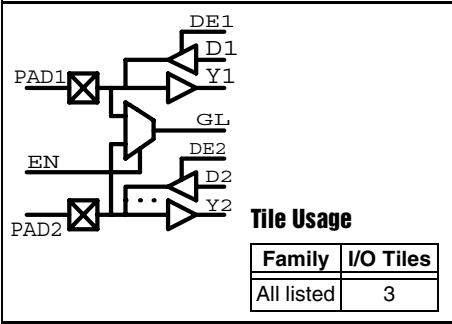
Input					Output		
DE	D	PAD	A	EN	PAD	Y	GL
1	X	N/A	X	0	D	D	A
1	X	N/A	X	1	D	D	D
0	X	X	X	0	N/A	PAD	A
0	X	X	X	1	N/A	PAD	PAD

Tile Usage

Family	I/O Tiles
All listed	2

Available GLMIOBLx Macro Types

Name	Description
GLMIOBL25LLU	2.5 Volt CMOS input levels, low power, low slew, w/ pull-up resistor
GLMIOBL25LL	2.5 Volt CMOS input levels, low power, low slew
GLMIOBL25LNU	2.5 Volt CMOS input levels, low power, normal slew, w/ pull up resistor
GLMIOBL25LN	2.5 Volt CMOS input levels, low power, normal slew
GLMIOBL25LHU	2.5 Volt CMOS input levels, low power, high slew, w/ pull-up resistor
GLMIOBL25LH	2.5 Volt CMOS input levels, low power, high slew
GLMIOBL25HLU	2.5 Volt CMOS input levels, high power, low slew, w/ pull-up resistor
GLMIOBL25HL	2.5 Volt CMOS input levels, high power, low slew
GLMIOBL25HNU	2.5 Volt CMOS input levels, high power, normal slew, w/ pull-up resistor
GLMIOBL25HN	2.5 Volt CMOS input levels, high power, normal slew
GLMIOBL25HHU	2.5 Volt CMOS input levels, high power, high slew, w/ pull-up resistor
GLMIOBL25HH	2.5 Volt CMOS input levels, high power, high slew
GLMIOBL25LPLLU	2.5 Volt CMOS input levels, low power, low strength, low slew, w/ pull-up resistor
GLMIOBL25LPLL	2.5 Volt CMOS input levels, low power, low strength, low slew
GLMIOBL25LPLNU	2.5 Volt CMOS input levels, low power, low strength, normal slew, w/ pull-up resistor
GLMIOBL25LPLN	2.5 Volt CMOS input levels, low power, low strength, normal slew
GLMIOBL25LPLHU	2.5 Volt CMOS input levels, low power, low strength, high slew, w/ pull-up resistor
GLMIOBL25LPLH	2.5 Volt CMOS input levels, low power, low strength, high slew
GLMIOBL25LPLHU	2.5 Volt CMOS input levels, low power, high strength, low slew, w/ pull-up resistor
GLMIOBL25LPLH	2.5 Volt CMOS input levels, low power, high strength, low slew
GLMIOBL25LPHN	2.5 Volt CMOS input levels, low power, high strength, normal slew
GLMIOBL25LPHNU	2.5 Volt CMOS input levels, low power, high strength, normal slew, w/ pull-up resistor
GLMIOBL25LPHHU	2.5 Volt CMOS input levels, low power, high strength, high slew, w/ pull-up resistor
GLMIOBL25LPHH	2.5 Volt CMOS input levels, low power, high strength, high slew
GLMIOBL33LLU	3.3 Volt CMOS input levels, low power, low slew, w/ pull-up resistor
GLMIOBL33LL	3.3 Volt CMOS input levels, low power, low slew
GLMIOBL33LNU	3.3 Volt CMOS input levels, low power, normal slew, w/ pull up resistor
GLMIOBL33LN	3.3 Volt CMOS input levels, low power, normal slew
GLMIOBL33LHU	3.3 Volt CMOS input levels, low power, high slew, w/ pull-up resistor
GLMIOBL33LH	3.3 Volt CMOS input levels, low power, high slew
GLMIOBL33PLU	3.3 Volt CMOS input levels, PCI compliant, low slew, w/ pull-up resistor
GLMIOBL33PL	3.3 Volt CMOS input levels, PCI compliant, low slew
GLMIOBL33PNU	3.3 Volt CMOS input levels, PCI compliant, normal slew, w/ pull-up resistor
GLMIOBL33PN	3.3 Volt CMOS input levels, PCI compliant, normal slew
GLMIOBL33PHU	3.3 Volt CMOS input levels, PCI compliant, high slew, w/ pull-up resistor
GLMIOBL33PH	3.3 Volt CMOS input levels, PCI compliant, high slew



Function
Two bi-directional IO pads (global and regular), multiplexed

Truth Table

Input							Output				
DE	D1	PAD1	DE2	D2	PAD2	EN	PAD1	Y1	PAD2	Y2	GL
1	X	N/A	1	X	N/A	0	D1	D1	D2	D2	D1
1	X	N/A	1	X	N/A	1	D1	D1	D2	D2	D2
0	X	X	0	X	X	0	N/A	PAD1	N/A	PAD2	PAD1
0	X	X	0	X	X	1	N/A	PAD1	N/A	PAD2	PAD2
1	X	N/A	0	X	X	0	D1	D1	N/A	PAD2	D1
1	X	N/A	0	X	X	1	D1	D1	N/A	PAD2	PAD2
0	X	X	1	X	N/A	0	N/A	PAD1	D2	D2	PAD1
0	X	X	1	X	N/A	1	N/A	PAD1	D2	D2	D2

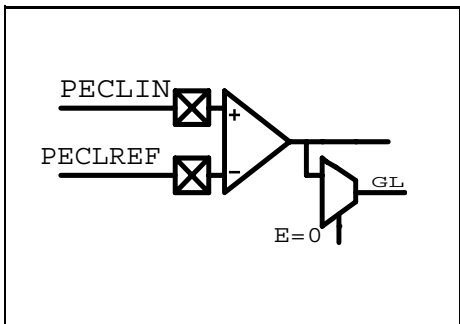
Input	Output
DE1, D1, PAD1, DE2, D2, PAD2, EN	PAD1, Y1, PAD2, Y2, GL

Available GLMIOBLx Macro Types

Name	Description
GLMX25LLU	2.5 Volt CMOS input levels, low power, low slew, w/ pull-up resistor
GLMX25LL	2.5 Volt CMOS input levels, low power, low slew
GLMX25LNU	2.5 Volt CMOS input levels, low power, normal slew, w/ pull up resistor
GLMX25LN	2.5 Volt CMOS input levels, low power, normal slew
GLMX25LHU	2.5 Volt CMOS input levels, low power, high slew, w/ pull-up resistor
GLMX25LH	2.5 Volt CMOS input levels, low power, high slew
GLMX25HLU	2.5 Volt CMOS input levels, high power, low slew, w/ pull-up resistor
GLMX25HL	2.5 Volt CMOS input levels, high power, low slew
GLMX25HNU	2.5 Volt CMOS input levels, high power, normal slew, w/ pull-up resistor
GLMX25HN	2.5 Volt CMOS input levels, high power, normal slew
GLMX25HHU	2.5 Volt CMOS input levels, high power, high slew, w/ pull-up resistor
GLMX25HH	2.5 Volt CMOS input levels, high power, high slew
GLMX25LPLLU	2.5 Volt CMOS input levels, low power, low strength, low slew, w/ pull-up resistor
GLMX25LPLL	2.5 Volt CMOS input levels, low power, low strength, low slew
GLMX25LPLNU	2.5 Volt CMOS input levels, low power, low strength, normal slew, w/ pull-up resistor
GLMX25LPLN	2.5 Volt CMOS input levels, low power, low strength, normal slew
GLMX25LPLHU	2.5 Volt CMOS input levels, low power, low strength, high slew, w/ pull-up resistor
GLMX25LPLH	2.5 Volt CMOS input levels, low power, low strength, high slew
GLMX25LPLHU	2.5 Volt CMOS input levels, low power, high strength, low slew, w/ pull-up resistor
GLMX25LPLH	2.5 Volt CMOS input levels, low power, high strength, low slew
GLMX25LPHN	2.5 Volt CMOS input levels, low power, high strength, normal slew
GLMX25LPHNU	2.5 Volt CMOS input levels, low power, high strength, normal slew, w/ pull-up resistor
GLMX25LPHHU	2.5 Volt CMOS input levels, low power, high strength, high slew, w/ pull-up resistor
GLMX25LPHH	2.5 Volt CMOS input levels, low power, high strength, high slew
GLMX33LLU	3.3 Volt CMOS input levels, low power, low slew, w/ pull-up resistor
GLMX33LL	3.3 Volt CMOS input levels, low power, low slew
GLMX33LNU	3.3 Volt CMOS input levels, low power, normal slew, w/ pull up resistor
GLMX33LN	3.3 Volt CMOS input levels, low power, normal slew
GLMX33LHU	3.3 Volt CMOS input levels, low power, high slew, w/ pull-up resistor
GLMX33LH	3.3 Volt CMOS input levels, low power, high slew
GLMX33PLU	3.3 Volt CMOS input levels, PCI compliant, low slew, w/ pull-up resistor
GLMX33PL	3.3 Volt CMOS input levels, PCI compliant, low slew
GLMX33PNU	3.3 Volt CMOS input levels, PCI compliant, normal slew, w/ pull-up resistor
GLMX33PN	3.3 Volt CMOS input levels, PCI compliant, normal slew
GLMX33PHU	3.3 Volt CMOS input levels, PCI compliant, high slew, w/ pull-up resistor
GLMX33PH	3.3 Volt CMOS input levels, PCI compliant, high slew

GLPE

APA

**Input**

PECLIN, PECLREF

Output

GL

Function

LVPECL inputs for high-speed signaling.

The GLPE macro reads the difference between the PECLIN and PECLREF analog signals and returns a voltage of 1 if it is above a (user-specified) threshold.

Truth Table

Input ^a		Output
PECLIN	PECLREF	GL
X	X	PECLIN

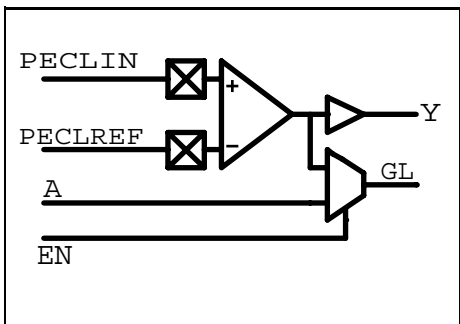
- a. This table describes digital model behavior for PECLIN and PECLREF

Tile Usage

Family	I/O Tiles
All listed	1

GLPEMIB

APA

**Input**

A, EN, PECLIN

Output

Y, GL

Function

LVPECL inputs for high-speed signaling.

The GLPEMIB macro reads the difference between the PECLIN and PECLREF analog signals and returns a voltage of 1 if it is above a (user-specified) threshold.

Truth Table

Input ^a			Output	
A	EN	PECLIN / PECLREF	GL	Y
X	0	X	PECLIN/PECLREF	PECLIN/PECLREF
X	1	X	A	PECLIN/PECLREF

- a. This table describes digital model behavior for PECLIN and PECLREF

Tile Usage

Family	I/O Tiles
All listed	1

Memory Cells

Embedded memory blocks in the A500K family can be configured as FIFO or static RAM with the following features:

- basic block size is 256 word by 9 bit.
- FIFO includes complete control logic.
- static RAM with independent read and write ports.

Naming Convention for RAMs

RAM model names consist of up to four parts:

- A base name indicating the type and size (RAM256x9)
- A one character code designating the write port as asynchronous (A) or synchronous (S).
- A one or two character code designating the read port as asynchronous (A) or synchronous registered (SR) or synchronous transparent (ST).
- An optional one character code designating parity (P) generated.

For example: RAM256x9SAP is a 256-word by 9-bit RAM with synchronous write and asynchronous read ports using the generate parity feature.

SRAM Interface Signals

The illustration and table below describe basic embedded SRAM interface signals.

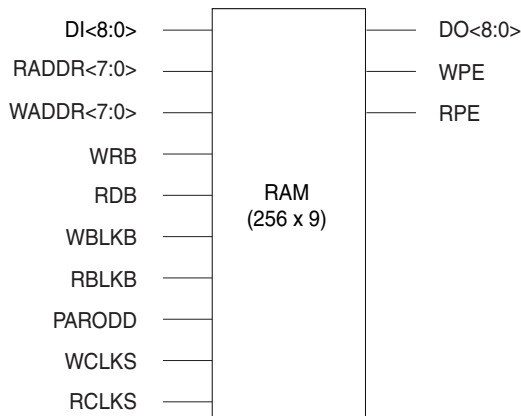


Table 4-1: SRAM Signal Descriptions

SRAM Signal	Bits	In/Out	Description
DI<8:0>	9	IN	Input data bits <8:0>, <8> can be used for parity in
RADDR<7:0>	8	IN	Read address
WADDR<7:0>	8	IN	Write address
WRB	1	IN	Negative true write pulse
RDB	1	IN	Negative true read pulse
WBLKB	1	IN	Negative true write block select
RBLKB	1	IN	Negative true read block select
PARODD	1	IN	Selects odd parity generation/detect when high, even when low
WCLKS	1	IN	Write clock used in synchronous mode on write side
RCLKS	1	IN	Write clock used in synchronous mode on read side
DO<8:0>	9	OUT	Output data bits <8:0>, <8> can be used for parity out
WPE	1	OUT	Write parity error flag
RPE	1	OUT	Read parity error flag

Naming Convention for FIFOs

FIFO model names consist of up to four parts:

- A base name indicating the type and size (FIFO256x9)
- A one character code designating the write port as asynchronous (A) or synchronous (S).
- A one or two character code designating the read port as asynchronous (A) or synchronous registered (SR) or synchronous transparent (ST).
- An optional one character code designating parity (P) generated.

For example: FIFO256x9SSRP is a 256-word by 9-bit FIFO with synchronous write and synchronous read ports (synchronous to separate clocks named RCLKS and WCLKS), has registered outputs and uses the generate parity feature.

FIFO Interface Signals

This illustration and the table below describe FIFO interface signals.

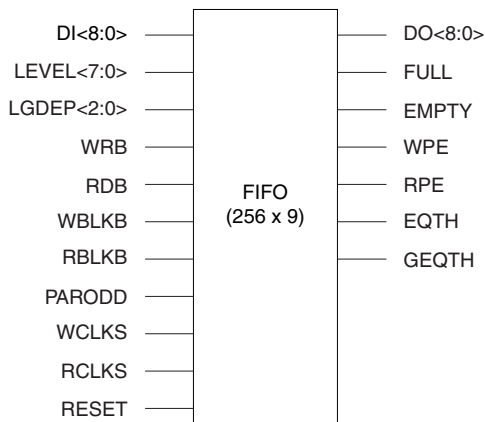
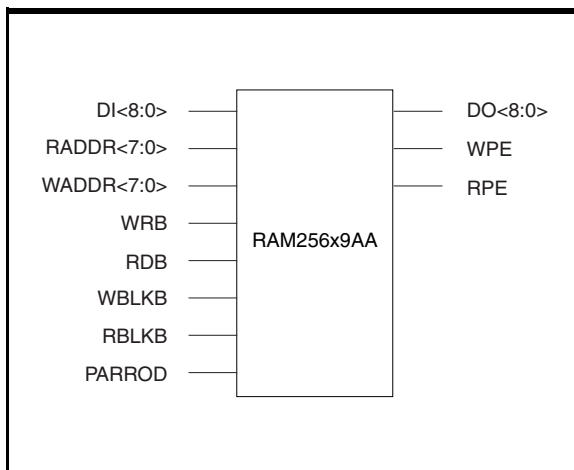


Table 4-2: FIFO Signal Descriptions

FIFO Signal	Bits	In/Out	Description
DI<8:0>	9	IN	Input data bits <8:0>, <8> can be used for parity in
LEVEL<7:0>	8	IN	Reference signal for the generation of the EQTH and GEQTH flags
LGDEP<2:0>	3	IN	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
WRB	1	IN	Negative true write pulse
RDB	1	IN	Negative true read pulse
WBLKB	1	IN	Negative true write block select
RBLKB	1	IN	Negative true read block select
PARODD	1	IN	Selects odd parity generation/detect when high, even when low
WCLKS	1	IN	Write clock used in synchronous mode on write side
RCLKS	1	IN	Write clock used in synchronous mode on read side
RESET	1	IN	Negative true reset for FIFO pointers
DO<8:0>	9	OUT	Output data bits <8:0>, <8> can be used for parity out
FULL	2	OUT	FIFO flag. FULL prevents write. EMPTY prevents read
EMPTY	1	OUT	FIFO flag. EMPTY prevents read
WPE	1	OUT	Write parity error flag
RPE	1	OUT	Read parity error flag
EQTH	1	OUT	EQTH is true when the FIFO holds (LEVEL) words
GEQTH	1	OUT	GEQTH is true when the FIFO holds (LEVEL) words or more

RAM256x9AA**A500K, APA****Function**

Asynchronous Write/Asynchronous Read RAM with Parity Checking

Tile Usage

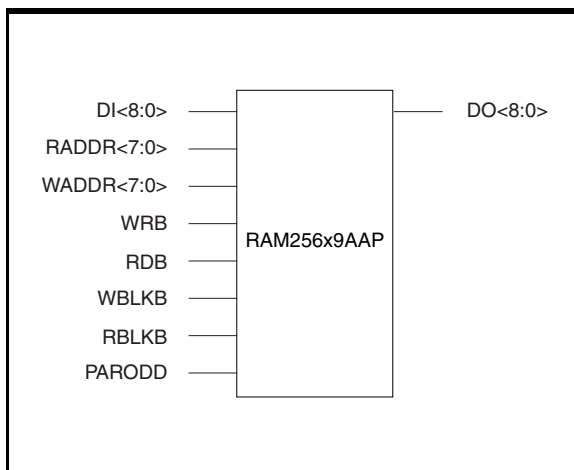
Family	RAM Port Tiles
All listed	16

Input

DI, RADDR, WADDR,
WRB, RDB, WBLKB,
RBLKB, PARROD

Output

DO, WPE, RPE

RAM256x9AAP**A500K, APA****Function**

Asynchronous Write/Asynchronous Read RAM with Parity Generation

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

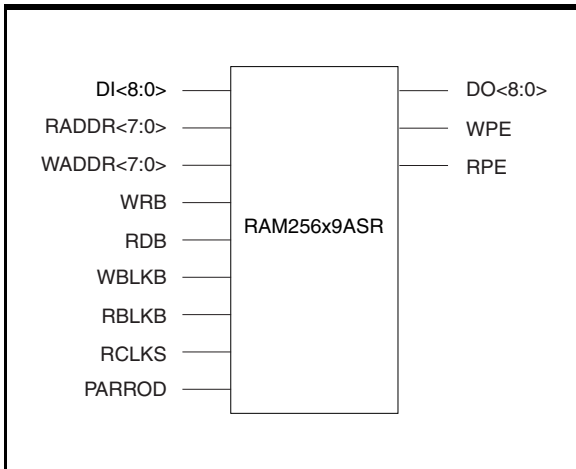
DI, RADDR, WADDR,
WRB, RDB, WBLKB,
RBLKB, PARROD

Output

DO

RAM256x9ASR

A500K, APA

**Function**

Asynchronous Write/Synchronous Read RAM with Registered Output and Parity Checking

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

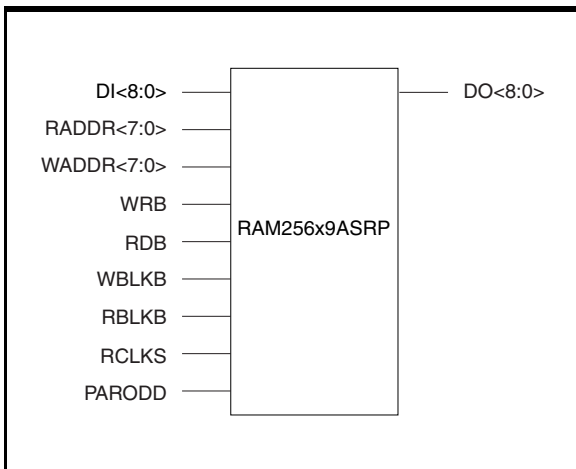
DI, RADDR, WADDR,
WRB, RDB, WBLKB,
RBLKB, RCLKS, PARROD

Output

DO, WPE, RPE

RAM256x9ASRP

A500K, APA

**Function**

Asynchronous Write/Synchronous Read RAM with Registered Output and Parity Generation

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

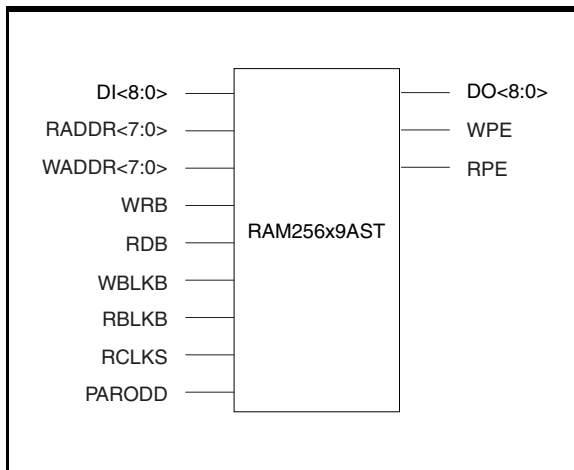
DI, RADDR, WADDR,
WRB, RDB, WBLKB,
RBLKB, RCLKS, PARROD

Output

DO

RAM256x9AST

A500K, APA

**Function**

Asynchronous Write/Synchronous Read RAM with Transparent Output and Parity Checking

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

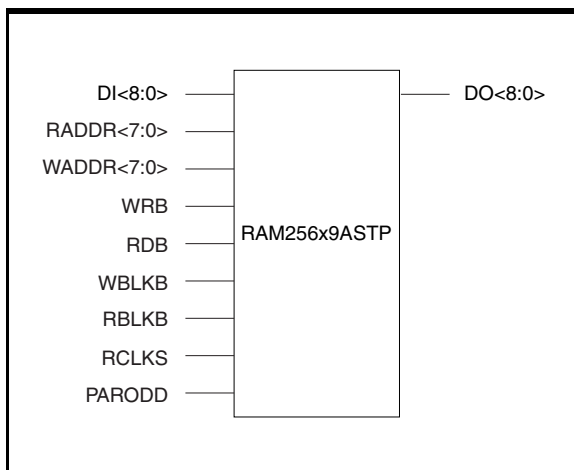
DI, RADDR, WADDR,
WRB, RDB, WBLKB,
RBLKB, RCLKS, PARODD

Output

DO, WPE, RPE

RAM256x9ASTP

A500K, APA

**Function**

Asynchronous Write/Synchronous Read RAM with Transparent Output and Parity Generation

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

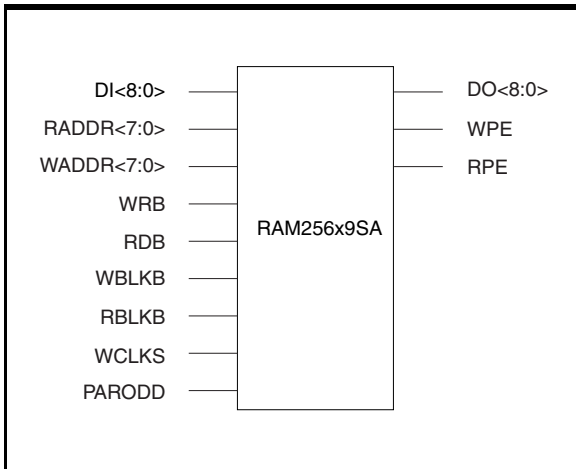
DI, RADDR, WADDR,
WRB, RDB, WBLKB,
RBLKB, RCLKS, PARODD

Output

DO

RAM256x9SA

A500K, APA

**Function**

Synchronous Write/Asynchronous Read RAM with Parity Checking

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

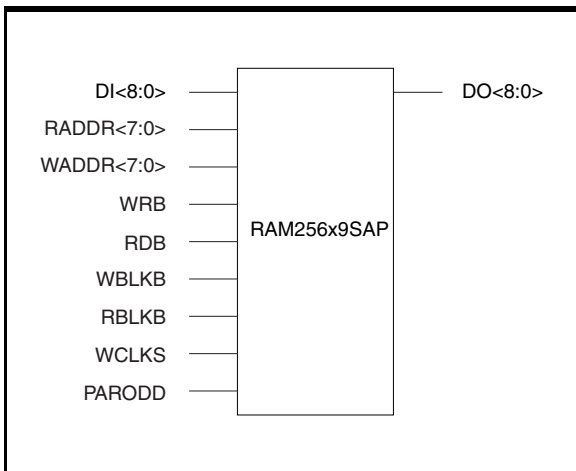
DI, RADDR, WADDR,
WRB, RDB, WBLKB,
RBLKB, WCLKS, PAROD

Output

DO, WPE, RPE

RAM256x9SAP

A500K, APA

**Function**

Synchronous Write/Asynchronous Read RAM with Parity Generation

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

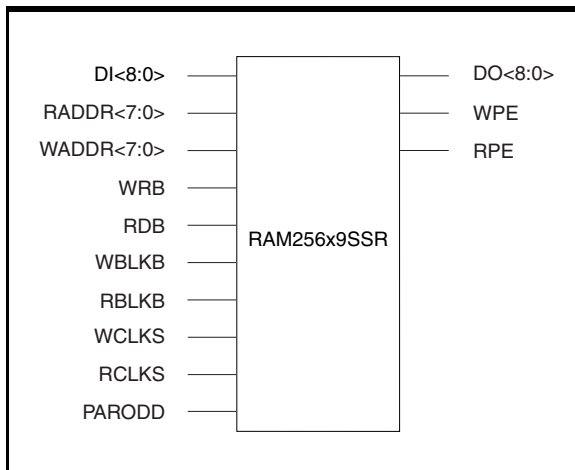
DI, RADDR, WADDR,
WRB, RDB, WBLKB,
RBLKB, WCLKS, PAROD

Output

DO

RAM256x9SSR

A500K, APA

**Function**

Synchronous Write/Synchronous Read RAM with Registered Output and Parity Checking

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

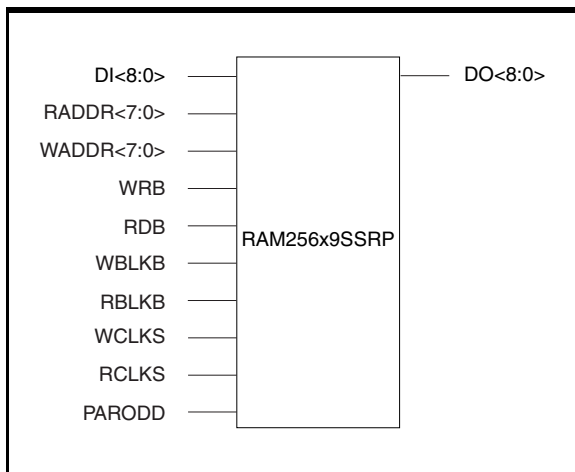
DI, RADDR, WADDR,
WRB, RDB, WBLKB,
RBLKB, WCLKS, RCLKS,
PARROD

Output

DO, WPE, RPE

RAM256x9SSRP

A500K, APA

**Function**

Synchronous Write/Synchronous Read RAM with Registered Output and Parity Generation

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

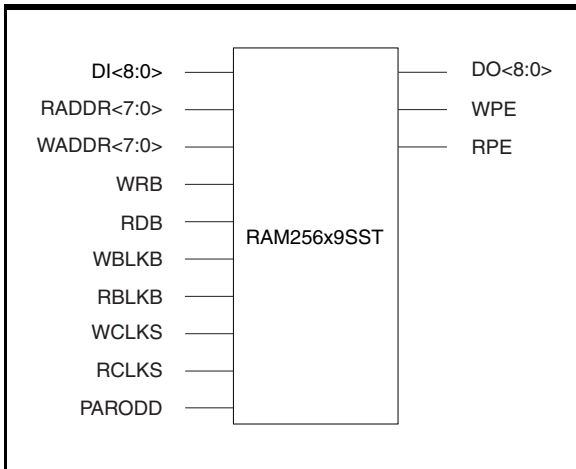
DI, RADDR, WADDR,
WRB, RDB, WBLKB,
RBLKB, WCLKS, RCLKS,
PARROD

Output

DO

RAM256x9SST

A500K, APA

**Function**

Synchronous Write/Synchronous Read RAM with Transparent Output and Parity Checking

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

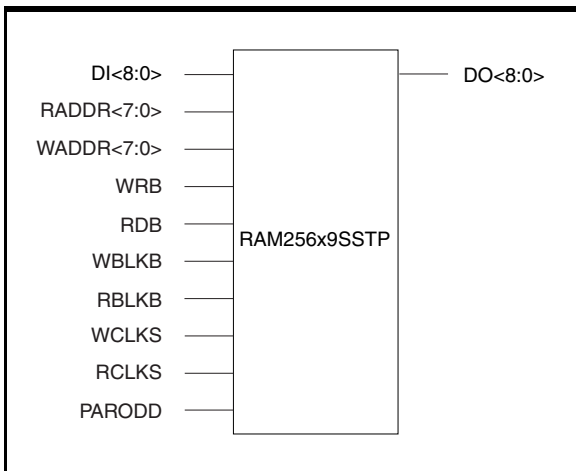
DI, RADDR, WADDR,
WRB, RDB, WBLKB,
RBLKB, WCLKS, RCLKS,
PARROD

Output

DO, WPE, RPE

RAM256x9SSTP

A500K, APA

**Function**

Synchronous Write/Synchronous Read RAM with Transparent Output and Parity Generation

Tile Usage

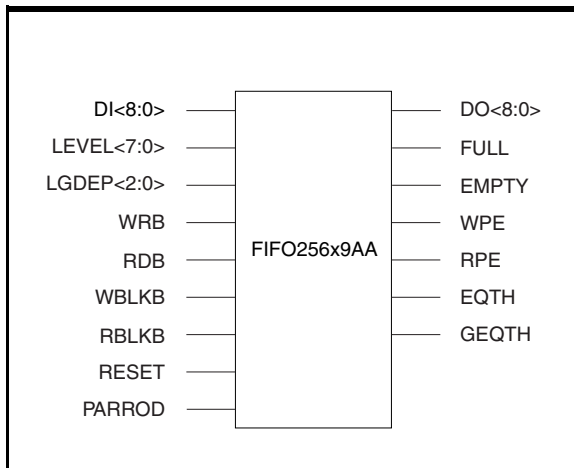
Family	RAM Port Tiles
All listed	16

Input

DI, RADDR, WADDR,
WRB, RDB, WBLKB,
RBLKB, WCLKS, RCLKS,
PARROD

Output

DO

FIFO256x9AA**A500K, APA****Function**

Asynchronous Write/Asynchronous Read FIFO with Parity Checking

Tile Usage

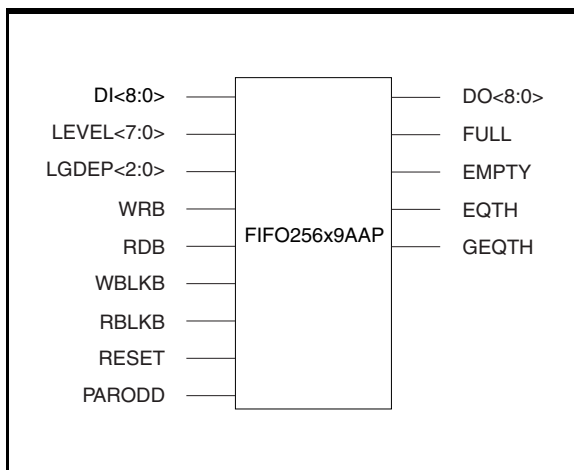
Family	RAM Port Tiles
All listed	16

Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, RESET, PARROD

Output

DO, FULL, EMPTY, WPE, RPE, EQTH, GEQTH

FIFO256x9AAP**A500K, APA****Function**

Asynchronous Write/Asynchronous Read FIFO with Parity Generation

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

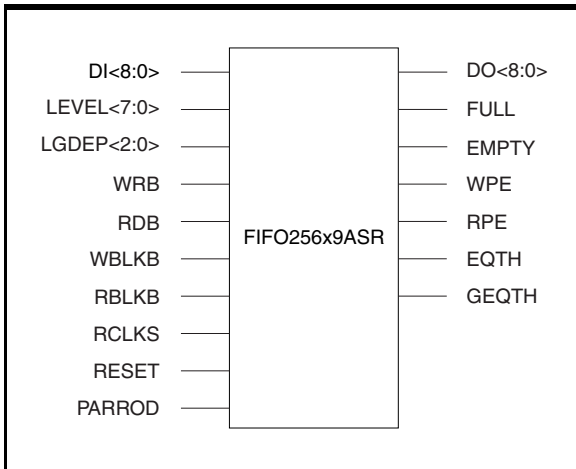
DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, RESET, PARROD

Output

DO, FULL, EMPTY, EQTH, GEQTH

FIFO256x9ASR

A500K, APA

**Function**

Asynchronous Write/Synchronous Read FIFO with Registered Output and Parity Checking

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

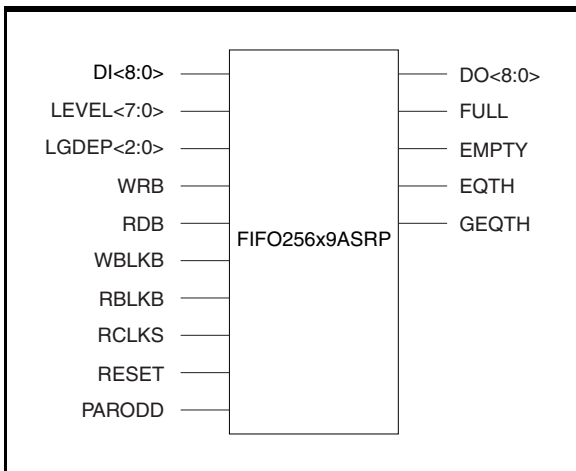
DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, RCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, WPE, RPE, EQTH, GEQTH

FIFO256x9ASRP

A500K, APA

**Function**

Asynchronous Write/Synchronous Read FIFO with Registered Output and Parity Generation

Tile Usage

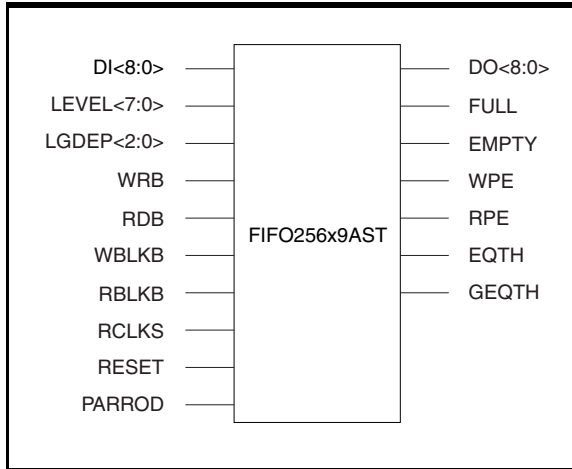
Family	RAM Port Tiles
All listed	16

Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, RCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, EQTH, GEQTH

FIFO256x9AST**A500K, APA****Function**

Asynchronous Write/Synchronous Read FIFO with Transparent Output and Parity Checking

Tile Usage

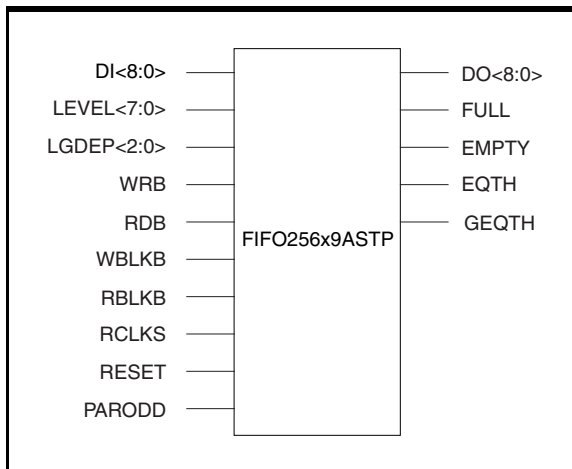
Family	RAM Port Tiles
All listed	16

Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, RCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, WPE, RPE, EQTH, GEQTH

FIFO256x9ASTP**A500K, APA****Function**

Asynchronous Write/Synchronous Read FIFO with Transparent Output and Parity Generation

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

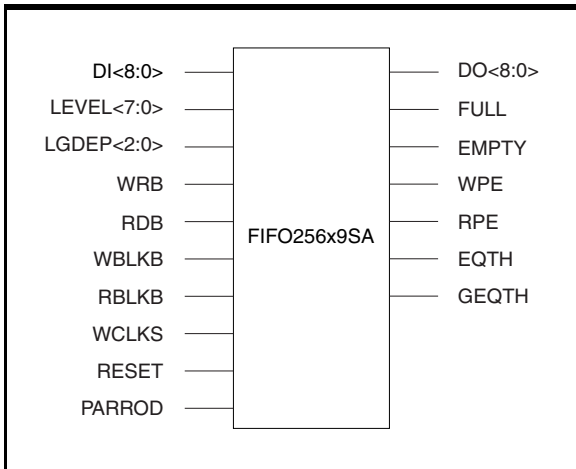
DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, RCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, EQTH, GEQTH

FIFO256x9SA

A500K, APA

**Function**

Synchronous Write/Asynchronous Read FIFO with Parity Checking

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

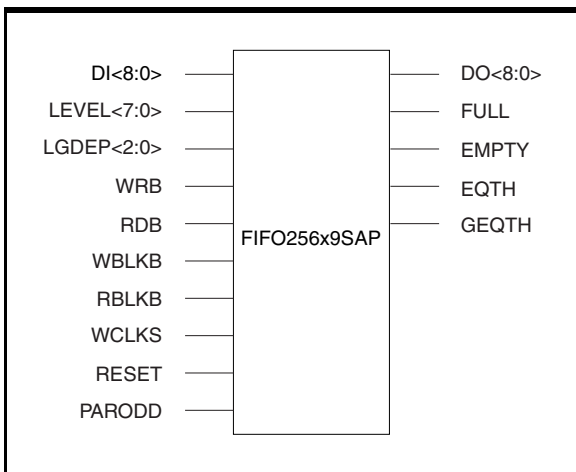
DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, WCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, WPE, RPE, EQTH, GEQTH

FIFO256x9SAP

A500K, APA

**Function**

Synchronous Write/Asynchronous Read FIFO with Parity Generation

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

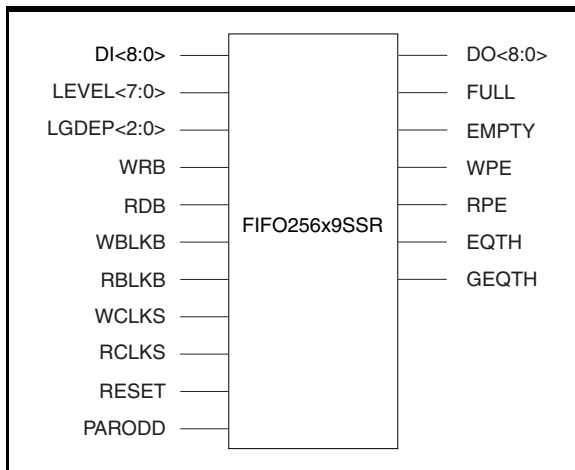
DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, WCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, EQTH, GEQTH

FIFO256x9SSR

A500K, APA

**Function**

Synchronous Write/Synchronous Read FIFO with Registered Output and Parity Checking

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

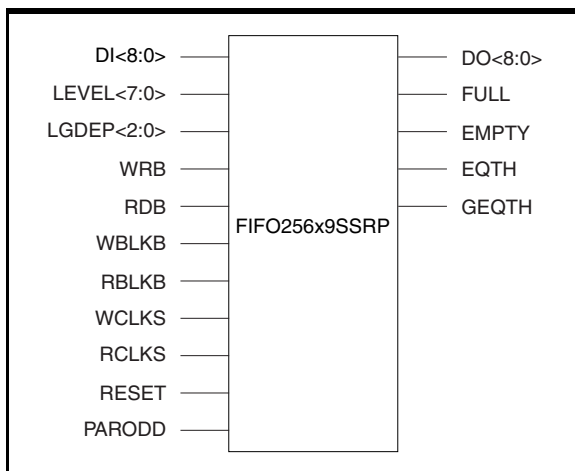
DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, WCLKS, RCLKS, RESET, PARODD

Output

DO, FULL, EMPTY, WPE, RPE, EQTH, GEQTH

FIFO256x9SSRP

A500K, APA

**Function**

Synchronous Write/Synchronous Read FIFO with Registered Output and Parity Generation

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

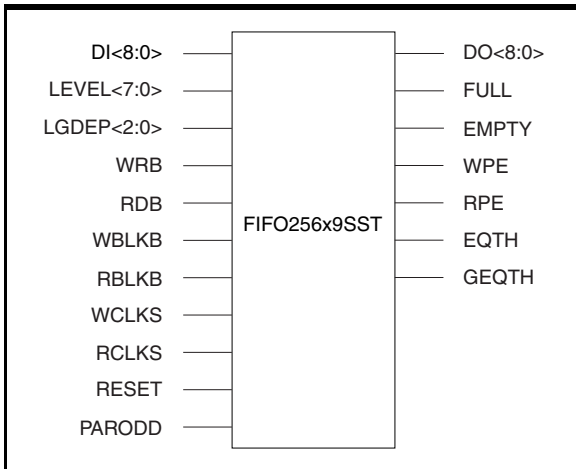
DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, WCLKS, RCLKS, RESET, PARODD

Output

DO, FULL, EMPTY, EQTH, GEQTH

FIFO256x9SST

A500K, APA

**Function**

Synchronous Write/Synchronous Read FIFO with Transparent Output and Parity Checking

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

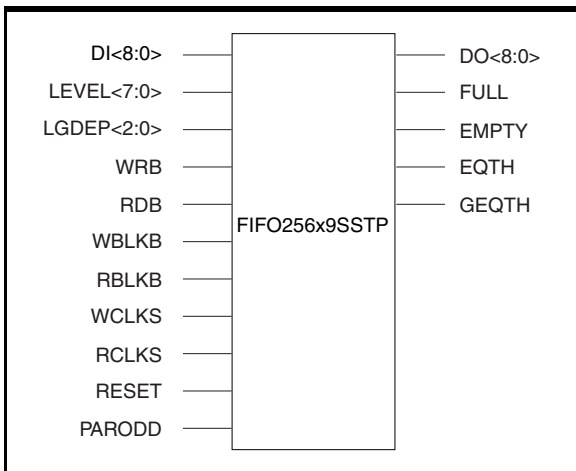
DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, WCLKS, RCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, WPE, RPE, EQTH, GEQTH

FIFO256x9SSTP

A500K, APA

**Function**

Synchronous Write/Synchronous Read FIFO with Transparent Output and Parity Generation

Tile Usage

Family	RAM Port Tiles
All listed	16

Input

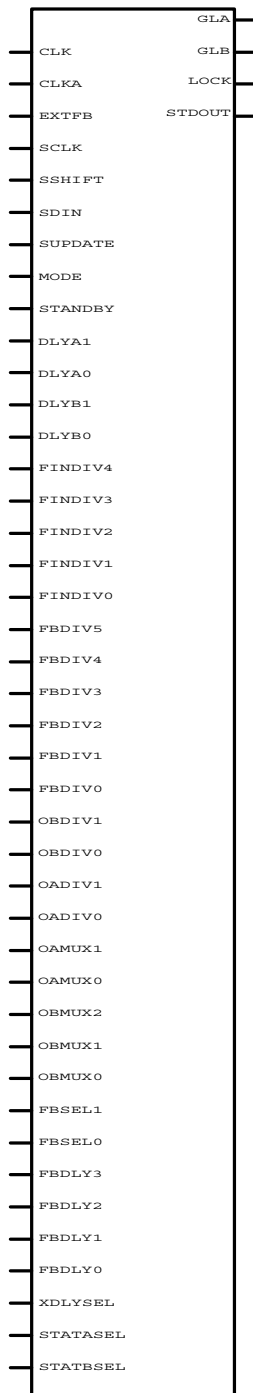
DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, WCLKS, RCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, EQTH, GEQTH

PLLCORE

APA



Function

Phase locked loop; please refer to PLL and APA datasheets for more information on the PLL.

Tile Usage

Family	I/O Tiles
All listed	6

Product Support

Actel backs its products with various support services including Customer Service, a Customer Applications Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature about Actel and Actel products, Customer Service, investor information, and using the Action Facts service.

The Actel toll-free line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for nontechnical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480.

From Southeast and Southwest U.S.A., call (408) 522-4480.

From South Central U.S.A., call (408) 522-4434.

From Northwest U.S.A., call (408) 522-4434.

From Canada, call (408) 522-4480.

From Europe, call (408) 522-4252 or +44 (0) 1256 305600.

From Japan, call (408) 522-4743.

From the rest of the world, call (408) 522-4743.

Fax, from anywhere in the world (408) 522-8044.

Customer Applications Center

Actel staffs its Customer Applications Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Applications Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your question(s).

Guru Automated Technical Support

Guru is a web-based automated technical support system accessible through the Actel home page (<http://www.actel.com/guru/>). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations, and links to other resources on the Actel web site. Guru is available 24 hours a day, seven days a week.

Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and nontechnical information. Use a Net browser (Netscape recommended) to access Actel's home page.

The URL is <http://www.actel.com>. You are welcome to share the resources provided on the Internet.

Be sure to visit the Technical Documentation area on our web site, which contains information regarding products, technical services, current manuals, and release notes.

You can visit the Product Support area of the Actel website from your Designer software. Click the Product Support button in your Designer Main Window to access the latest datasheets, application notes, and more.

FTP Site

Actel has an anonymous FTP site located at **ftp://ftp.actel.com**. Here you can obtain library updates, software patches, design files, and data sheets.

Contacting the Customer Applications Center

Highly skilled engineers staff the Customer Applications Center from 7:30 A.M. to 5:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. We constantly monitor the e-mail account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support e-mail address is **tech@actel.com**.

Telephone

Our Technical Message Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:30 A.M. to 5:00 A.M., Pacific Time, Monday through Friday.

The Customer Applications Center number is (800) 262-1060.

European customers can call +44 (0) 1256 305600.

Worldwide Sales Offices

Headquarters

Actel Corporation
955 East Arques Avenue
Sunnyvale, California 94086
Toll Free: 888.99.ACTEL

Tel: 408.739.1010
Fax: 408.739.1540

US Sales Offices

California

Bay Area
Tel: 408.328.2200
Fax: 408.328.2358

Irvine
Tel: 949.727.0470
Fax: 949.727.0476

Newbury Park
Tel: 805.375.5769
Fax: 805.375.5749

Colorado

Tel: 303.420.4335
Fax: 303.420.4336

Florida

Tel: 407.977.6846
Fax: 407.977.6847

Georgia

Tel: 770.277.4980
Fax: 770.277.5896

Illinois

Tel: 847.259.1501
Fax: 847.259.1575

Massachusetts

Tel: 978.244.3800
Fax: 978.244.3820

Minnesota

Tel: 651.917.9116
Fax: 651.917.9114

New Jersey

Tel: 609.517.0304

North Carolina

Tel: 919.654.4529
Fax: 919.674.0055

Pennsylvania

Tel: 215.830.1458
Fax: 215.706.0680

Texas

Tel: 972.235.8944
Fax: 972.235.965

International Sales Offices

Canada

235 Stafford Rd. West,
Suite 106
Nepean, Ontario K2H 9C1

Tel: 613.726.7575
Fax: 613.726.8666

France

Actel Europe S.A.R.L.
361 Avenue General de Gaulle
92147 Clamart Cedex

Tel: +33 (0)1.40.83.11.00
Fax: +33 (0)1.40.94.11.04

Germany

Lohweg 27
85375 Neufahrn
Tel: +49 (0)8165.9584.0
Fax: +49 (0)8165.9584.1

Italy

Via de Garibaldini, No. 5
20019 Settimo Milanese,
Milano, Italy

Japan

EXOS Ebisu Building 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150

Tel: +81 (0)3.3445.7671
Fax: +81 (0)3.3445.7668

Korea

30th Floor, ASEM Tower,
159-1 Samsung-dong,
Kangam-ku,
Seoul, Korea

Tel: +82.2.6001.3382
Fax: +82.2.6001.3030

United Kingdom

Maxfli Court,
Riverside Way
Camberley,
Surrey GU15 3YL

Tel: +44 (0)1276.401452
Fax: +44 (0)1276.401490