ASICmaster™ Pro/Lite Pre-production Version 5.1 Release Notes - June1999

This document describes the new features, enhancements and release-specific details of pre-production Version 5.1 of ASICmaster Pro/Lite. In addition to information regarding known limitations, it explains how the A500K family is supported through ASICmaster Pro and associated design kits in Verilog, VHDL, Exemplar and Synopsys design environments.

Introduction

The pre-production V5.1 release supports the new A500K family of 0.25µ ProASIC™ devices with integrated embedded memory blocks. This family offers access to high density devices, up to 1,000,000 system gates, and the industry's most advanced and flexible programmable embedded memory (up to 63K bits). Programming options include synchronous or asynchronous read and write operations, multiple port access configurations, true FIFO capability, user specified depth and width, and parity mode selection.

Refer to the *ASICmaster User's Guide*, *ProASIC Interface Guide*, *ProASIC Macro Library Guide*, *MEMORYmaster User's Guide*, and the *ProASIC A500K Family Data Sheet* for additional information. Documentation is available in .pdf format on the installation CD.

New Features and Enhancements

This section lists the new features and enhancements of the ASICmaster™ Pro/Lite pre-production Version 5.1 release.

Support for A500K Devices

This release supports the following ProASIC A500K family of devices:

A500K270 (PQ208 and BG456 packages)

Maximum 442 I/O pads, 4 global I/O pads, 26880 core logic tiles, 28 embedded memory blocks each of 256x9 bits.

A500K180 (PQ208 and BG456 packages)

Maximum 364 I/O pads, 4 global I/O pads, 18432 core logic tiles, 24 embedded memory blocks each of 256x9 bits.

A500K130 (PQ208, BG456, and BG272 packages)

Maximum 308 I/O pads, 4 global I/O pads, 12800 core logic tiles, 20 embedded memory blocks each of 256x9 bits.

A500K050 (PQ208 and BG272 packages)

Maximum 206 I/O pads, 4 global I/O pads, 5376 core logic tiles, 6 embedded memory blocks each of 256x9 bits.

Support for A500K Memories

This release allows memory generation using embedded memory resources as well as distributing memories within the core logic area.

The ability to create distributed or embedded RAMs and FIFOs is fully described in the *MEMORYmaster User's Guide*.

Timing Driven Engine

The Timing Driven option allows use of timing driven placement. To take full advantage of this, post-synthesis SDF timing budgets (PATHCONSTRAINTS constructs) should be submitted to ASICmaster as an additional constraint file. The placer will use this information to improve the timing along those paths, which do not have slack.

Also the router will take into account constraints on critical nets, as specified in "set_critical" constraint statements.

Placement Refinement Engine

The Placement Refinement feature allows processing of an ECO (Engineering Change Order) on an existing placement. This feature assumes that the user has provided a constraint file, which contains an initial placement, and wants to adjust for changes in the netlist or constraints.

When the placement task is finished, the system always produces a constraints file in the design directory: "<design>.dtf/last_placement.gcf". This file contains all information about placement constraints. Blocks with fixed placement constraints regenerate fixed placement constraints while the others generate initial placement constraints. Users can edit the existing constraints files to remove any prior placement constraints and copy the last_placement.gcf file one level up and add it to the list of constraints files.

Incremental Routing

The tool performs an initial routing, where it may repeat existing routes if the Incremental Routing feature is turned on. It then checks for any unrouted nets and, if necessary, performs several passes in which it allows shorting of nets to determine which nets are competing for particular resources. This process continues until a satisfactory solution is found.

If routing completion is not achieved, users have the option of starting a new routing run in Incremental Routing mode. When a previous result finishes with a small number (<=20) of shorted segments, Actel recommends running the routing task again using this new incremental feature.

Licensing

In release V5.1, we have migrated to Version 5 license keys.

2 daemons must be run: gfdaemon and CLKCAD.

The current release uses FLEXlm version 6.0 from Globetrotter Software.

Licensing checks are now performed during place and route only. This means that a license is no longer needed to program a part.

For V5.1 of ASICmaster Pro, you now can set your AM_LIC_FILE environment variable to <socket_number>@<hostname>, where socket_number is the last number on the SERVER line of your license file and hostname is the name following the SERVER keyword in the same file.

Sample license file:

```
#
#FLEXlm license file for hostid 721012d0:
#
SERVER pericles 721012d0 1702
DAEMON GATEFLD /ASICmaster/exe/sun5/gfdaemon
DAEMON CLKCAD /ASICmaster/exe/sun5/CLKCAD
FEATURE FPGA_GF_PLACE CLKCAD 1.01 31-dec-1999 50 84D65561786E
FEATURE ampro GATEFLD 5.0 31-dec-1999 100 DBFFCBEB28B4 ck=140
```

To access this license use the following:

```
setenv AM_LIC_FILE 1702@pericles
```

Power Estimation Tool

The new Estimate Power tool is available under the Tasks Menu.

When estimating power, user's can enter data about the device output and logic of the design. This tool also allows calculation of the junction temperature as a function of power dissipation, the device package, and the device environment.

Note that the power calculation uses a worst case approach and uses VDDL as 2.75V while VDDP is user selectable between 3.63V and 2.75V.

Junction temperatures above 110°C are marked red, because the A500K devices are not guaranteed to work at temperatures above 110°C. The junction to ambient thermal resistance (Θ_{ja}) is shown and depends on the package used, the airflow and the heatsink reduction factor. If the value was the result of interpolation it is shown in brown, otherwise it is shown in black.

Automatic Placement of Embedded Memories

Embedded memories, generated by MEMORYmaster, are automatically placed by the checker.

Specification of individual embedded memory placement is also possible through the set_location command. The checker will then make sure this placement is appropriate.

Regional Placement of Subcircuits

The constraint command set_location accepts a window, rather than a single tile and a wildcard name. This allows definition of a design floorplan.

```
set_location (x_bl, y_bl x_tr, y_tr)   hier_name_wildcard;
```

where

x_{bl}. y_{bl}, x_{tr}, y_{tr}	(required) are the x, y tile coordinates for the bottom left and top right corner of the region.
hier_name_wildcard	(required) is the hierarchical path wild card to cell instances. Only simple wild carding is supported: "?" stands for one character and "*" stands for zero to many characters.

For example:

```
set_location (1,1 12,16) u4/u3/*;
```

Known Limitations

The following limitations are known to exist in this ASICmaster Pro/Lite V5.1 release.

I/O Pad Timing Calculation

ASICmaster may calculate longer I/O pad intrinsic delays and drive impedances than those found in actual device I/O delays.

At the time of this release, qualification continues to explore the process corners to determine more typical I/O timing data.

BG456 Package on the A500K270 Device

When you select A500K270-BG456 as part, you need to add the following constraint:

```
set_empty_io W 69;
```

This is because the current data in this release define a pin named W66 as location W69, which does not exist on the package.

Default Voltage Range Values For Industrial Grade Devices

When you select an industrial grade device, the default voltage range used in Design Options is set erroneously between 2.0 to 3.0 V. The voltage range should not change between industrial and commercial grade devices and is always between 2.3 and 2.7 V. As a work-around, you can manually set the voltage range to the correct range.

Default Button for Industrial Grade Devices

The default button in the Design Options window always defaults to Industrial grade instead of the selected grade. Do not press this button and the ranges will remain as the grade of the part you selected.

MEMORYmaster May Write Out Lines Longer Than 255 Characters.

MEMORYmaster currently may write out lines longer than 255 characters. This may cause problems in simulators that can only handle 255 characters per line.

False Timing Violation In VHDL RAM/ FIFO Simulation

When you check RCLK/WCLK setup/hold in sync/sync mode match, even if the RCLK edge was not for an active read (i.e. RDB and RBLKB both 0), you still get a violation, which should be disregarded.

Verilog RAM Model Does Not Compile In ModelSim.

The ram primitive for Verilog does not compile with ModelSim Vlog. It seems the setups for EMPTY/FULL use registered values for internal signals.

The error message says...

```
must use ports for setup and conditional signals must be
nets...
```

Global I/O Pad Pull-up Resistors Are Reversed

When the Global I/O pads are used, they will have the pull-up resistor enabled by default. If a Global Pad is specified in the netlist with a pull-up (e.g., GL33U), the resulting bitstream will not have a pull-up on that Global I/O.

As a work-around, specify the Global Pad without a pull-up if one is desired. If no pull-up is desired, specify the Global pad with a pull-up. For unused global pads, grounding the global pads is also acceptable.

Documentation

Documents on the CD are pre-production versions. Check the User's area on the Actel web site (http://www.actel.com/user) for more information.

The *ProASIC Interface Guide* is available in the User's area on the Actel web site (http://www.actel.com/user)