Revision History

Date	ECO#	Description	Sheet	Initiater	Approval
08/11/04	0.3	Capture the full schematic	1 to 10	Actel	
08/13/04	0.4	Added the LCD MODULE INTERFACE CIRCUIT LCD POWER SUPPLY CIRCUIT LVDS SIGNAL ROUTING VIA CAT-5E CONNECTORS	3,9,10	Sanmina-SCI	
08/16/04	0.5	Schematic changed on	10,5	Sanmina-SCI	
08/20/04	0.6	Changed the LCD MODULE INTERFACE CIRCUIT AND LVDS SIGNAL ROUTING VIA CAT-5E CONNECTORS	3,4	Sanmina-SCI	
08/26/04	0.7	Schematic changed on	3,4,6	Sanmina-SCI	
08/27/04	0.8	Schematic changed on	2,3,6,7,10	Sanmina-SCI	
08/28/04	0.9	Schematic changed on	2,8	Sanmina-SCI	
09/03/04	1.0	Schematic changed on	2,3,4,5,6,7,8,9,10	Sanmina-SCI	
09/04/04	1.1	Schematic changed on	6,8	Sanmina-SCI	
09/06/04	1.2	Schematic changed on	1,2,3,4,5,6,7,8,9,10	Sanmina-SCI	
09/07/04	1.3	Schematic changed on	2,4,6,7,8	Sanmina-SCI	
09/07/04	1.4	Schematic changed on	10	Sanmina-SCI	
09/08/04	1.5	Schematic changed on	1,2,10	Sanmina-SCI	
09/09/04	1.6	Schematic changed on	6,8	Sanmina-SCI	
09/20/04	1.7	Bom Changed on	1,2,3,4,5,6,7,8,9,10	Sanmina-SCI	
09/24/04	1.8	Schematic changed on	5	Sanmina-SCI	
02/18/05	2.0	Schematic changed on	3,4,6,7	Sanmina-SCI	
02/22/05	2.1	Schematic changed on	2,4,6,7,10	Sanmina-SCI	
02/24/05	2.2	Schematic changed on	1,2,3,4,5,6,7,8,9,10	Sanmina-SCI	
03/07/05	2.3	Schematic changed on	3,5,6,7,10	Sanmina-SCI	
03/10/05	2.4	Schematic changed on	7,10	Sanmina-SCI	
04/05/05	3.0	Schematic changed on	8	Sanmina-SCI	

ProASIC3/E STARTER KIT BOARD

Actel Corp
2061 Stierlin Ct
Mountain View, CA 94043

ProASIC3/E STARTER KIT BOARD
A3PE-EVAL-BRD600-SA

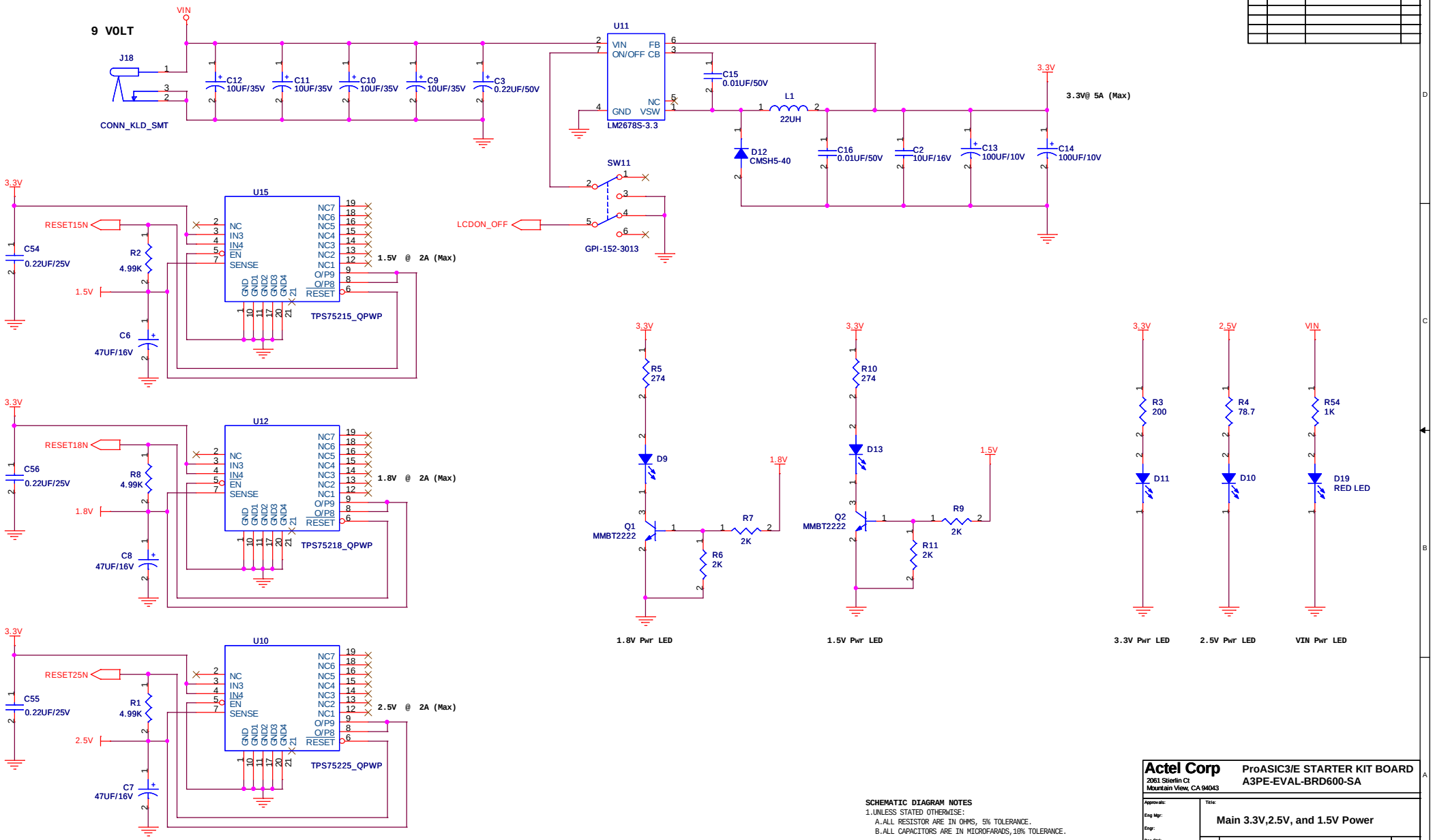
Approved:
Eng Mgr:
Engr:
Doc Ctrl:
Assembly

Title: ProASIC3/E STARTER KIT BOARD

Size: Document No: Sanmina-SCI Rev: 3.0

Date: 03/11/05 DRAWN BY:

Sheet 1 of 10



Revision History			
ECO#	Approval	Description	Date

SCHEMATIC DIAGRAM NOTES

1. UNLESS STATED OTHERWISE:
   A. ALL RESISTOR ARE IN OHMS, 5% TOLERANCE.
   B. ALL CAPACITORS ARE IN MICROFARADS, 10% TOLERANCE.

BOARD INFORMATION

PCB FAB:,REV.02 PCB ASSEMBLY:,REV.02

Actel Corp
2061 Stierlin Ct
Mountain View, CA 94043

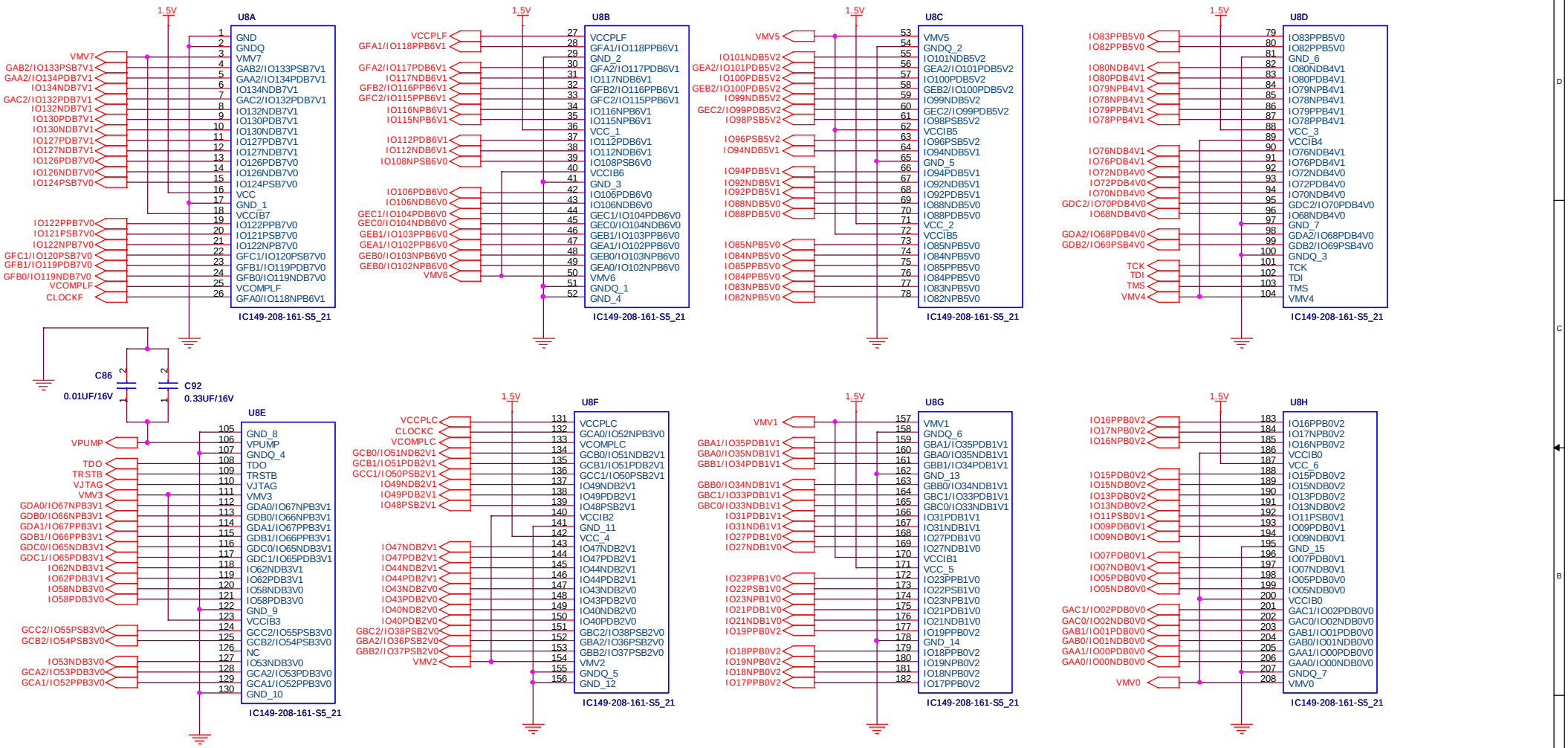
ProASIC3/E STARTER KIT BOARD
A3PE-EVAL-BRD600-SA

Approvals:
Eng Mgr:
Engr:
Doc Cntl:
Assembly

Title: **Main 3.3V,2.5V, and 1.5V Power**

Size: B | Document No: | Rev 3.0

Date: 03/11/05 | DRAWN BY: Sanmina-SCI | Pg 2 of 10



SCHEMATIC DIAGRAM NOTES

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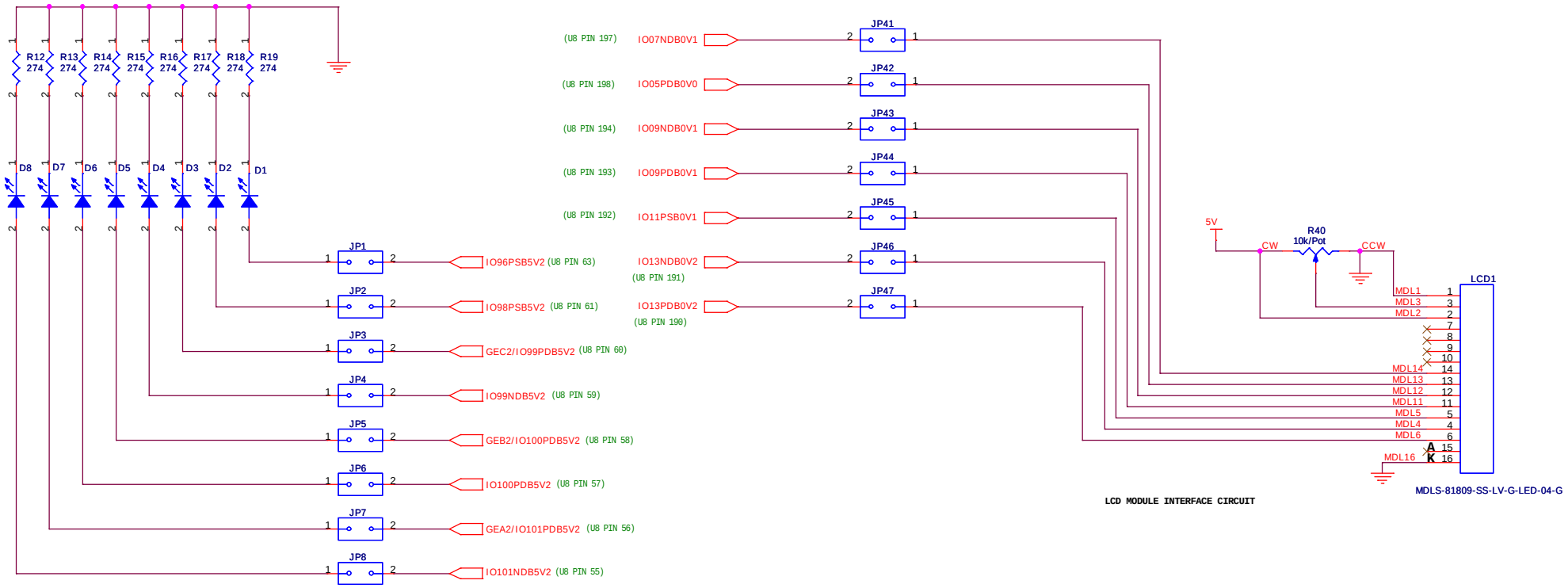
BOARD INFORMATION

PCB FAB:,REV.02 PCB ASSEMBLY:,REV.02

Actel Corp 2061 Stierlin Ct Mountain View, CA 94043	ProASIC3/E STARTER KIT BOARD A3PE-EVAL-BRD600-SA
Approvals:	Title: ProASIC3 FPGA
Eng Mgr:	
Engr:	
Doc Ctrl:	Size: B Document No: Rev 3.0
Assembly	
Date: 03/11/05	DRAWN BY: Sanmina-SCI Pg 3 of 10



LCD MODULE INTERFACE CIRCUIT

SCHEMATIC DIAGRAM NOTES

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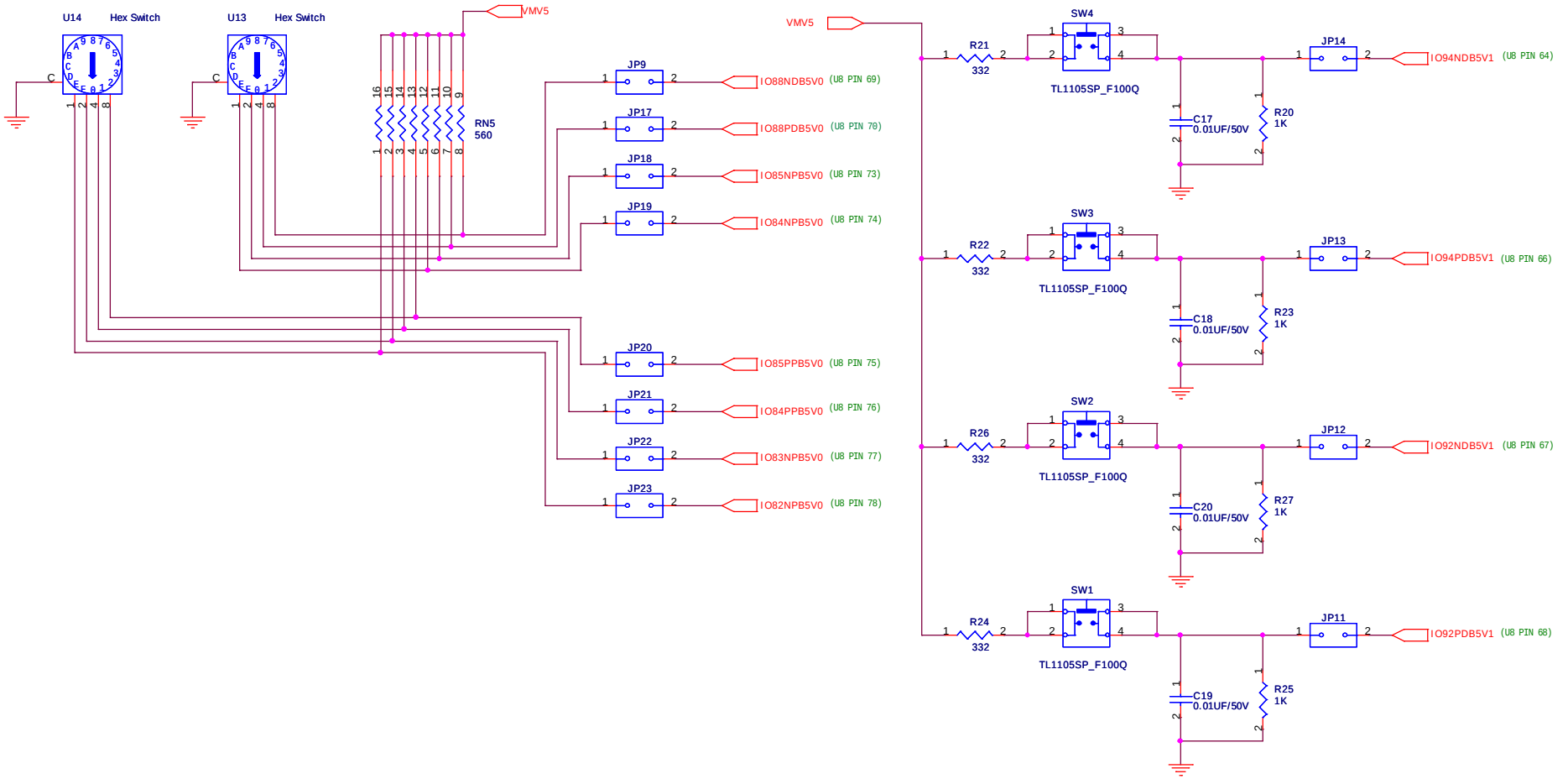
BOARD INFORMATION

PCB FAB:,REV.02 PCB ASSEMBLY:,REV.02

Actel Corp 2061 Stierlin Ct Mountain View, CA 94043	**ProASIC3/E STARTER KIT BOARD** **A3PE-EVAL-BRD600-SA**	
Approvals: Eng Mgr: Engr: Doc Cont: Assembly	Title: **LED & LCD Module Interface Circuit**	
	Size: B	Document No:
		Rev 3.0
Date: 03/11/05	DRAWN BY: Sanmina-SCI	Pg.4 of 10



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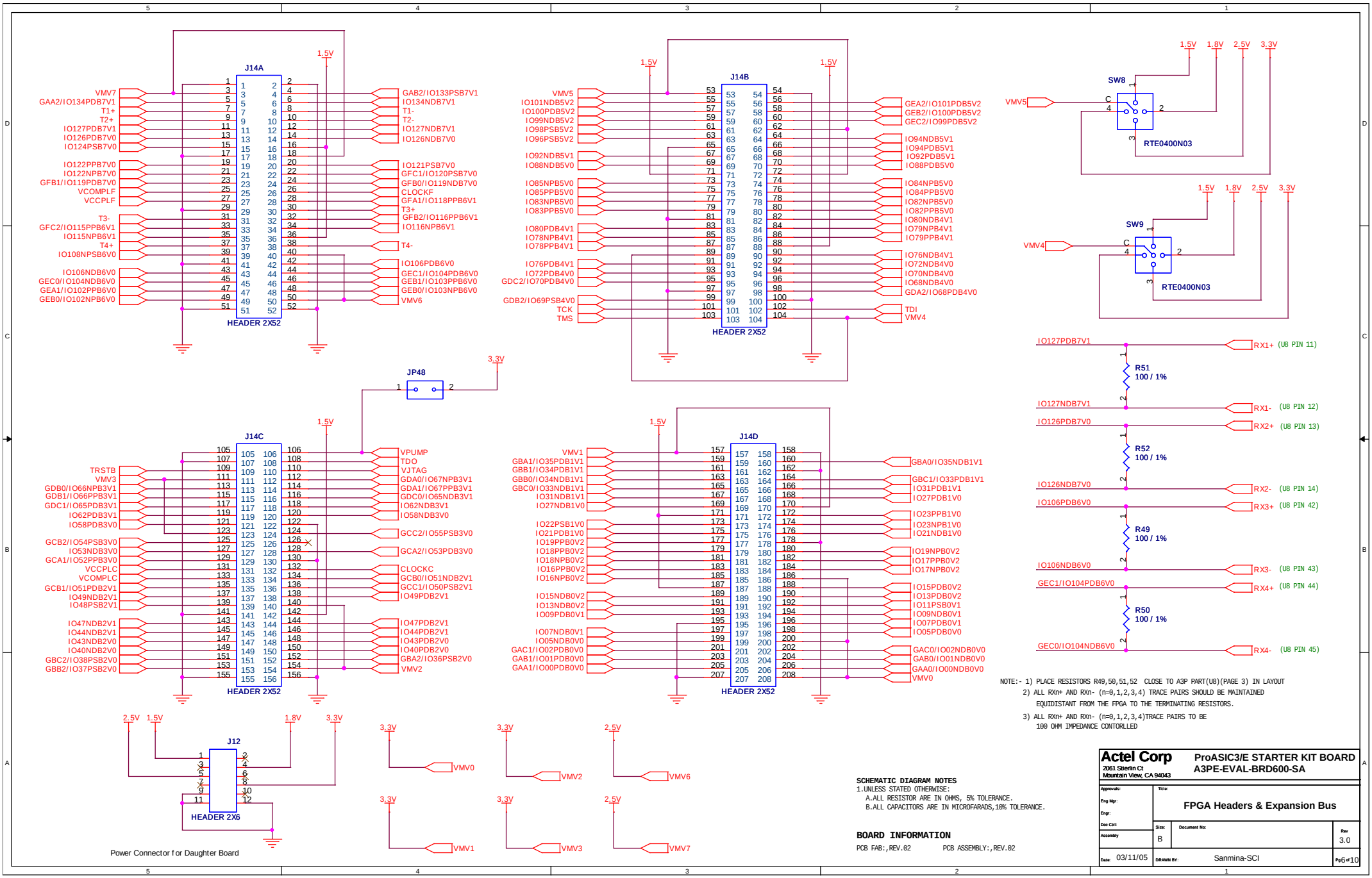
BOARD INFORMATION

PCB FAB:,REV.02 PCB ASSEMBLY:,REV.02

Actel Corp 2061 Stierlin Ct Mountain View, CA 94043	**ProASIC3/E STARTER KIT BOARD** **A3PE-EVAL-BRD600-SA**	
Approvals:	Title: **PushButton & HEX Switches**	
Eng Mgr:		
Engr:		
Doc Cont:	Size: B	Rev 3.0
Assembly	Document No:	
Date: 03/11/05	DRAWN BY: Sanmina-SCI	Pg 5 of 10



NOTE:- 1) PLACE RESISTORS R49,50,51,52 CLOSE TO A3P PART(U8)(PAGE 3) IN LAYOUT
2) ALL RXn+ AND RXn- (n=0,1,2,3,4) TRACE PAIRS SHOULD BE MAINTAINED EQUIDISTANT FROM THE FPGA TO THE TERMINATING RESISTORS.
3) ALL RXn+ AND RXn- (n=0,1,2,3,4)TRACE PAIRS TO BE 100 OHM IMPEDANCE CONTORLLED

SCHEMATIC DIAGRAM NOTES
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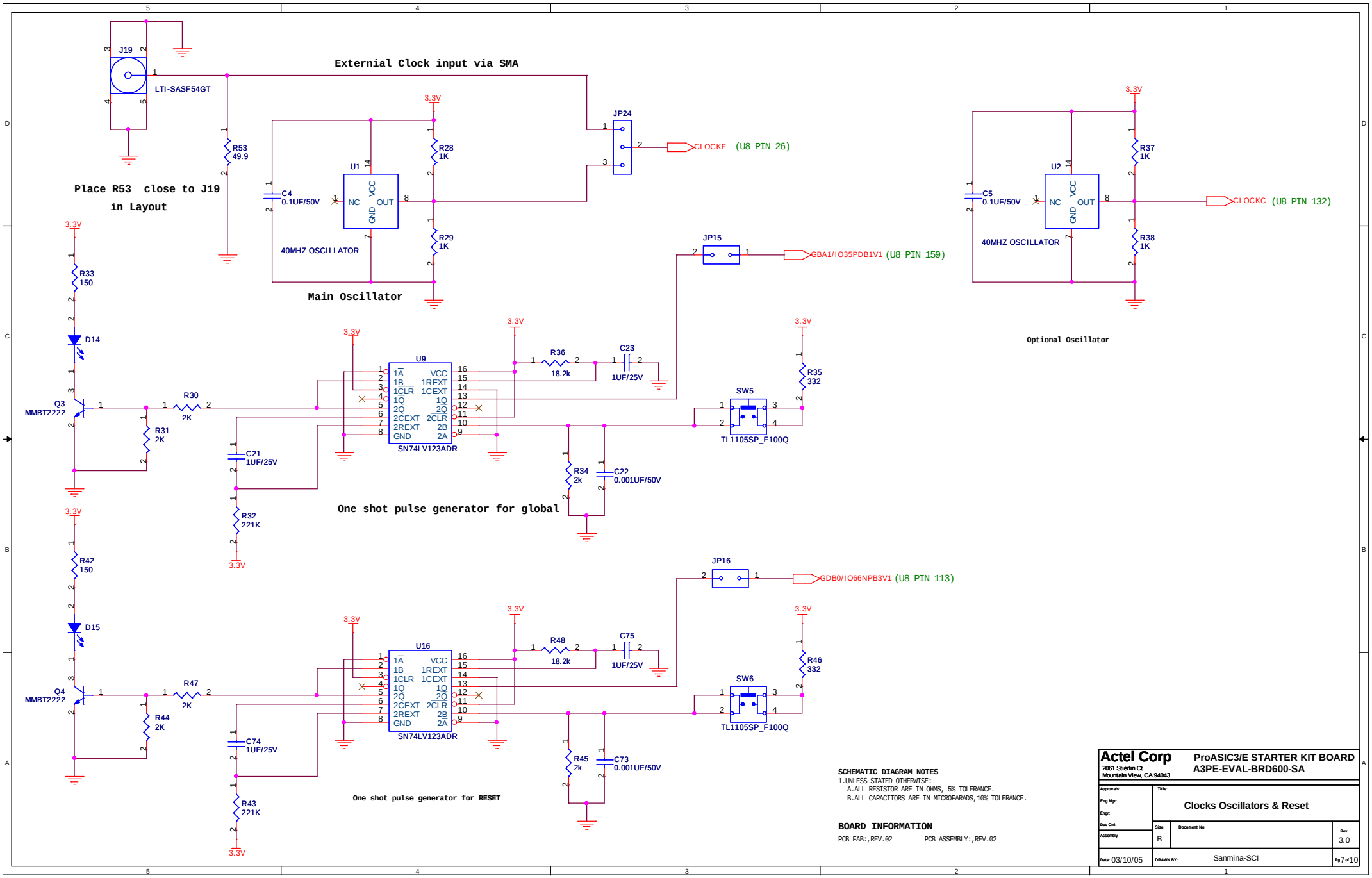
BOARD INFORMATION
PCB FAB:,REV.02 PCB ASSEMBLY:,REV.02

Actel Corp
2061 Stierlin Ct
Mountain View, CA 94043

ProASIC3/E STARTER KIT BOARD
A3PE-EVAL-BRD600-SA

Approvals:
Eng Mgr:
Engr:
Doc Cntl:
Assembly
Date: 03/11/05

Title: FPGA Headers & Expansion Bus
Size: B
Document No:
Rev 3.0
DRAWN BY: Sanmina-SCI
Pg 6 of 10



SCHEMATIC DIAGRAM NOTES

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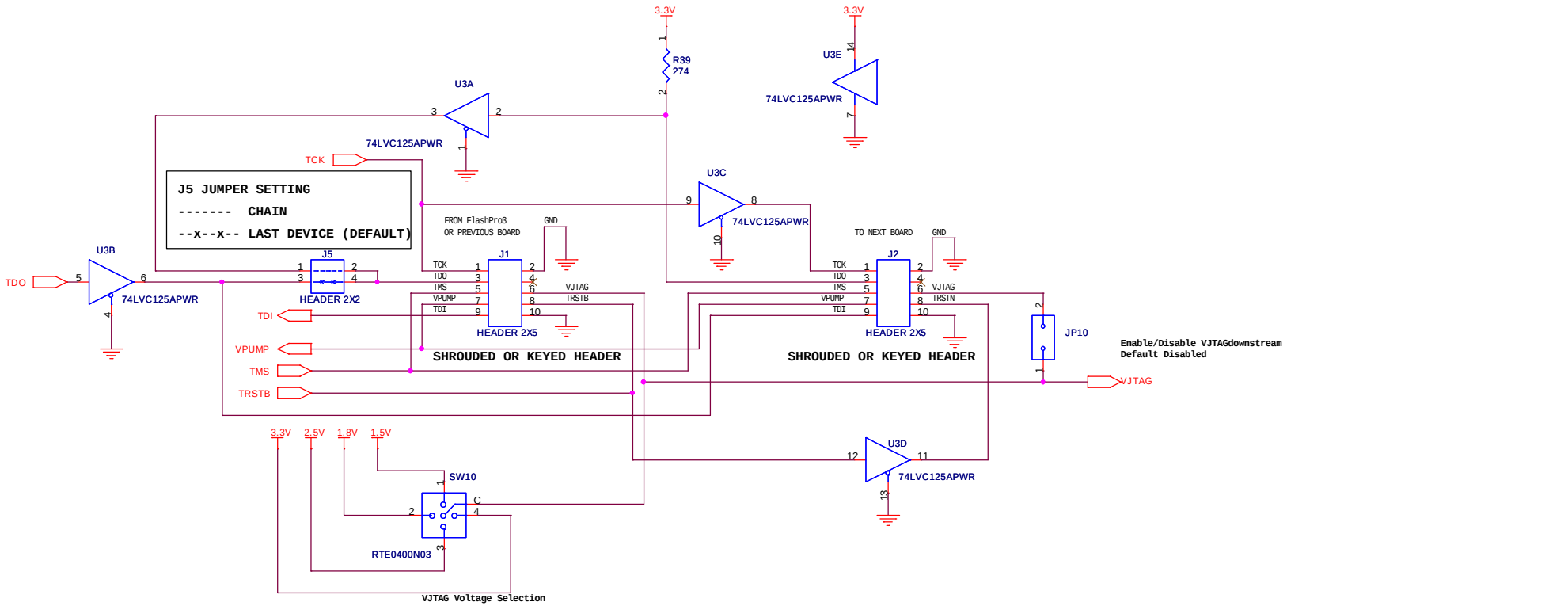
BOARD INFORMATION

PCB FAB:,REV.02 PCB ASSEMBLY:,REV.02

Actel Corp 2061 Stierlin Ct Mountain View, CA 94043	ProASIC3/E STARTER KIT BOARD A3PE-EVAL-BRD600-SA
Approvals:	Title: Clocks Oscillators & Reset
Eng Mgr:	
Engr:	
Doc Ctrl:	Size: B — Document No: — Rev 3.0
Assembly	
Date: 03/10/05	DRAWN BY: Sanmina-SCI — Pg 7 of 10



SCHEMATIC DIAGRAM NOTES

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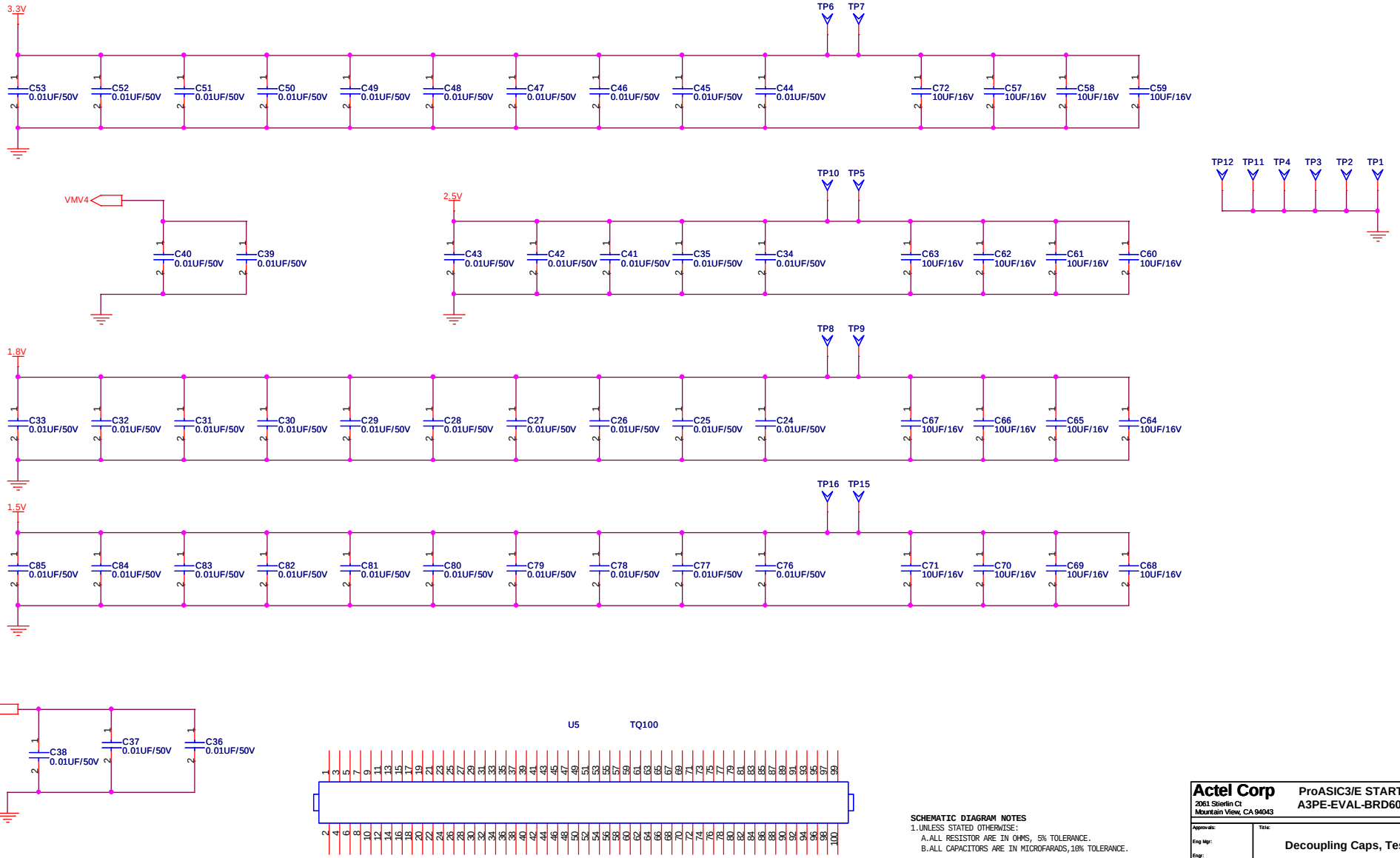
BOARD INFORMATION

PCB FAB:,REV.02 PCB ASSEMBLY:,REV.02

Actel Corp 2061 Stierlin Ct Mountain View, CA 94043	ProASIC3/E STARTER KIT BOARD A3PE-EVAL-BRD600-SA	
Approvals: Eng Mgr: Engr: Doc Cont: Assembly	Title: JTAG & JTAG DaisyChain Connector	
Date: 03/11/05	Size: B / Document No: / DRAWN BY: Sanmina-SCI	Rev 3.0
		Pg 8 of 10



SCHEMATIC DIAGRAM NOTES

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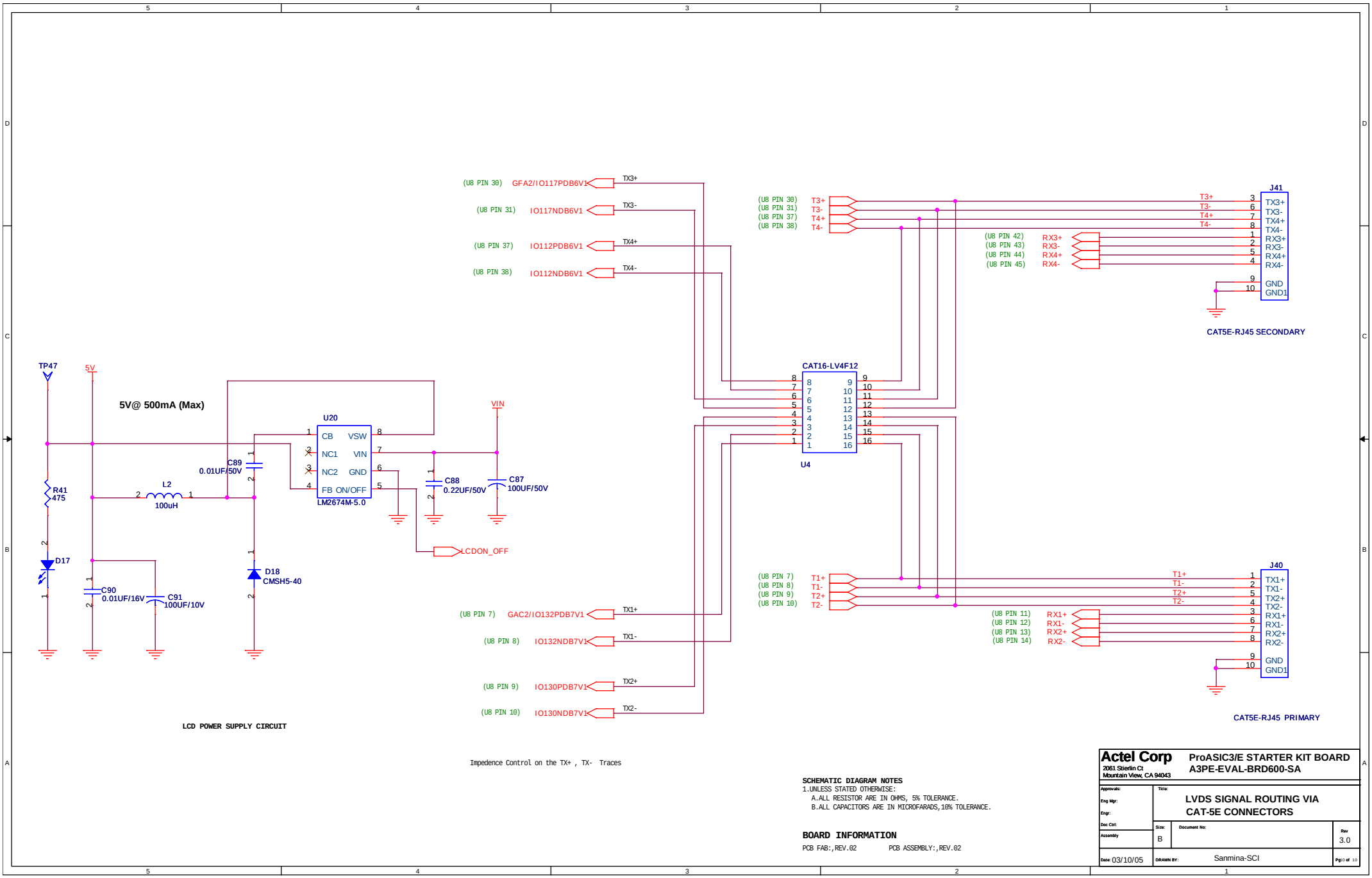
BOARD INFORMATION

PCB FAB:,REV.02 PCB ASSEMBLY:,REV.02

Actel Corp 2061 Stierlin Ct Mountain View, CA 94043	**ProASIC3/E STARTER KIT BOARD** **A3PE-EVAL-BRD600-SA**	
Approvals: Eng Mgr: Engr: Doc Ctrl: Assembly	Title: **Decoupling Caps, Test Points**	
	Size: B	Document No:
		Rev 3.0
Date: 03/11/05	DRAWN BY: Sanmina-SCI	Pg 9 of 10



Impedence Control on the TX+ , TX- Traces

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BOARD INFORMATION

PCB FAB:,REV.02 PCB ASSEMBLY:,REV.02

Actel Corp
2061 Stierlin Ct
Mountain View, CA 94043

ProASIC3/E STARTER KIT BOARD
A3PE-EVAL-BRD600-SA

Approvals:
Eng Mgr:
Engr:
Doc Ctrl:
Assembly

Title: **LVDS SIGNAL ROUTING VIA CAT-5E CONNECTORS**

Size: B
Document No:
Rev 3.0

Date: 03/10/05
DRAWN BY: Sanmina-SCI
Pg 10 of 10