ACTgen User's Guide

v6.1

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Trademarks

Table of Contents

What's new in ACTgen?

The ACTgen software generates a large variety of commonly used functions. You can generate structural netlists in EDIF, VHDL, and Verilog. Furthermore, you can generate VHDL and Verilog behavioral models for most parameterized functions (the behavioral models may be used in a simulation environment). ACTgen includes workspace and core management features.

This help provides descriptions of cores that you can generate using the ACTgen software. For more information about instantiating specific cores refer to the *Actel HDL Coding Style Guide*.

Previous users of ACTgen may notice substantial changes in the software. You no longer operate directly on a genfile; rather, you create a workspace, and then import existing cores and create new ones.

ACTgen includes several new features.

Actel's ACTgen workspace

You must open a workspace in ACTgen before you can create or modify a core. Workspaces enable you to create, modify, and import existing ACTgen cores. The workspace is a logical grouping for your cores; each workspace contains cores for a specific product family.

Cores

When you generate an ACTgen core, ACTgen creates a core file that includes a structural netlist, an optional VHDL or Verilog behavioral netlist, a log file that summarizes your core parameters, and a GEN file that includes all the parameters you selected when you generated the core. Do not manually edit any of the core files. Use ACTgen to edit your cores.

Varieties

Varieties list different implementations of similar functions. For example, when you click Arithmetic in the Category tab, ACTgen displays the complete list of varieties available for Arithmetic. Click a column header to sort the list of varieties. Click the Adder function to display the list of core varieties for Adder.

Core Catalog

The Categories tab in the Core Catalog window displays the device family for your workspace at the top. Available categories are listed below. Categories may vary according to device family; select the latest families to see and test the newest cores available. Click a core category to expand the list and display the functions.

The Alphabetic tab displays an alphabetical list of all the functions available for your device family. Click a function to display a list of varieties. Click the column headers to sort your core varieties.

Core Variety View

The Core Variety View window displays the list of cores available for your device family. Click core categories and functions to narrow your list of core varieties. For example, click your device family for a complete list of all the core varieties for your family. Click the Arithmetic category to view a list of only Arithmetic core varieties, and click a specific function to narrow your list even further and view core varieties for the function.

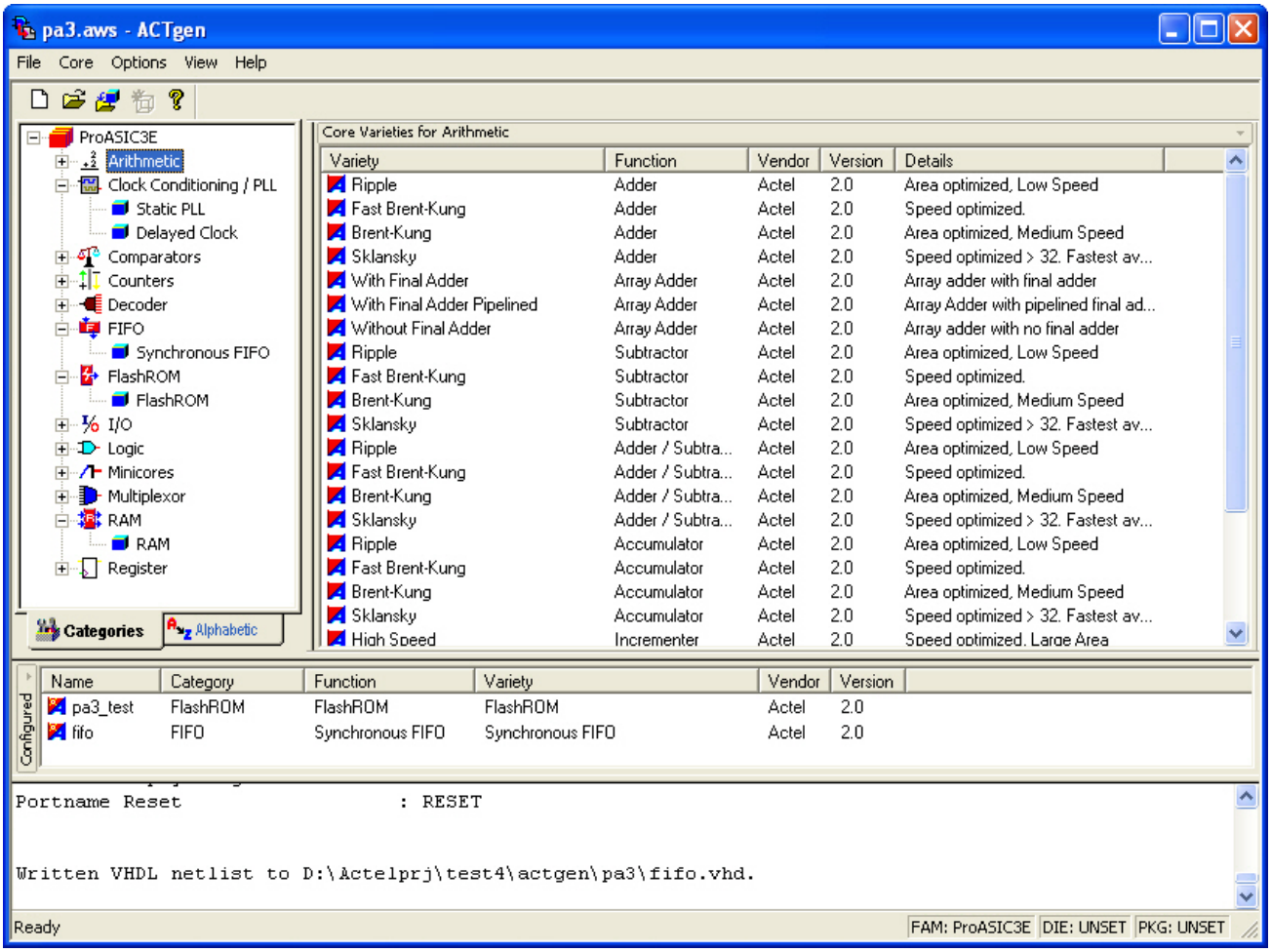
Log Window

The log window displays tips and instructions on the ACTgen flow. It may list errors and warnings that occur during core generation, as well as core parameters after you generate a core.

ACTgen user interface

The ACTgen software generates a large variety of commonly used functions. You can generate structural netlists in EDIF, VHDL, and Verilog. Furthermore, you can generate VHDL and Verilog behavioral models for most parameterized functions (the behavioral models may be used in a simulation environment). ACTgen includes workspace and core-management features.

The ACTgen is divided into four sections: the Core Catalog, the Variety View window, the Configured Core View window, and the Log Window (as shown in the figure below).



Use this interface to browse your cores, review your configured cores, and select cores to create or modify.

The **Variety View** window displays a list of core varieties available for the core you have selected. For example, if you select the Arithmetic core type, and then select the Adder core, the Variety View window displays a list that includes Sklansky, Fast Brent-Kung, Ripple, etc.

The **Configured Core View** window displays a list of configured cores in your workspace. The configured cores appear each time you re-open your workspace. You can delete cores from your Configured Core View (and leave them on the disk), or you may delete them from your disk entirely.

The **Log Window** displays information as you configure your cores in your workspace.

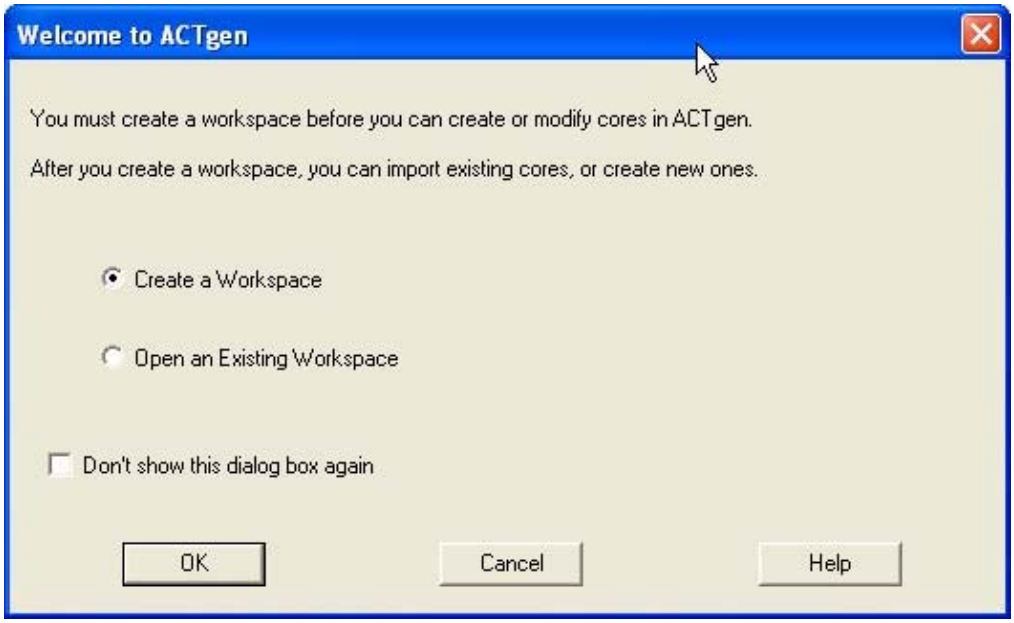
Create a workspace

You must create a workspace to generate a core in ACTgen.

A workspace defines your family and the default directory in which you save your configured cores. If you wish, you may save your workspace in a different directory. The workspace is a logical grouping for your cores; each workspace contains cores for a specific product family.

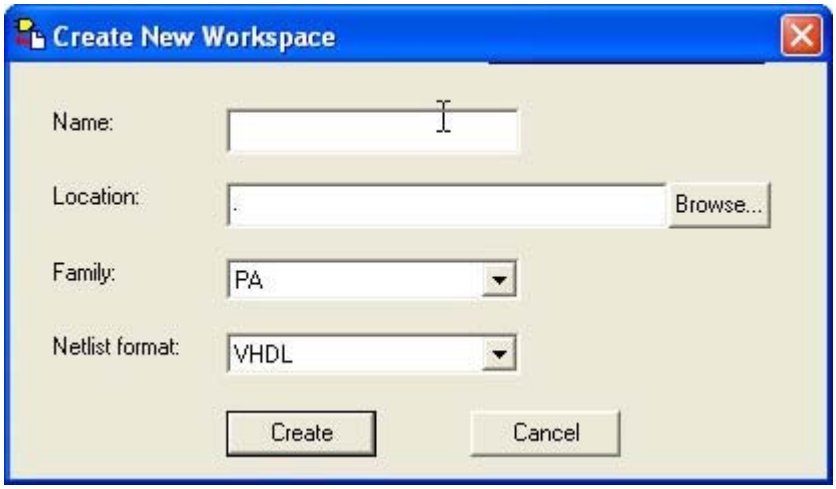
To create a workspace:

1. Start ACTgen. When you open ACTgen it asks if you wish to create a workspace or open an existing workspace (as shown in the figure below).



You may choose to create a workspace or open an existing workspace. Select the check box to hide this dialog the next time you open ACTgen.

2. From the **File** menu, select **New Workspace**, or click CTRL + N.
3. Specify the **Workspace name**, **Workspace location** (click the **Browse** button to navigate to or create a directory), **Family**, and **Netlist format.**



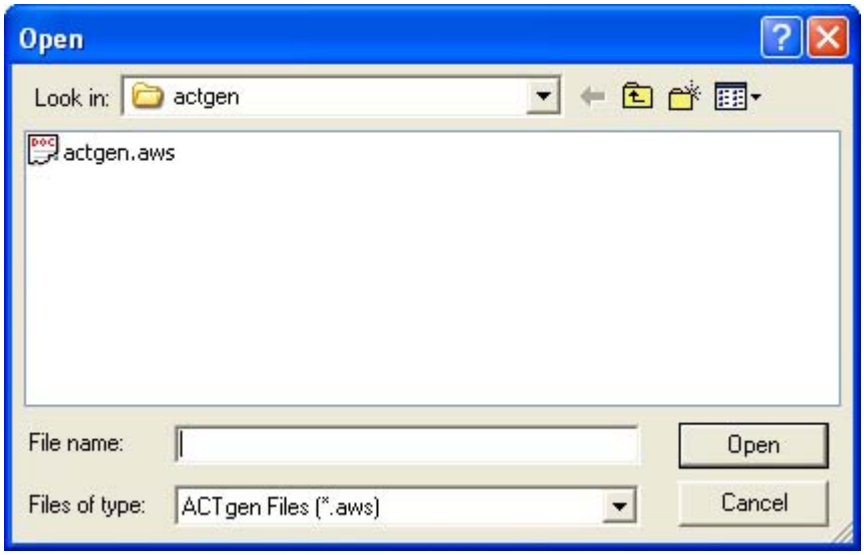
Create New Workspace Dialog Box

4. Click Create to create the new workspace. The new workspace appears in the ACTgen window. By default, the list of cores available in a new workspace is sorted by **Categories**. Click the **Alphabetic** tab to display the complete list of ACTgen cores.

Open a workspace

You must open a workspace in ACTgen to generate cores. If you have never opened a workspace, you can create one. To open an existing workspace:

1. Start ACTgen.
2. From the **File** menu, select **Open Workspace**, or click the Open Workspace button in the ACTgen toolbar. This opens the Open Workspace dialog box (as shown in the figure below).



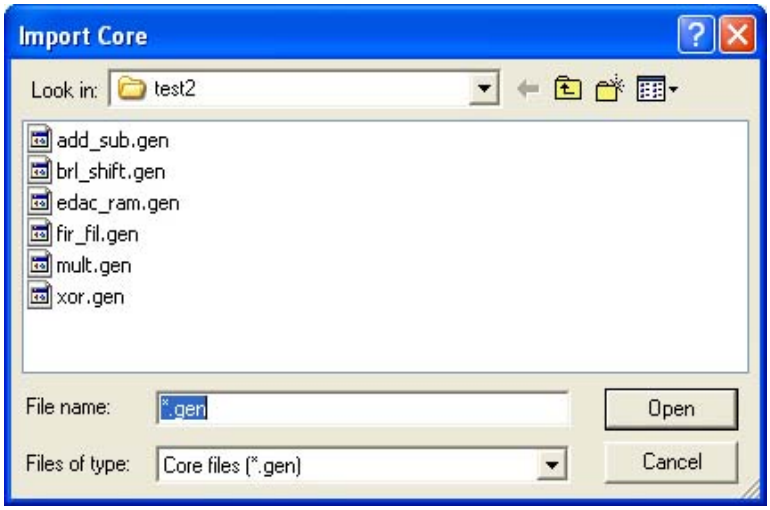
3. Navigate to the workspace you wish to open and click **Open.**

Import a legacy core

You can import ACTgen legacy cores into your current workspace. When you import a legacy core the import copies only the genfile into your workspace. You MUST regenerate the core to get a new netlist in ACTgen.

To import a legacy core:

1. From the **File** menu, select **Import Core**. This displays the Import Core dialog box (as shown in the figure below).



Import Core Dialog Box

2. Navigate to your core you wish to import and click **Open**. The core is added to your current workspace and remains in your workspace until you **Remove** it.

You can only import legacy cores that were generated for the family on which the workspace operates. If you import cores from other families, you get an error message, as shown in the figure below.

Import Core Error Message

Remove or Delete a core

To remove a core from your workspace, select the core in the **Core View** window and from the **Core** menu select **Remove**. You do not need to save your workspace.

Note: removing a core from your workspace does not delete the core from your directory. You can import the core later if you wish.

You may also choose to **Remove from Disk and Workspace**; you cannot re-import the core if you remove it from your disk and workspace. All files associated with the core are deleted along with the core itself.

Save the workspace

All changes to the workspace are saved automatically. You can save the workspace with a different name (useful if you want to create a copy of your workspace in a different directory).

To save your workspace, from the **File** menu, select **Save Workspace As** and specify the **Name** and **Location**.

ACTgen Preferences

Use the Preferences dialog box to set the default directory for new workspaces. Whenever you try to Open a GEN file or generate a netlist, ACTgen uses the preferences you set here to generate your file.

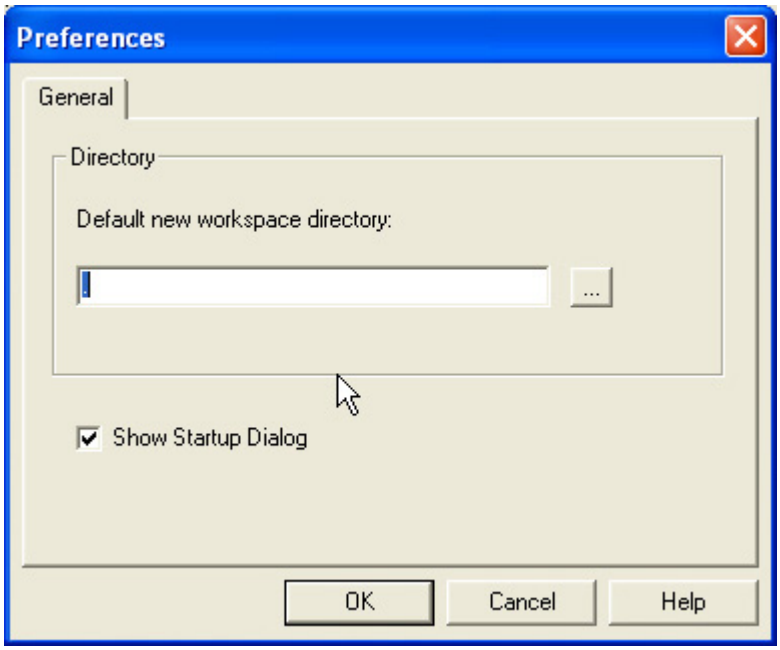
Your default netlist output and family type are workspace settings.

To set or modify your preferences:

From the **File** menu, select **Preferences**. The Preferences dialog box (**General** tab) appears. Type the pathname, or click the browse button and navigate to your new default directory for your new workspaces.

UNIX Only: Specify the location of your PDF reader and web browser.

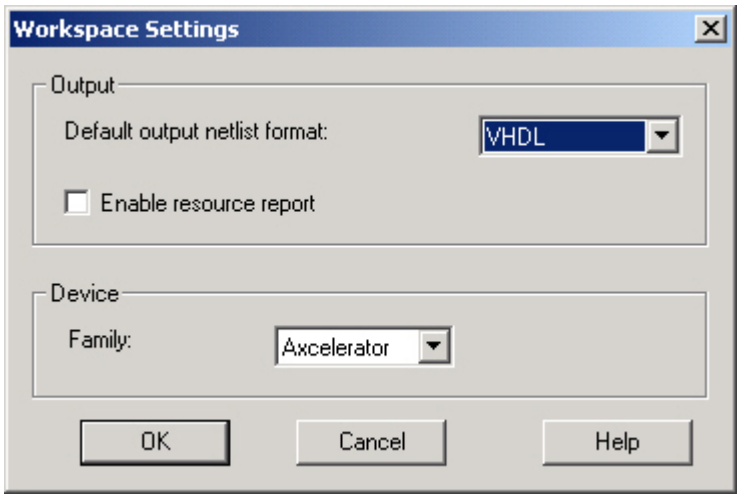
Select the **Show Startup Dialog checkbox** to display the startup dialog (as shown in the figure below).



ACTgen Preferences Dialog Box

Workspace settings

To change your workspace settings, from the **Options** menu, select **Workspace settings**. If you wish to change your preferences, you can modify them in the File menu.



Workspace Settings Dialog Box

The Workspace Settings dialog box (above) specifies your Default output netlist format, enables or disables the Resource report (antifuse families only), and lists the device family you have selected for your workspace.

Antifuse families only: The Resource report calculates and displays the sequential, combinatorial, I/O, memory, and PLL resources used in the generated core as a percentage of the largest device in the family.

Select the check box to enable the Resource report.

Generating reports in ACTgen

As ACTgen generates a core it writes information to the Log window. The report contains information defining the core, and is divided into the following sections:

Core Parameters - This section lists the options selected to build the core

Fan-in Control information - This section defines the type of buffering for each control signal and the values used to distribute the total load

(Optional) **Compile report -** Lists compile information related to the core

Create Cores

Create a new core in ACTgen

You can create a new core in ACTgen only after you have created a workspace.

To create a new core in ACTgen:

1. Select a core type in the **Categories** tab (Arithmetic, Comparator, Converters, etc.). The **Variety View** window displays the list of configurable cores.

2. Double-click the core variety you wish to generate, or right-click and select **Create Core**. The core configuration dialog box appears. The configuration dialog box varies depending on which core you select.
3. Set the parameters for your core and click **Generate**. The **Save As** dialog box appears.
4. Specify the name of your new core and click **Save** to continue. ACTgen saves your core to the specified directory and adds your core to your workspace (in the Configured Core View Window). If you deliberately save the core in a different directory than the workspace, the core will be saved, but will not be added to the workspace.
   Your core remains in the workspace until you choose to **Remove** it.

Note: You cannot create two cores with the same name. ACTgen is case-insensitive; "core_A" is equivalent to "core_a".

Reconfigure a previously generated core in ACTgen

You can reconfigure your cores in ACTgen. To do so, you must first have added a core to your workspace.

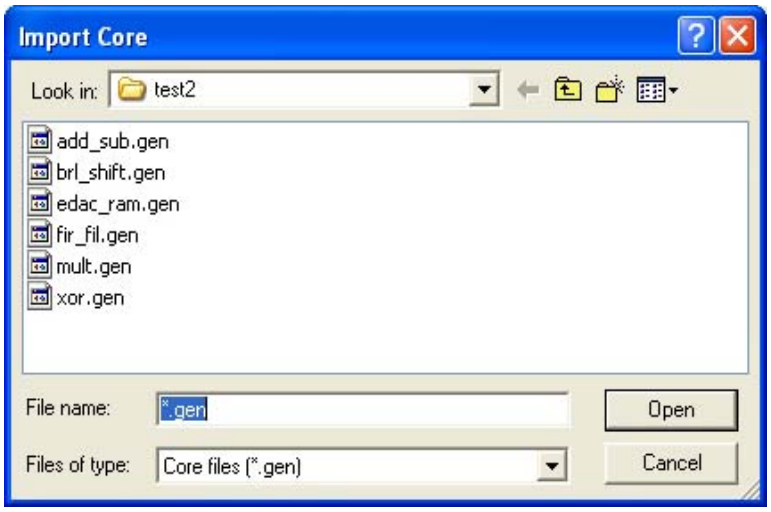
To reconfigure a core in ACTgen:

1. Select the core in the Configured Core View window.
2. From the **Core** menu, select **Modify Core,** or right-click the core and select **Modify Core** from the shortcut menu. The configuration dialog box opens to display the configuration options specified in the core. Your core configuration options vary depending on the device family you selected when you created your workspace.

Import an ACTgen core

You can import ACTgen cores into your current workspace. To do so:

1. From the **File** menu, select **Import Core**. This displays the Import Core dialog box (as shown in the figure below).



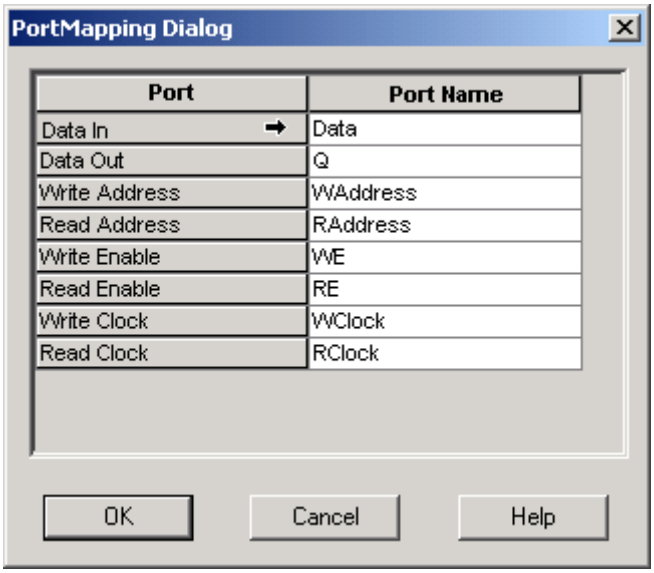
Import Core Dialog Box

2. Navigate to the core you wish to import and click **Open**. The core is added to your current workspace and remains in your workspace until you **Remove** it.

Note: You cannot import two cores with the same name. ACTgen is case-insensitive; "core_A" is equivalent to "core_a".

Port Mapping dialog box

Some cores have a high number of input and output signals. You can use the Port Mapping function to specify the port naming for cores with a high number of input and output signals. Click the Port Mapping button to open the Port Mapping dialog box.

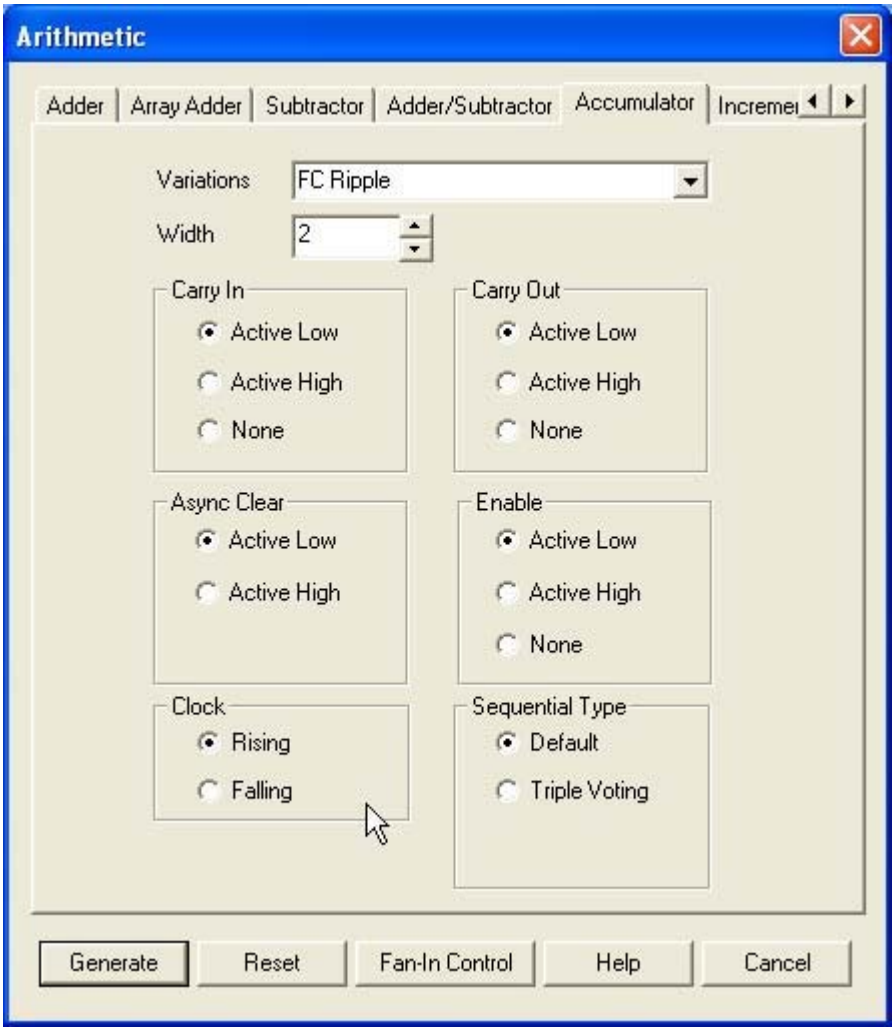


Port Mapping Dialog Box

The Port Mapping dialog box appears and displays the default port name values. Enter changes and click OK to submit, or click Cancel to return to the default values.

Fast carry chains (Axcelerator only)

The Axcelerator Family offers fast carry-chain cores for a compact design of Arithmetic Macros and Counters. Fast Carry cores for Axcelerator are available in the Variations drop-down menu.



Fast Carry Chain Macros in Variations Drop-Down Menu

You can generate FC cores via the ACTgen module generator or infer them via Actel's Synopsys Designware (DWACT). FC cores are always the most area-efficient way to implement these modules. They are superior in performance for up to 32-bit designs, although some modules may be inferior beyond 32-bit (incrementors, for example). Though ACTgen offers both architecture types (FC cores and non-FC cores), Actel recommends you use FC cores to guarantee area efficiency.

In the ACTgen GUI, you can distinguish the FC cores from non-FC cores by the prefix “FC” or "Fast Carry" (e.g. “FC High Speed” versus “High Speed”). The GUI also lists a description of the macro in the Details column in the Variety View.

The core parameters used in the GEN file also use “FC” for distinction. For example the “High Speed” Adder using fast carry chains is specified by:

LPMTYPE:LPM_FC_ADD_SUB

LPM_HINT:FC_FADD

whereas the corresponding non-FC version is specified by:

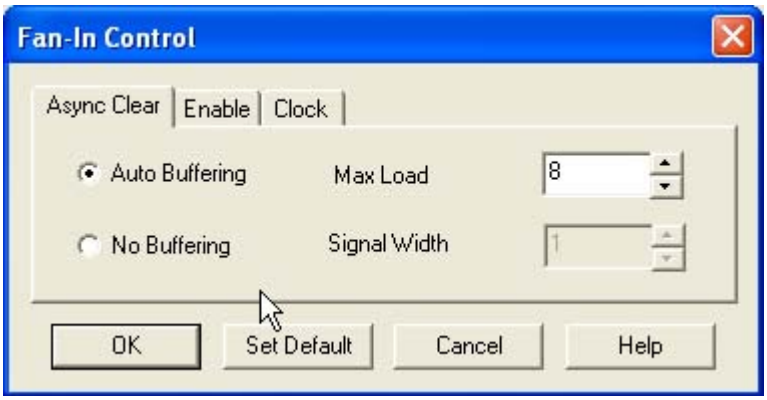
LPMTYPE:LPM_ADD_SUB

LPM_HINT:FADD

Fan-in control tool

Fan-In Control

The Fan-In Control tool gives advanced users the ability to control the buffering of clocks, asynchronous presets and clears, and other control signals. This tool is optional because default buffering values are provided for all signals. The tool supports two types of buffering control, automatic and no buffering, which provide maximum buffering flexibility.



Fan-In Control Dialog Box

Using Fan-In Control

1. Set your core options.
2. Open the Fan-In Control dialog box and input your values. If you modify your core options after you set your fan-in values, you must check them to ensure that they are unaffected.

Auto Buffering

Automatic buffering automatically inserts buffers as required, and provides ease of use for fanning out heavily loaded signals. Automatic buffering is the default buffering type for most signals. ACTgen automatically inserts buffers/inverters for this option and provides a single input for the signal. The value defined for automatic buffering indicates the maximum loading on the network for the given control signal. ACTgen also balances the loading as required. Automatic buffering can indirectly define input loading to a core.

No Buffering

No buffering restricts ACTgen from inserting buffers. This allows designers to manually use global clock resources for control signals. This also provides the ability to enhance performance of control signals by performing a logic function and correcting for fan-in by duplicating logic external to the core. If the signal is to be driven by a clock resource, you must set the signal width on the clock to 1; a signal width value of one (1) causes all loads to be driven by a single input.

Fan-In Control Limitations

The Fan-In Control tool has the following limitations:

The Fan-In Control tool has been designed to be a slave to the primary core definition screen. Therefore, you should define exceptions to default values only after you have made all primary screen selections. Changing the main screen may affect the defined fan-in values. Information on modified fan-in will be provided in the Report window and should always be verified for correctness.

The ability to perform no buffering on some control signals is limited to a single polarity because of hardware limitations. For example, ACT 2, 1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, and eX limit asynchronous clears to Active Low only. Choosing Active High for this signal causes the No Buffering option to be unavailable. When this situation occurs, go back to the primary screen and change the active level for the given signal if no buffering is a must.

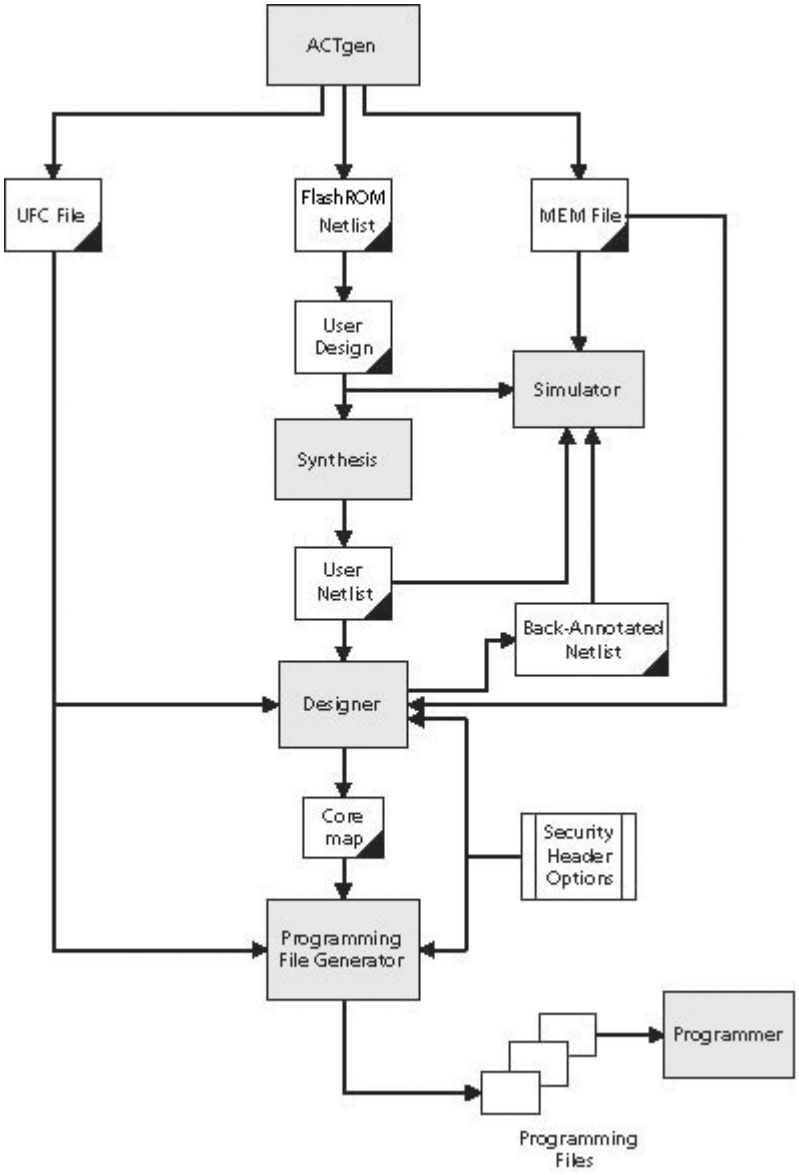
Some control signals, such as the Count Enable signal are not included in the Fan-In Control tool because fan-out is corrected internally using AND and OR logic functions.

Use the Fan-In Control dialog box to specify Auto Buffering or No Buffering, Max Load, and Signal Width.

FlashROM

Welcome to FlashROM

FlashROM memory provides the security of stored data in addition to a 128-bit AES decryption core. You can read, modify and write to the FlashROM using the JTAG interface; however, you can only read it from the FPGA core.



FlashROM Flow

Access FlashROM from the ACTgen tool. It opens a special FlashROM core generator that enables you to configure the FlashROM functionality.

Note: The FlashROM functionality is available only for ProASIC3/E devices.

ProASIC3/E devices have a flexible programming option. The FlashROM and the FPGA core fabric can be programmed independently of each other, allowing the FlashROM to be updated without changing the FPGA core fabric. The following are just a few examples of possible applications for the FlashROM feature:

Internet protocol (IP) addressing (wireless or fixed)

System-calibration settings

Device serialization and/or inventory control

Subscription-based business models (e.g. set-top boxes)

Secure key storage

Asset management tracking

Date stamping

Version management

The FlashROM is programmed using the standard IEEE1532 JTAG programming interface. Pages can be individually programmed (erased and written) and on-chip AES decryption can be used selectively to load data securely into the FlashROM (such as application based security keys stored in the FlashROM for a design).

The FlashROM can selectively be read back both through the JTAG programming interface or via direct FPGA core addressing. Its contents can only be updated via the JTAG interface. A seven-bit address from FPGA core defines which of the eight pages (3 MSBs) is being read and which of the 16 bytes in the page (4 LSBs) are being read.

The FlashROM is physically organized as 8x128 bit blocks and logically organized as eight pages by 16 bytes. Only Flash FPGAs contain on-chip nonvolatile memory (NVM) and Actel's ProASIC3/E is the only FPGA to support this feature.

You can assign specific regions of the FlashROM for specific purposes by floorplanning the FlashROM and assigning properties. The content of these regions can be modified during programming time if you assign a modifiable content property to a given region. If you do not want the FlashROM content to be modified, you can fix the content in ACTgen.

When you generate a new FlashROM file the generator saves the following files for you to use throughout the design cycle:

ACTgen GEN file

Netlist file - use this file to instantiate your core, just as you would instantiate any other core in your design.

UFC file - User Flash configuration file, it contains all the configuration information regarding the FlashROM data content and is used for programming. You can export a core map file that contains the core programming information use it along with the UFC file to generate programming files. Designer software supports importing the UFC file and launching the programming file generator to merge the FPGA core map file and the FlashROM programming file.

MEM file - FlashROM specific memory initialization file. The MEM file has 128 rows of eight bits, representing the contents of the FlashROM. ACTgen will default to 0s for any unspecified locations of the FlashROM memory. This file is used exclusively for simulation.

Use the FlashROM help to:

1. Configure FlashROM in ACTgen
2. Simulate Pre/Post Synthesis
3. Synthesize
4. Place-and-Route
5. Run Back-Annotation and Timing Simulation
6. Specify security settings
7. Specify FlashROM content
8. Generate a programming file

Create / Configure FlashROM in ACTgen

The FlashROM can be partitioned into regions and each region can be used for a specific purpose, like serial number storage, version number saving, etc.

Use the FlashROM core generator (in ACTgen) to create a region within a page, modify the region, and assign properties to that region.

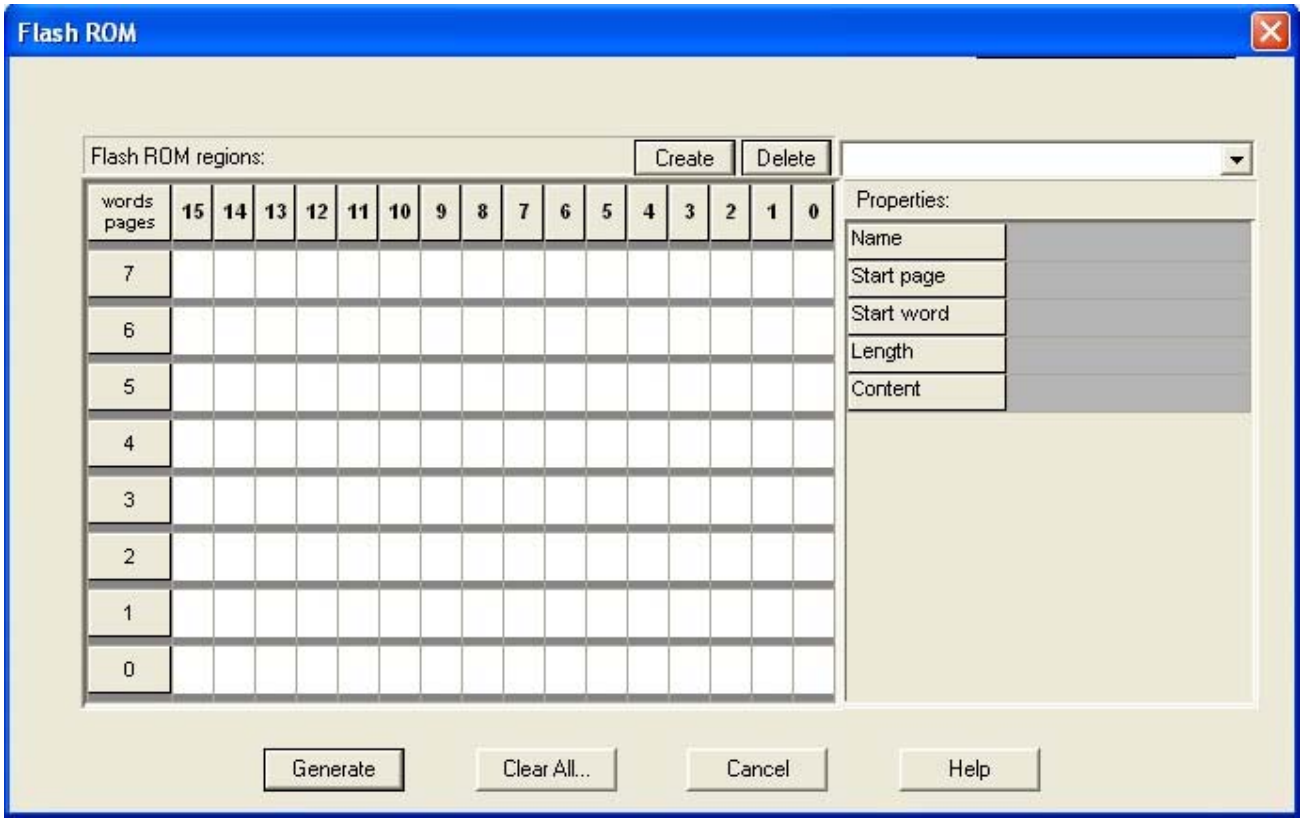
The FlashROM user interface includes the Configuration Grid, list of existing regions, and the Properties field. The Properties field includes region-specific information. You can assign values to the following properties:

Static Fixed Data - Enables you to fix the data so that it cannot be changed during programming time. This option is useful when the you have fixed data stored in this region that is required for the operation of the design in the FPGA. Key storage is one example.

Modifiable Fixed Data - Select this option when the data in a particular region is expected to be static data (such as a version number, which remains the same for a long duration, but could conceivably change in future). This option enables you to specify this region for this special purpose so that you need not come back and change the value every time you need to enter new data. The FlashROM configuration file can be handed off to the operations group at this point.

Read from File - This provides the full flexibility of FlashROM usage to the customer. If you have a customized algorithm for generating the FlashROM data, you can specify this setting. You can then generate a file with data for as many devices you wish to program and load that into FlashPoint programming file generation software to get programming files that include all the data. ACTgen will optionally pass the location of the file where the data is stored, if the file is specified in ACTgen.

Auto Increment/Decrement - This scenario is useful when you specify the contents of FlashROM for a large number of devices in a serial manner. You can specify the step value for the serial number and a maximum value for inventory control. During programming file generation, the actual number of devices to be programmed is specified and a start value is input to the software. Software generates the files to complete serial programming of the FlashROM.



FlashROM Core Generator

To create a new FlashROM in ACTgen:

1. In ACTgen, select the **Flash ROM** in the **Function** tab. Double-click the **FlashROM** core in the **Variety View** window to start the core generator.
2. Click and drag the mouse to select words, then click the **Create** button. The core generator displays the new region properties in the **Properties** grid.

   You may also right-click a word and select **Create** from the shortcut menu, or select a word and press the **Insert** key on your keyboard. You can copy and paste regions in FlashROM; to do so, right-click a word and select **Copy**, then click an empty word, right-click, and choose **Paste**. If the region does not copy, the page does not have enough room. Try another page with more room.

3. Click in the **Properties** grid to modify a regions properties. **Start page**, **Start word**, and **Length** are read-only. The data you enter is verified and stored in the FlashROM as soon as you leave the Properties grid and select another FlashROM region.
4. Click **Generate** to generate a Netlist (you must specify EDIF, VHDL, or Verilog), ACTgen GEN file, UFC, and MEM file. The **Generate** button opens the **Save As** dialog. Specify a name, location, and file type, and click **Save**.

   After you generate the FlashROM netlist, you can instantiate the core similar to other ACTgen cores in your design..

To delete a FlashROM Region:

1. Click to select a region in the **Regions** window.

2. Click the **Delete** button in the core generator, press the **Delete** key on the keyboard, or right-click and select **Delete** from the shortcut menu.

3. Click **OK**.

Modify existing FlashROM configuration

You can modify your existing FlashROM configuration the same way that you modify any configured core in ACTgen. To do so:

1. Open your ACTgen workspace that contains the configured FlashROM core.
2. Double-click the configured core (in the Configured Core View) to open the FlashROM configuration. The FlashROM core opens with all the settings you saved.
3. Modify the values you wish to change and select **Generate** to save your changes. Generate opens the Save As dialog. Save your new file with the same name if you wish to overwrite the old file.

You cannot edit the configuration of an existing FlashROM GEN file, only change the data. If you wish to change the configuration you must generate a new core.

Simulate Pre/Post Synthesis

FlashROM uses the MEM file for simulation.

The MEM file has 128 rows of eight bits, representing the contents of the FlashROM. ACTgen defaults to 0s for any unspecified locations of the FlashROM memory.

During simulation, employ the MEM file, which contains the memory content, along with the design netlist and testbench. The VITAL and Verilog simulation models accept the generics passed by the netlist, read the MEM file, and perform simulation with the data in the file.

In addition to using the MEM file from ACTgen, you may create a binary file with 128 rows of eight bits and save the file as a MEM file. Actel recommends using different names if you plan to generate multiple MEM files. During place-and-route in Designer, the software recognizes the generic property in the netlist and pass the MEM file links through to the output netlist.

Place-and-Route and FlashROM

There are no special instructions for place-and-route for FlashROM. Run Layout in Designer to place-and-route your design.

Index

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