

ALTERA®



SOPC
WORLD
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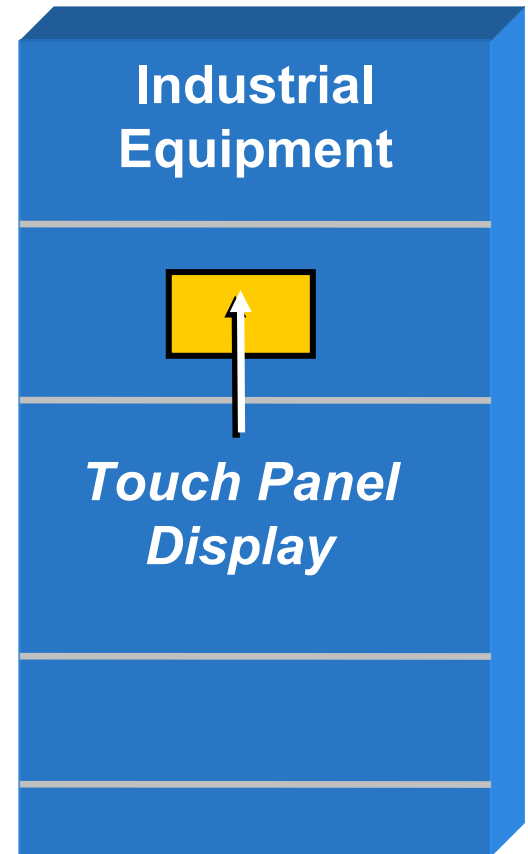
Designing Embedded Processors in FPGAs

Agenda

- Industrial Control Systems
- Concept
- Implementation
- Summary & Conclusions

Industrial Control Systems

- Typically Low Volume
 - Many Variations Required
- High Customization
 - Number of Attached Sensors
 - Types of Attached Sensors
 - Required User Interface Needs
 - Storage & Recording Needs
- Touch Panel Displays
 - Increasing Use to Reduce Cost



Concept

Flexibility

Need to Easily Modify Design
Allowing for Customization
or Feature Enhancements

**Reaction to Customer
Needs**

**Changing Solution Needs:
New Sensors/ New Control**

Time to Market

Capability to Complete
Development Work for
Solution in Time to
Meet Specific Market
Window



Reusability

Ability to Reuse Much of
Existing Design As Starting
Point for New Solution

**Rapid Design of New
Control Solutions**

Concept

■ Solution Requirements

– Minimal Cost

- Overall Solution Measured Not Only By Cost of Components, But Cost of Board
- The Lower the Solution Cost, The Easier It becomes to Win Business & Sustain Margins

– Manufacturability

- Can Existing Implementation Be Maintained If Devices Fail – i.e., Is Supply Guaranteed?

– Device Qualification

- If Company Has Stringent Device Qualification Needs, Advantages of Utilizing Single Device for Many Applications Becomes Apparent

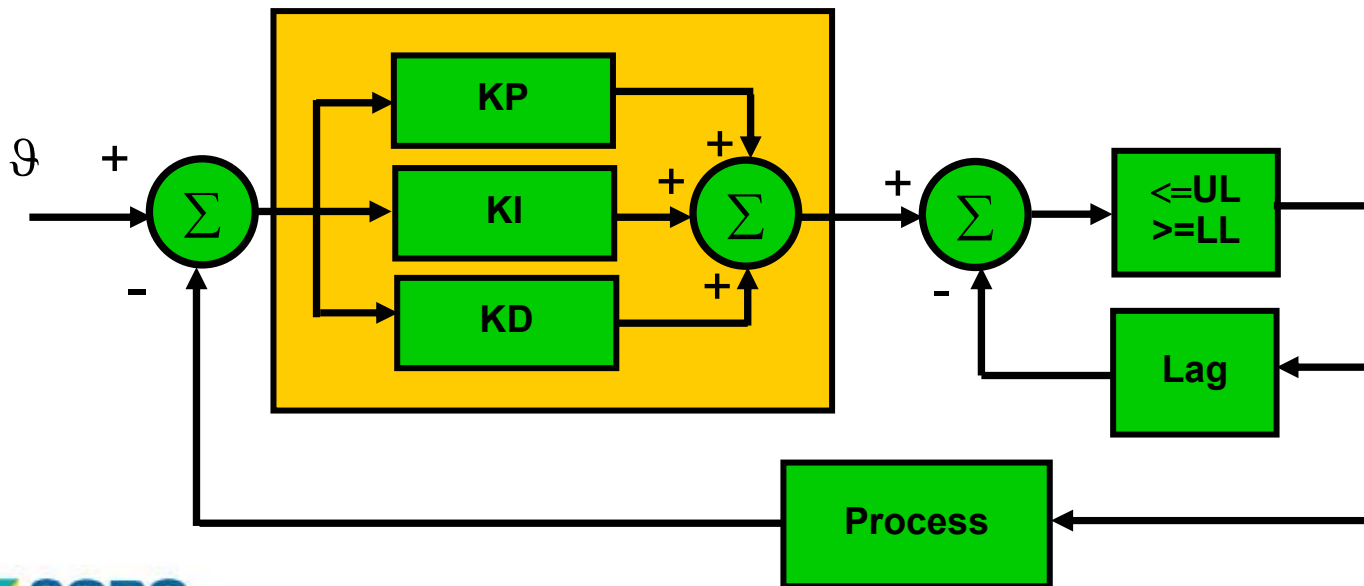
Conceptual Solution

- Industrial Control Flow Diagram
- Hardware Block Diagram
- Software System

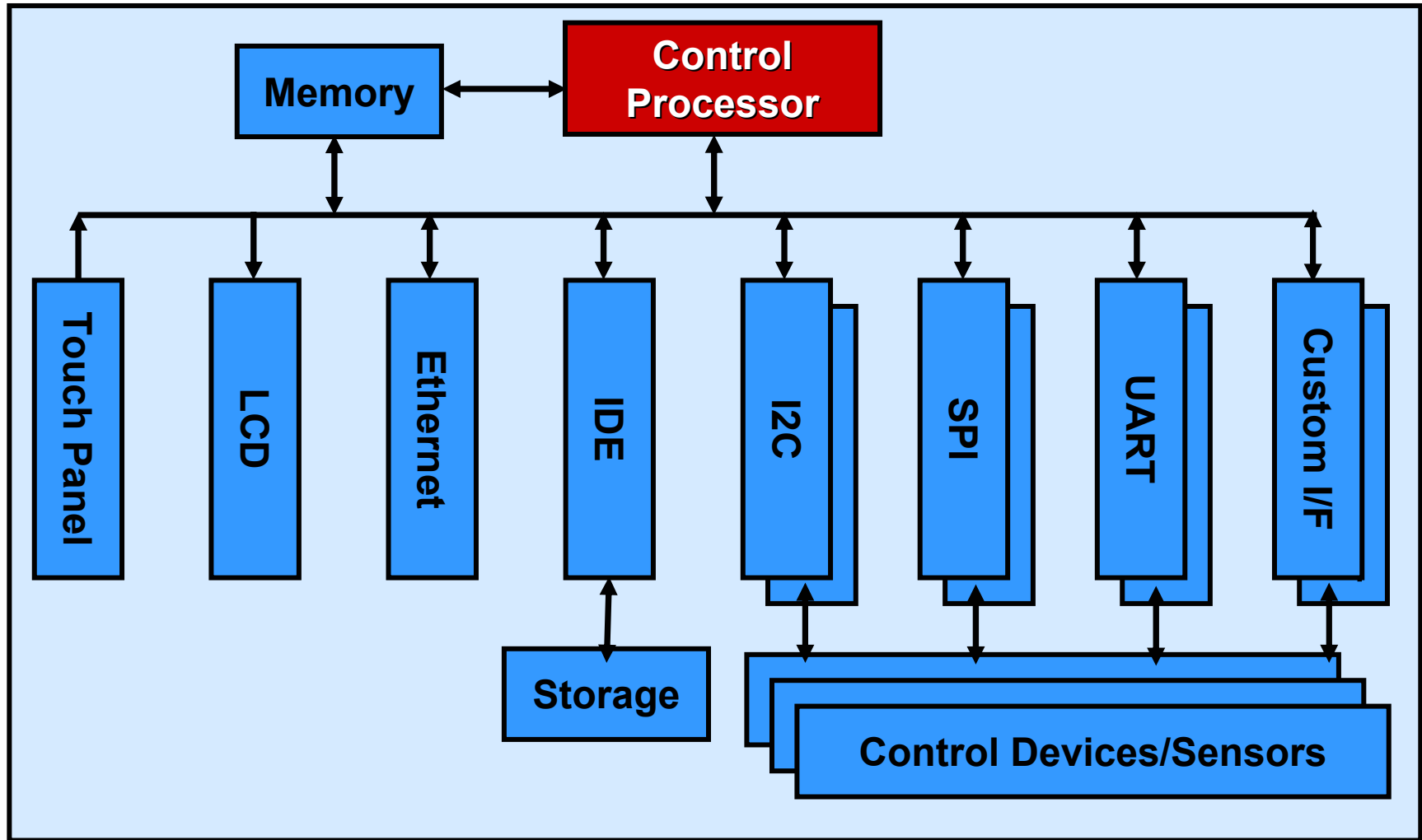
Industrial Control Flow Diagram

- Example: PID Controller
- Typical Transfer Function

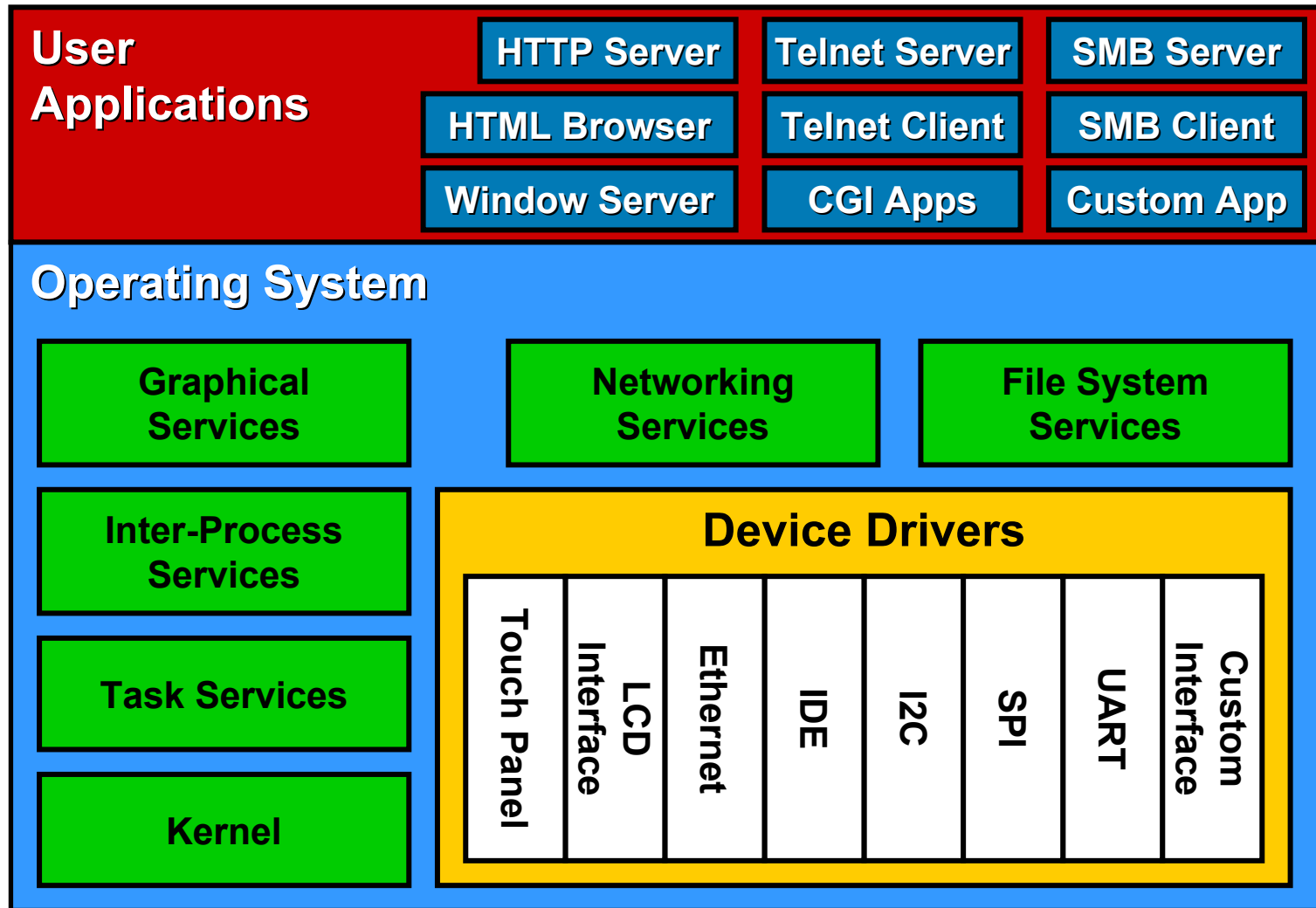
$$\frac{Y(s)}{U(s)} = \frac{K_D s^2 + K_P s + K_I}{(m + K_D)s^2 + (b + K_P)s + K_I}$$



Hardware Block Diagram



Software System



Implementation

- Selected System Components
 - Cyclone FPGA
 - Nios Embedded Processor
 - μ CLinux Software
- Solution Development

Cyclone FPGA

■ Advantages

- High-Density, Full-Featured FPGA
 - Maximizes Flexibility, Avoids Obsolescence & Device Qualification Issues
- Low Cost
 - Reduces Production Costs without Reducing Solution Functionality
- High Performance
 - Maximizes Longevity of Solution & Functional Economy
- Migration Path
 - Enables Same Board to Be Used for Different Solutions
- Enables High Levels of Integration
 - Minimizes Component Count & Board Costs

Powerful Cyclone Functionality

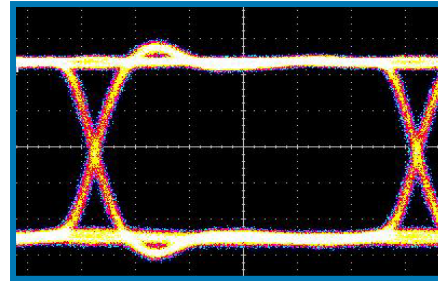
External Memory Interface

- Dedicated SDRAM & FCRAM Interface Circuitry
- 266-Mbps Performance



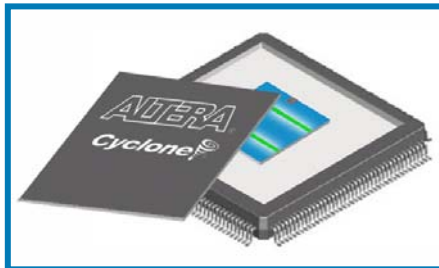
Differential Signaling

- 311-Mbps Performance
- Up to 129 Channels



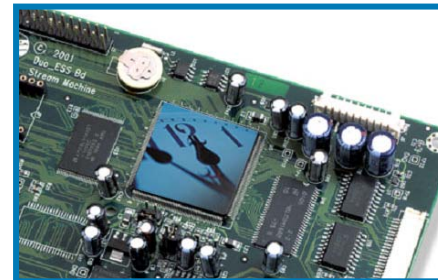
Embedded Memory

- Up to 294,912 RAM Bits
- 200-MHz Performance



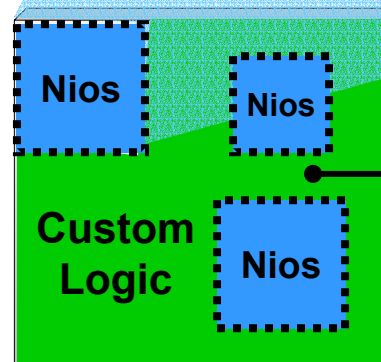
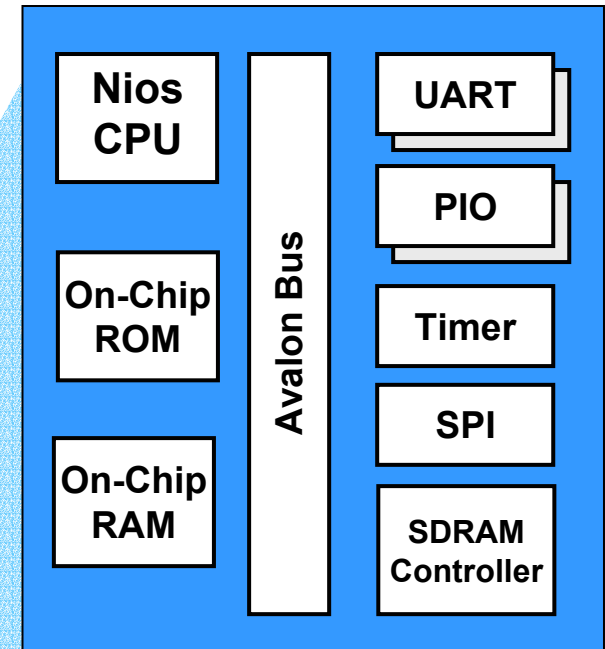
Phase-Locked Loops

- System Clock Management Features
- Up to 2 PLLs



Nios Processor Systems

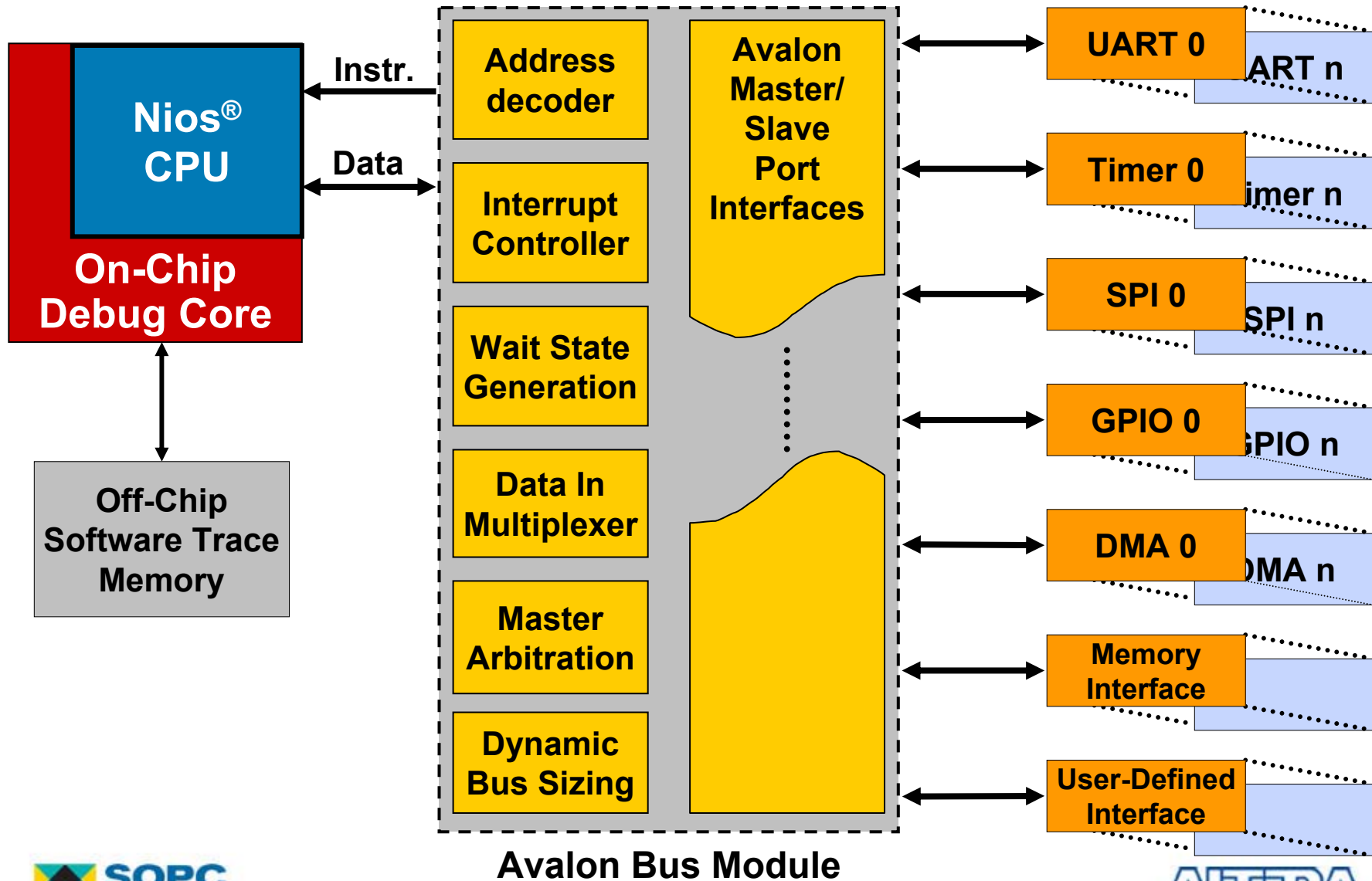
- Not Just A Processor
 - Complete Microprocessor Subsystem
- Processor Core Plus Peripherals & Memory Interfaces
- Custom Peripherals
- Custom Instructions
- Simultaneous Multi-Master Avalon™ Bus Connects All Components
- Multiprocessor Systems Possible



***Your Design
Here***

PIO: Parallel I/O
SPI: Serial Peripheral Interface

Nios System Architecture



Peripheral Components

■ Memory Interface

- On-Chip
 - RAM, ROM
- Off-Chip
 - SDRAM Controller
 - SSRAM
 - SRAM
 - Flash, ROM

■ DMA Controller

- Memory-Peripheral
- Memory-Memory
- Peripheral-Peripheral

■ Bridges

- AHB to Avalon™ Bus Bridge

■ Parallel I/O (PIO) Registers

- General-Purpose I/O Registers (PIO)
 - Input
 - Output
 - Bidirectional
- User-Defined Interface

■ Serial I/O

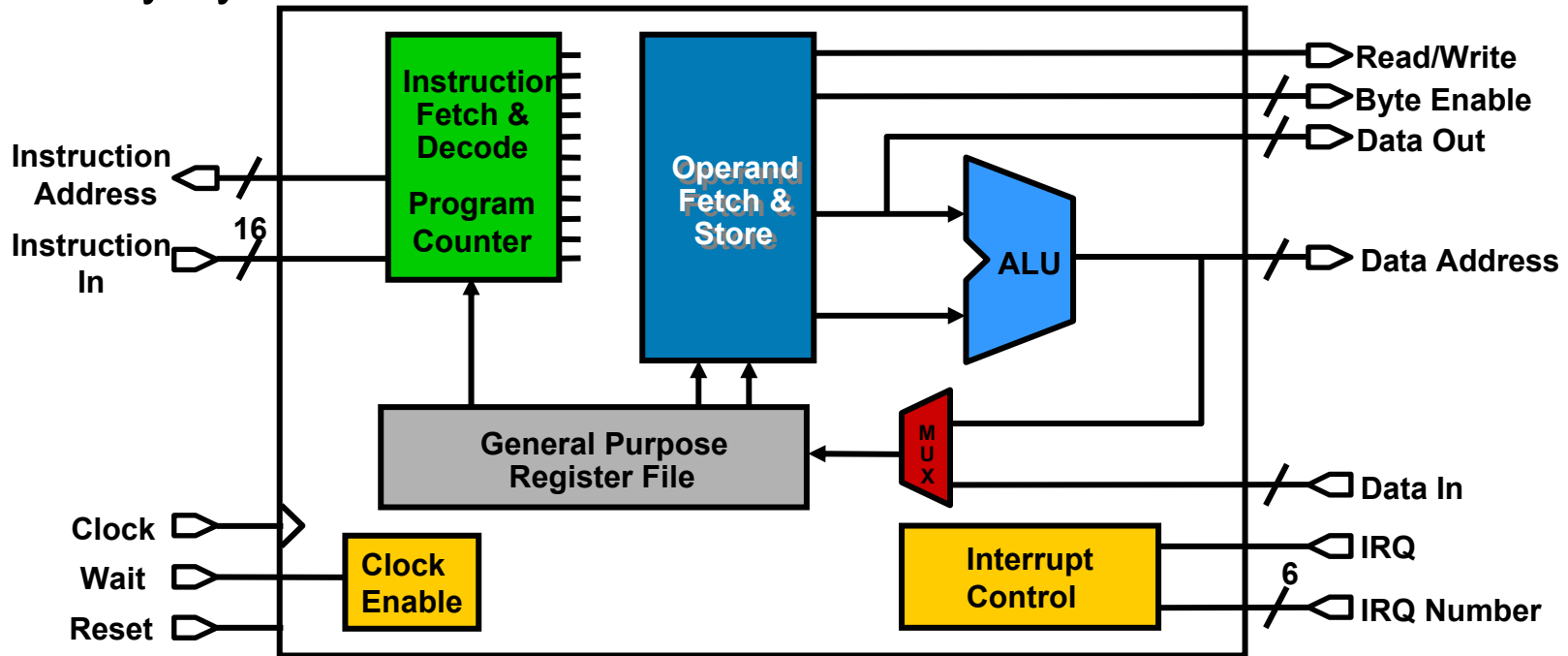
- UART
- SPI

■ Timer

- Simple Timer
- Pulse Generator
- Watchdog Timer

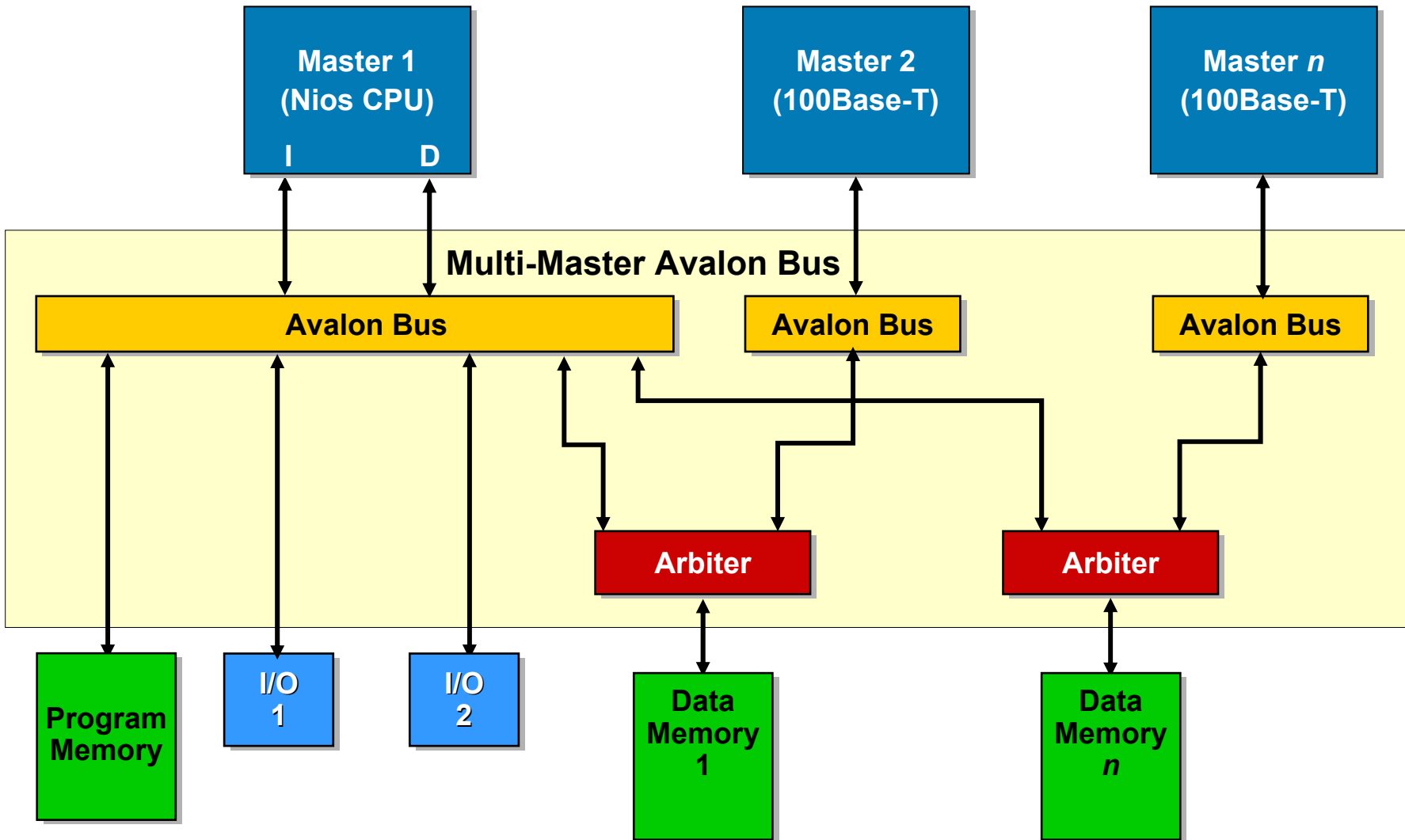
Nios Embedded Processor

- Standard RISC Components
- Optimized for Size & Performance in PLDs
- Fully Synchronous Interface

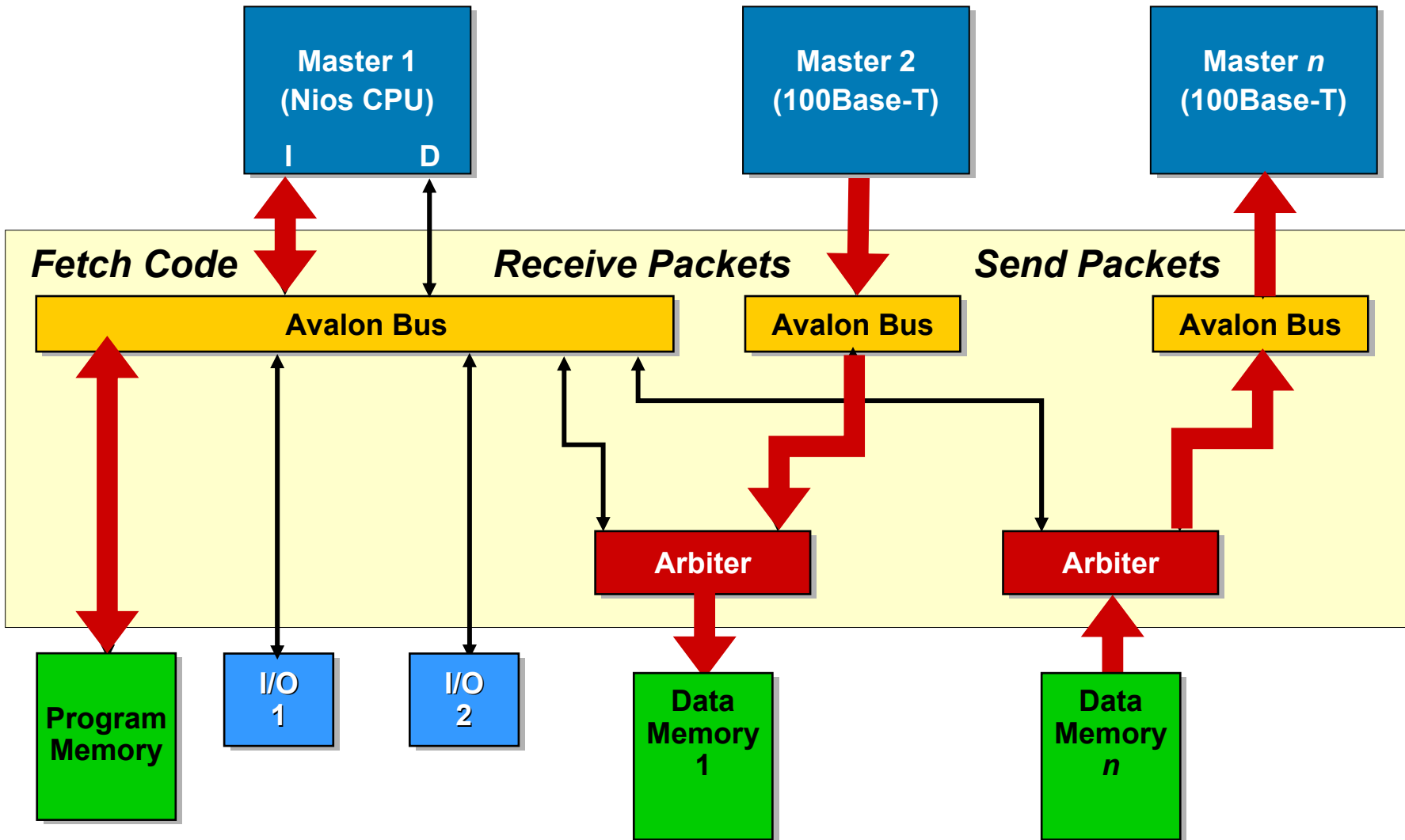


IRQ: Interrupt Request
ALU: Arithmetic Logic
Unit

Simultaneous Multi-Master Bus

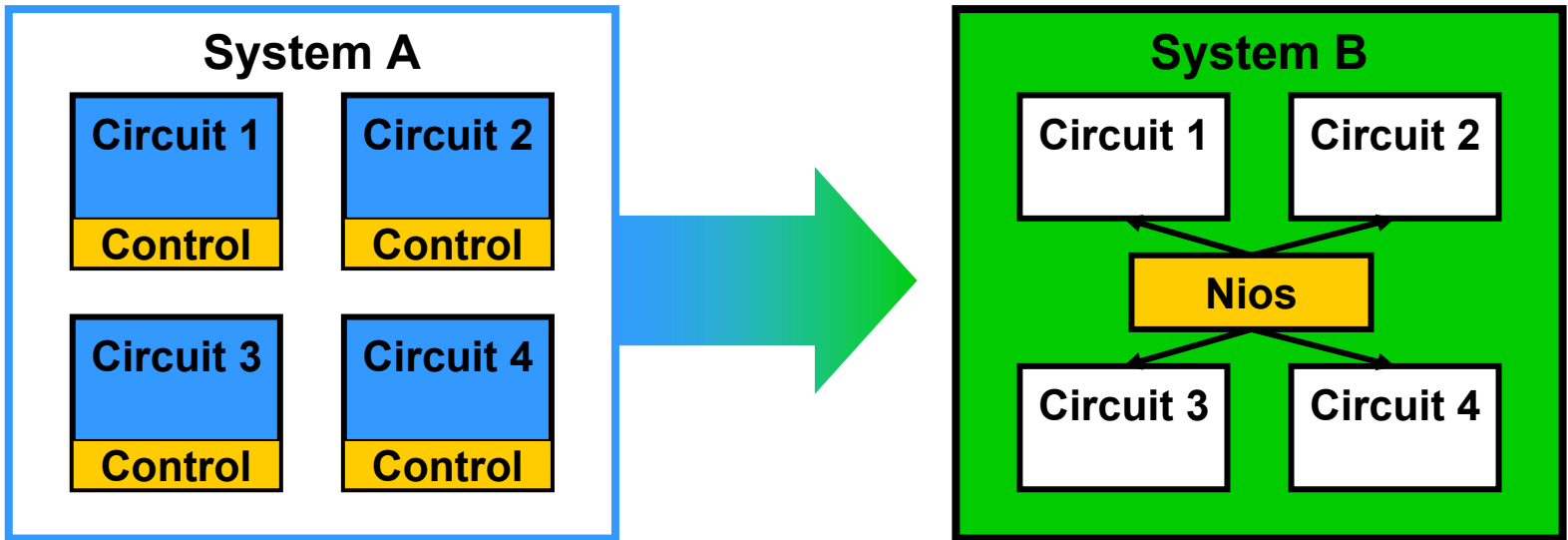


Simultaneous Multi-Master Bus



State Machine/PLC Replacement

System	A	B
Development Complexity	High	Lower
Development Time	High	Lower
Resource Utilization	High	Lower
Design Flexibility	Low	Higher



Nios Embedded Processor

■ Advantages

- Highly Configurable
 - 16-,32-Bit Variants, Add Peripherals as Required
- Optimized For PLD Implementation
 - Minimal Size, Reduces Device Costs
- Royalty Free
 - No per Product Fee
- Low Cost
 - Minimal Investment
- Obsolescence Proof
 - Migration to New Altera® Device Families
 - Longevity Associated with Altera Device Families

μCLinux Software

- Linux 2.4
- C++ Support
- μClibc Embedded Library
- Source Code Provided
- SOPC Builder Support
- Fully Supported in Cygwin Environment



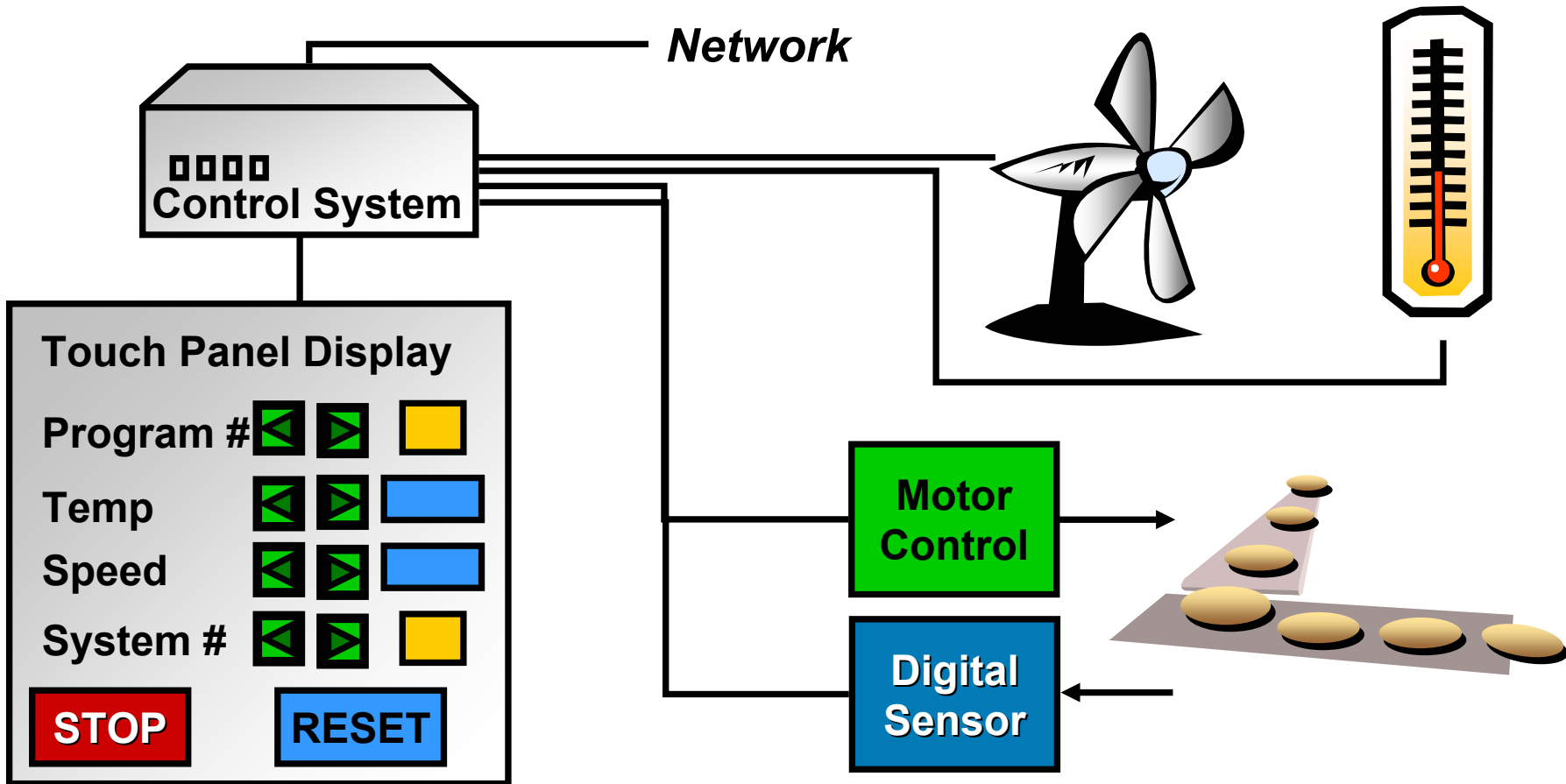
μClinux Software

■ Advantages

- Open Source Environment
- Availability of Solutions Simplifies Development
 - HTTP Server, HTTP Browser, Telnet Server, Telnet Client
- Driver Availability
 - Large Driver Resource
 - Ability to Integrate Custom Drivers
- Integration with Altera Tools
 - Quartus® Software
 - SOPC Builder

Solution Development

■ Example System: Cookie Factory



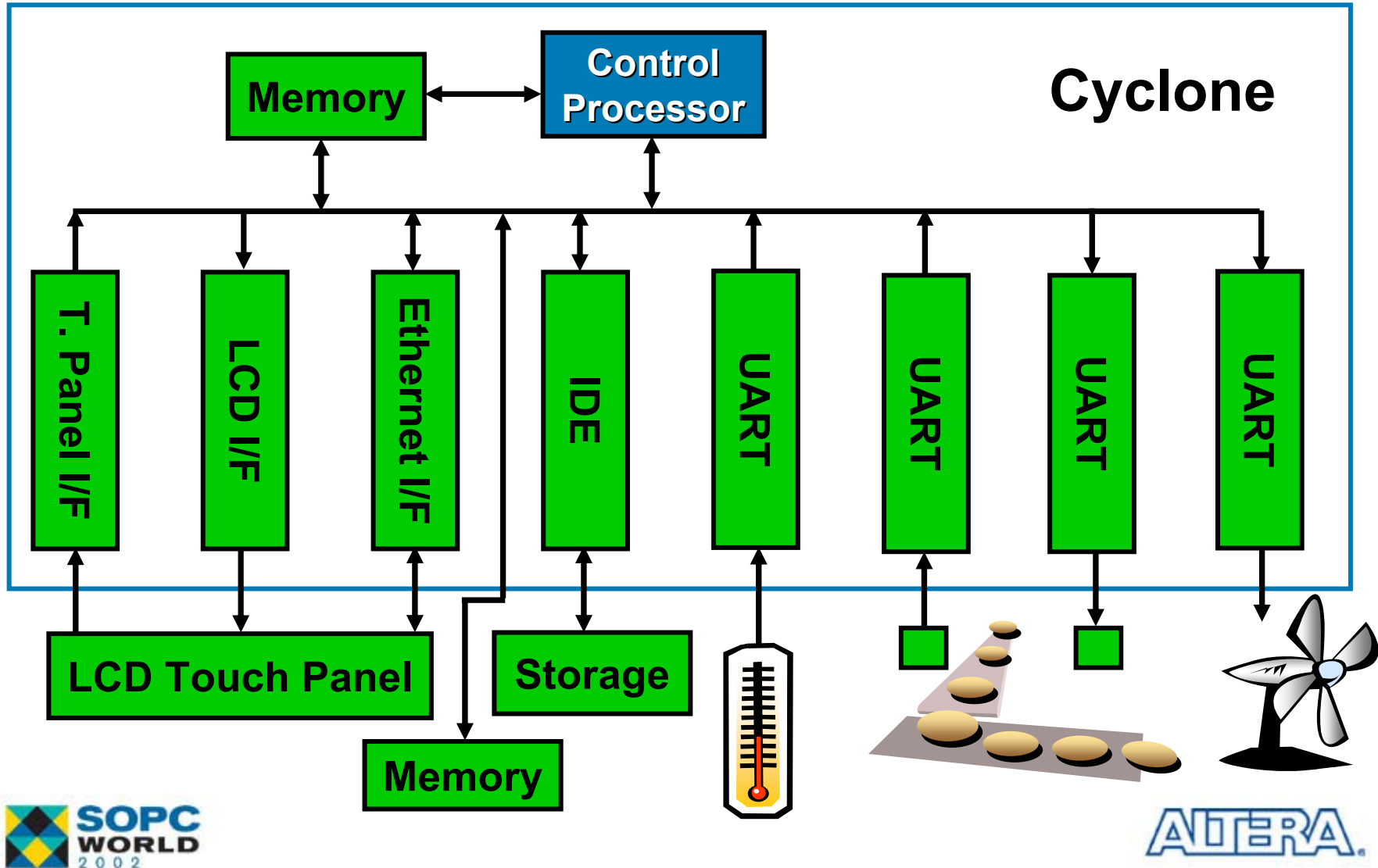
Solution Development

■ Cyclone Logic Element Implementation Cost

Block	LEs
16-Bit Nios	900-1,100
LCD I/F	100-2,500
Touch Panel I/F	200-5,000
Ethernet	100-2,500

Block	LEs
IDE Interface	100-200
Customer Interface	200
UART, SPI, I2C	200-300
CAN	100

Solution Development



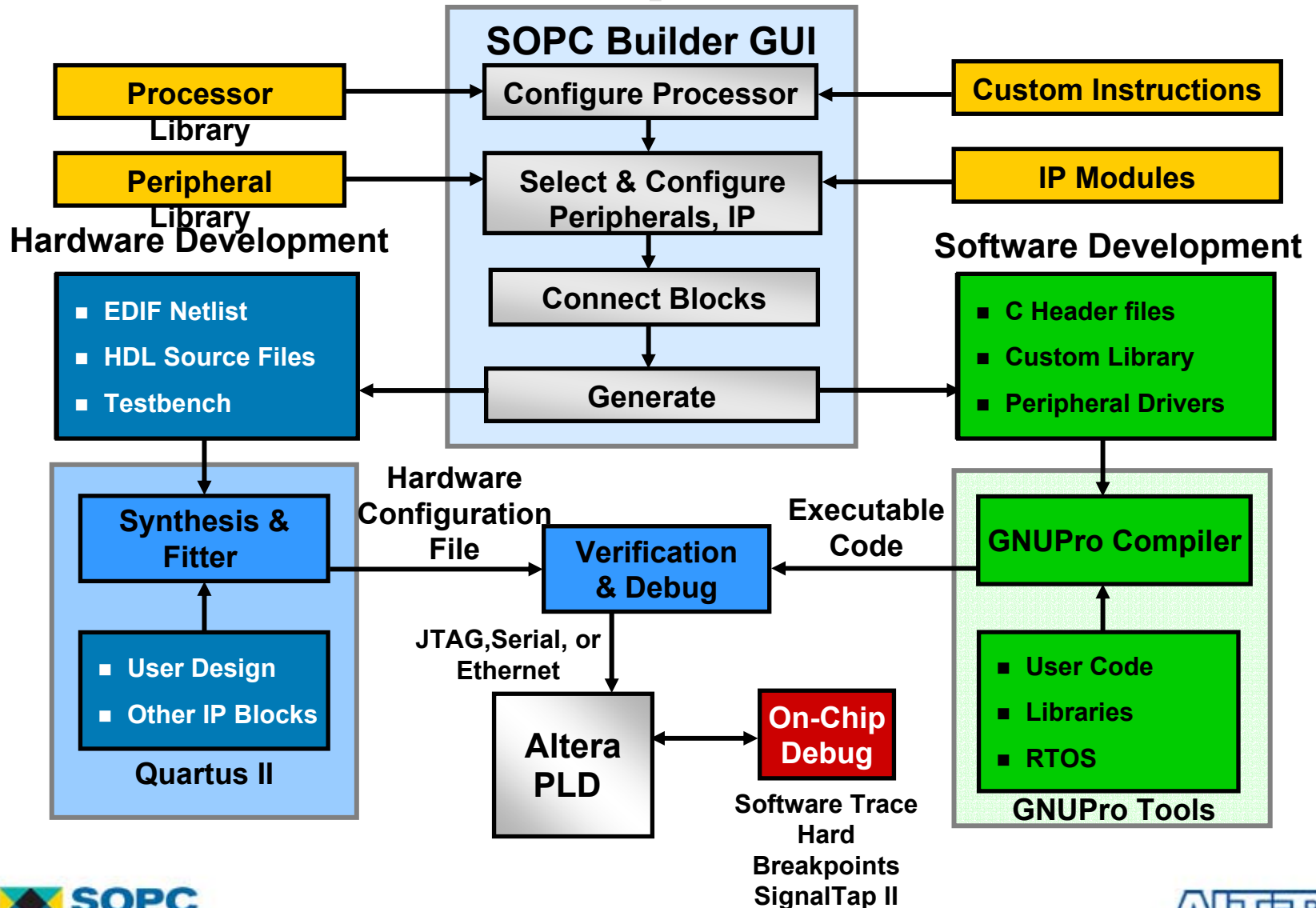
Solution Development

Function	Amount	LE Cost	Total
Processor	1	1,200	1,200
UART	4	300	1,200
Touch Panel Interface	1	500	500
LCD Interface	1	700	700
Ethernet Interface	1	100	100
IDE	1	100	100
Total			3,800

Solution Development

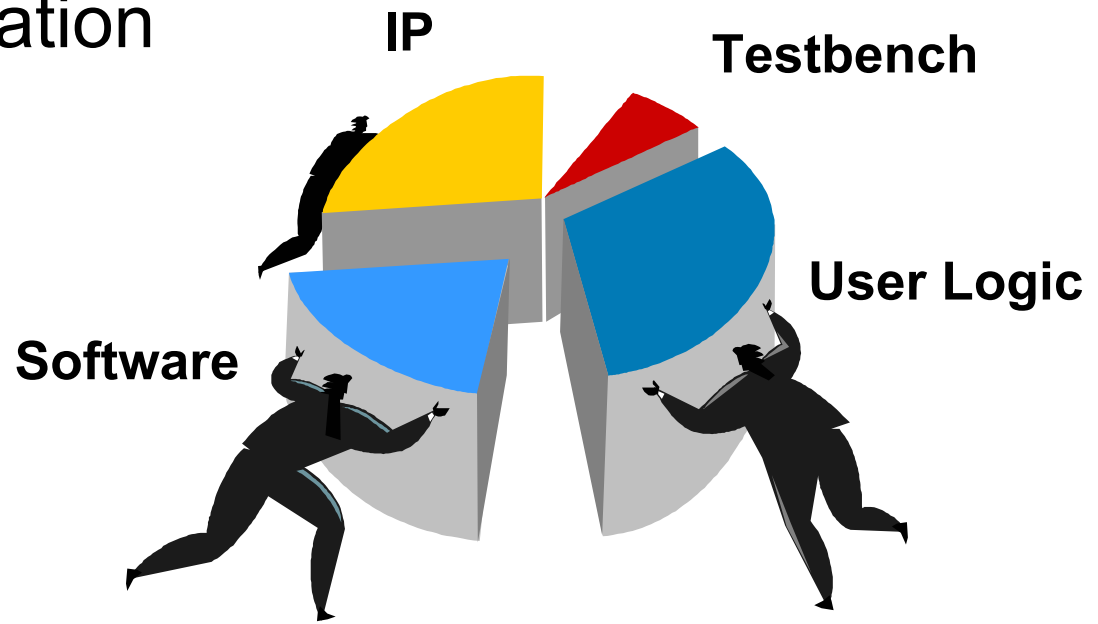
- EP1C6 Has 5,980 Logic Elements
- Solution Requires 3,800 Logic Elements
- Device 63.5% Utilized
- Memory Requirements
 - EP1C6 Has 92,160 RAM Bits
 - External Memory Only for LCD Image Memory
 - 614,400 RAM Bits Required for QVGA

Solution Development

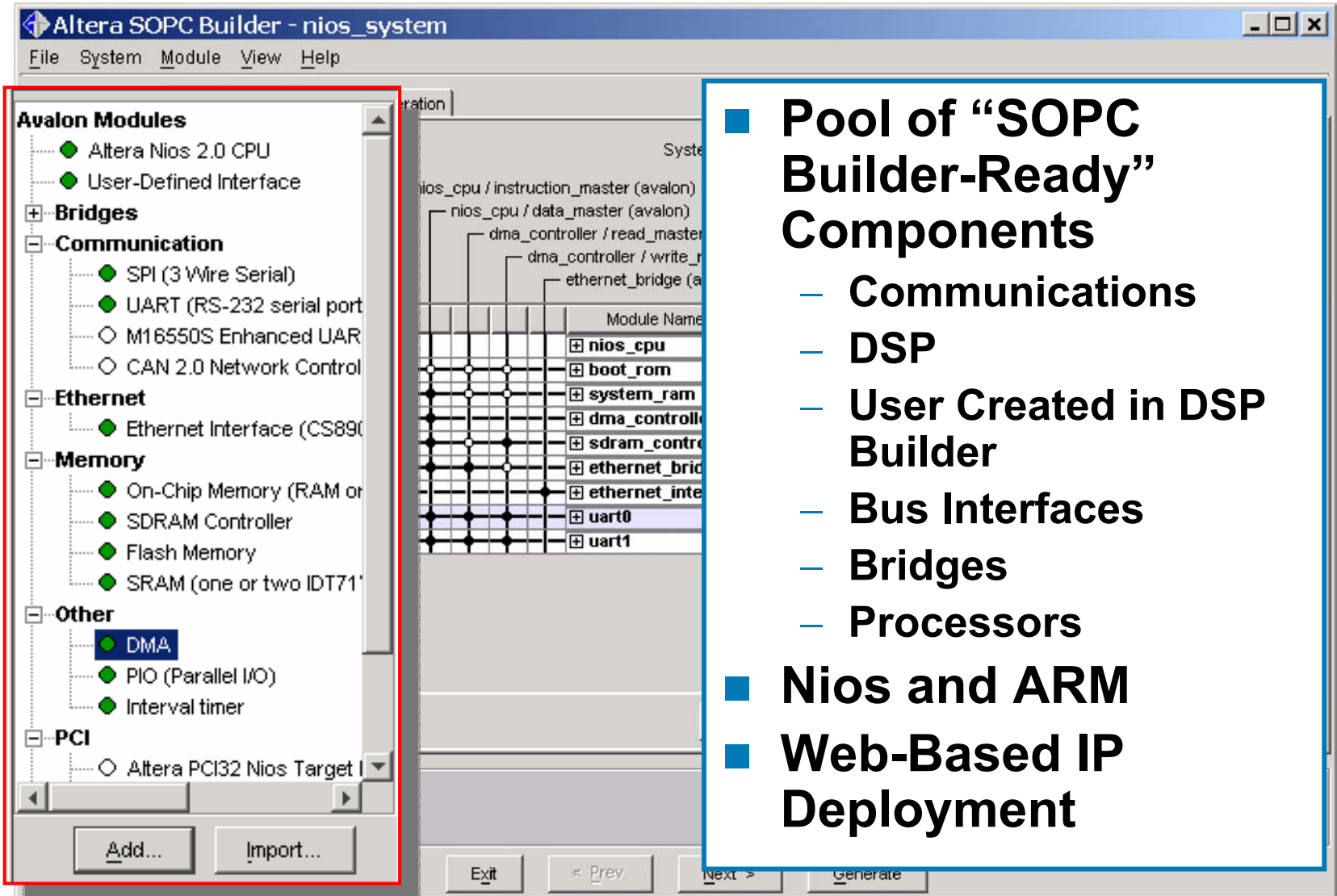


SOPC Builder Design Tool

- System Customization
- Component Integration
- Software Generation
- System Verification



SoPC Builder - Customization



Avalon Modules

- Altera Nios 2.0 CPU
- User-Defined Interface
- Bridges**
- Communication**
 - SPI (3 Wire Serial)
 - UART (RS-232 serial port)
 - M16550S Enhanced UAR
 - CAN 2.0 Network Control
- Ethernet**
 - Ethernet Interface (CS89C01)
- Memory**
 - On-Chip Memory (RAM or ROM)
 - SDRAM Controller
 - Flash Memory
 - SRAM (one or two IDT71V08)
- Other**
 - DMA**
 - PIO (Parallel I/O)
 - Interval timer
- PCI**
 - Altera PCI32 Nios Target Interface

Pool of “SOPC Builder-Ready” Components

- Communications
- DSP
- User Created in DSP Builder
- Bus Interfaces
- Bridges
- Processors

Nios and ARM

Web-Based IP Deployment

SoPC Builder - Customization

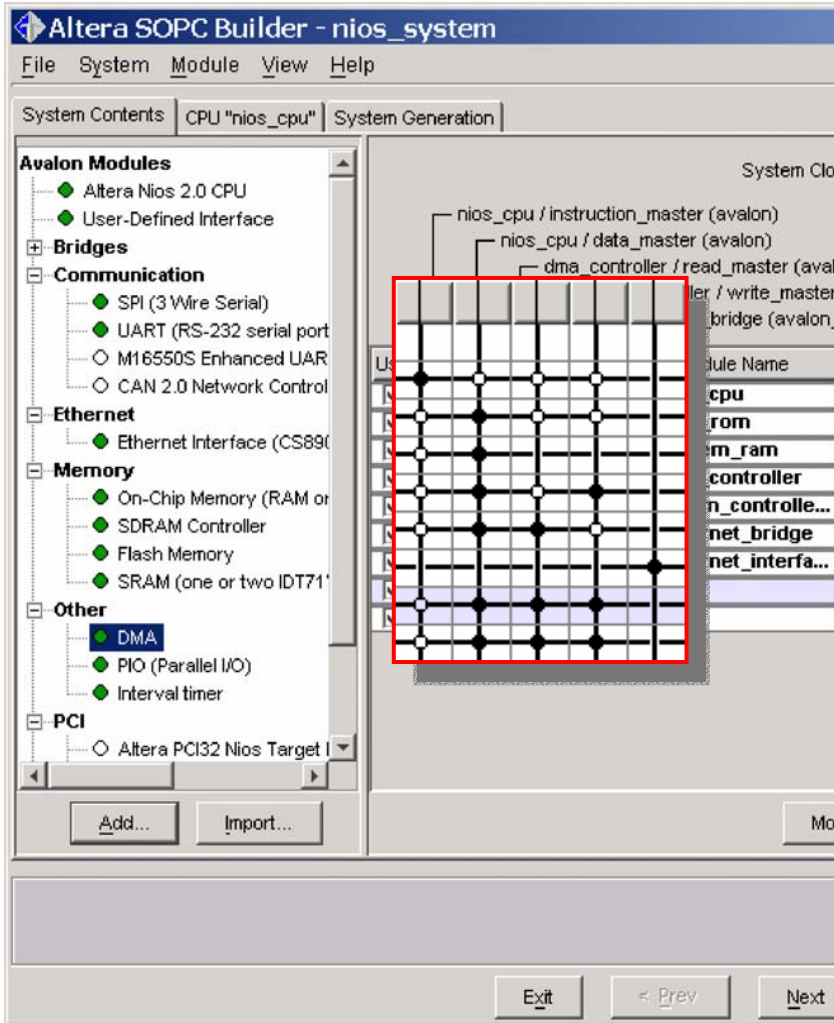
- **Table of Active Components**
- **Configure Each Component**
 - Interrupt Request (IRQ)
 - Base Address
 - Hardware Parameters
 - Software Parameters
- **Wizard-Based Configuration**

The screenshot displays the Altera SOPC Builder interface for a system named 'nios_system'. The 'System Contents' pane on the left shows a tree of components including 'nios_cpu', 'boot_rom', 'system_ram', 'dma_controller', 'sdram_controller', 'ethernet_bridge', 'ethernet_interface', 'uart0', and 'uart1'. A red box highlights the 'uart0' and 'uart1' components, and a red arrow points from this box to the 'Avalon UART - uart_0' configuration dialog.

The 'Avalon UART - uart_0' dialog is open, showing the 'Configuration' tab. The 'Baud Rate' section is expanded, showing a 'Baud Rate (bps)' dropdown set to '115200', an 'Input Clock Frequency (MHz)' of '33.333', and a 'Baud error' of '0.12%'. There is an unchecked checkbox for 'Baud rate can be changed by software (divisor register is writeable)'. The 'parity' is set to 'None', 'data bits' to '8', and 'stop bits' to '1'. The 'Flow Control' section has an unchecked checkbox for 'Include CTS/RTS pins and control register bits'. The 'Streaming Data (DMA) control' section has an unchecked checkbox for 'Enable streaming data'. At the bottom, it shows 'LEs: 157'.

Module Name	Description
nios_cpu	Altera Nios 2.0 CPU
boot_rom	On-Chip Memory (f
system_ram	On-Chip Memory (f
dma_controller	DMA
sdram_controller	SDRAM Controller
ethernet_bridge	Avalon Ethernet Bridge
ethernet_interface	Avalon Ethernet Interface
uart0	UART (RS-232 ser
uart1	UART (RS-232 ser

SoPC Builder - Integration



- **Bus Connection Patch Panel**
- **Multi-Master Bus**
 - Slave-Side Arbitration
 - Optimized for Throughput
- **Bus Bridging**
 - AMBA™ Advanced High-Performance Bus (AHB)
 - Avalon™ Bus
 - Atlantic™ Interface
 - PCI

Nios OS / RTOS Support

Provider	Product	Description
Accelerated Technology	Nucleus PLUS	Royalty-Free, Source-Available RTOS
Mapusoft Technologies	OSChanger	Tool to Convert pSOS / VxWorks Applications to Nucleus PLUS
Microtronix	μClinux	Open-Source OS
Shugyo Design	KROS	Small-Footprint, Royalty-Free, POSIX-Compliant RTOS
MiSPO Co., Ltd.	NORTi	μITRON 4.0-Compatible Real-Time Kernel



Nios Debug Solutions

Provider	Product	Description
Viosoft	Arriba!	IDE with Integrated Support for Nios On-Chip Debug Module - Hardware Breakpoints & Processor Trace
Microtronix	Debugger Module	External Memory Daughter Card for Use as Software Trace Capture Buffer
Microtronix	OCD Solutions Kit	Insight (gdb) Debugger Enhanced to Support Hard Breakpoints & Software Trace
Sophia Systems	WatchPoint	Full-Featured Debug Environment with Advanced On-Chip Debug Support
Red Hat	GDB / Insight*	Software Debugger
Altera	Tracelink*	Interface to Nios On-Chip Debug Module Hardware Breakpoints & Processor Trace

* Included in Nios Development Kit



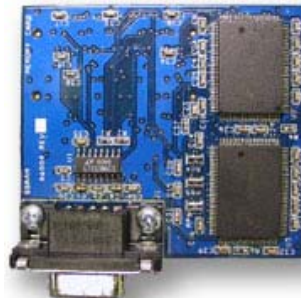
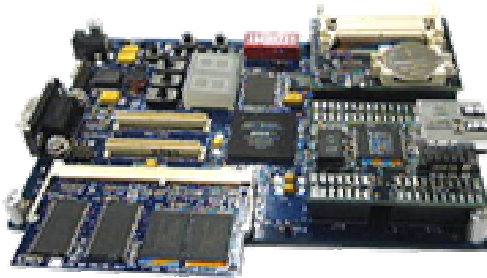
Nios Development Kits

■ Altera

- 10/100 Ethernet Development Kit
- PCI Development Kit
 - 32-Bit 33-MHz PCI Master/Target
 - PCI Bus Hosting Features

■ Third Party

- Linux Development Kit
 - IDE Interface
 - Compact Flash
 - SDRAM Controller
- VGA/LCD Touchscreen
- ADC/DAC Analog Module
- ACEX EP1K100 Development Kit



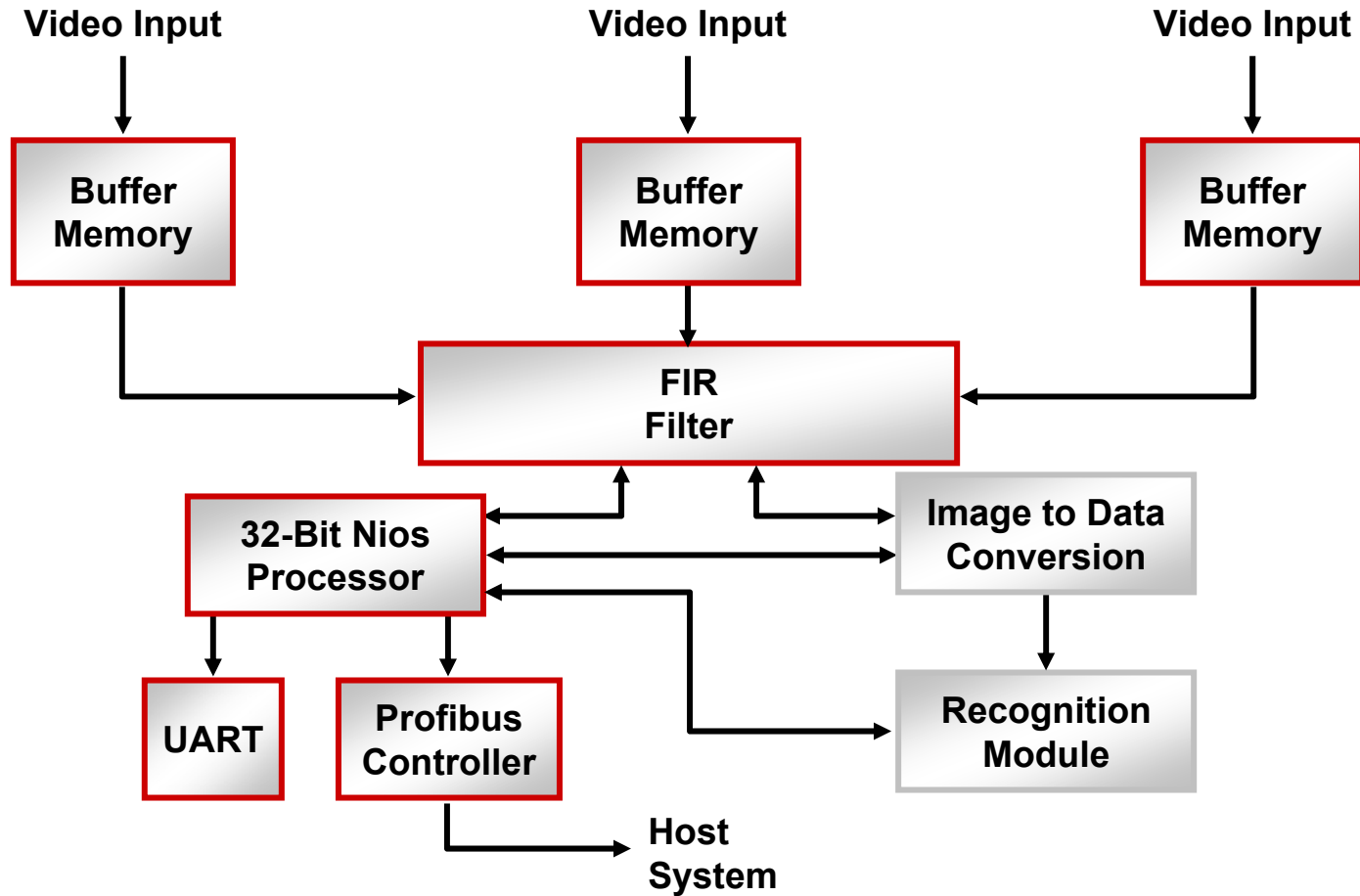
The List Keeps Growing . . .



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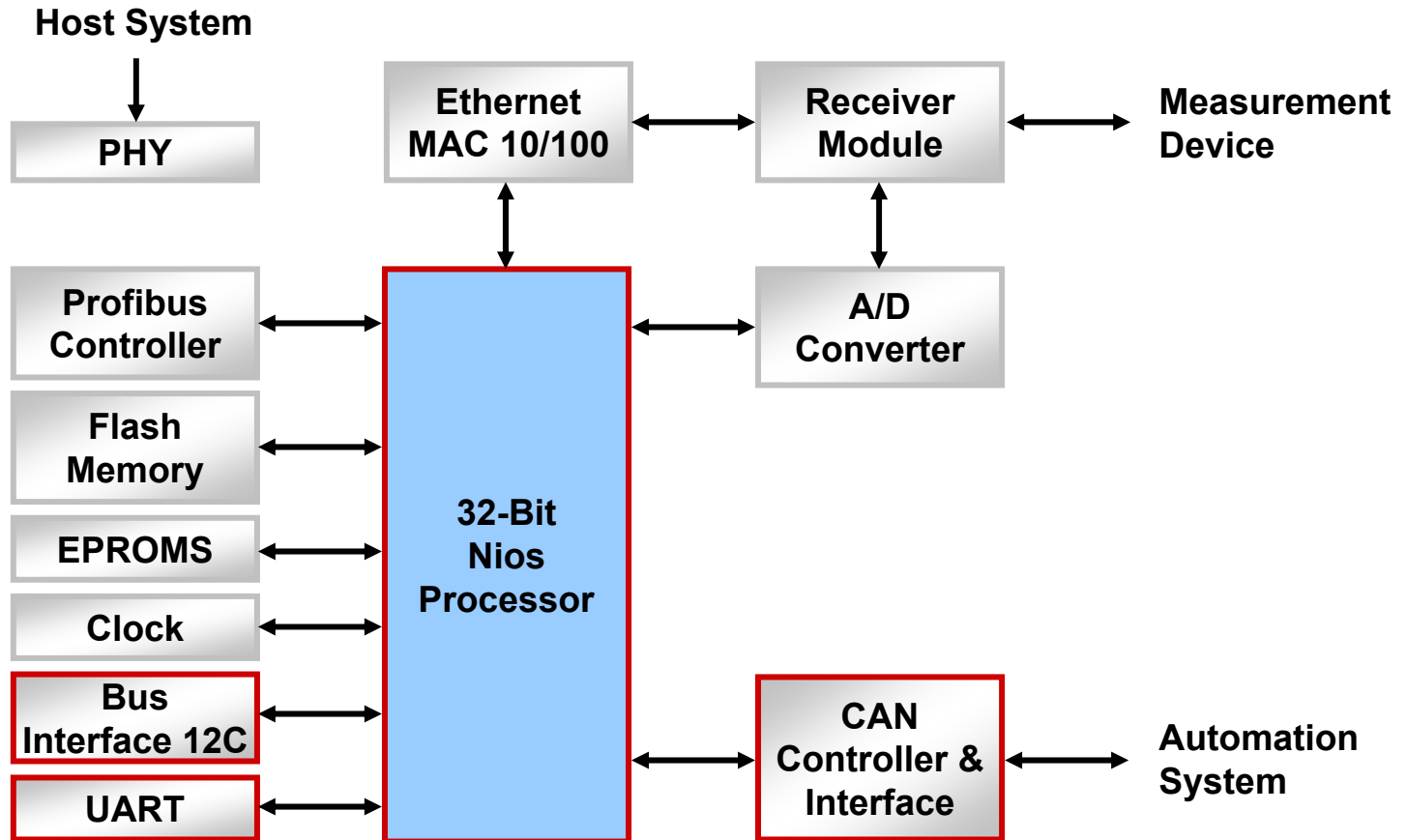
Other Industrial Applications

Factory Automation System



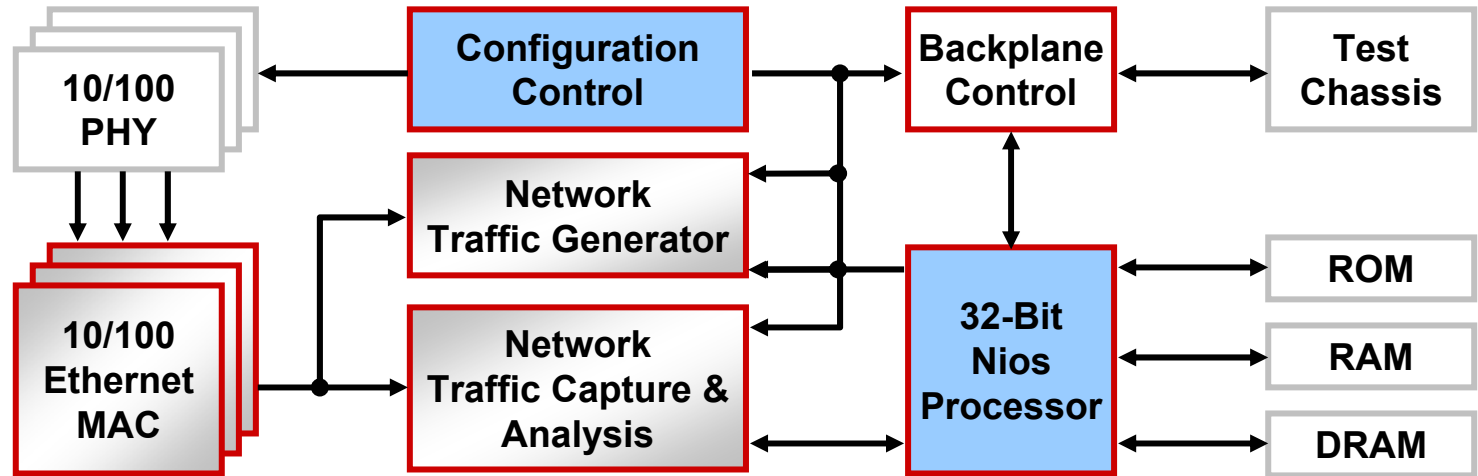
 System in Cyclone

Process Control System



 System in Cyclone

Network Test Equipment System



 System in Cyclone

Summary & Conclusions

- Provides Best All-Round Solution
- Addresses Major Design & Implementation Issues
 - Design Considerations
 - Flexibility
 - ✓ ● Time to Market
 - ✓ ● Reusability
 - Solution Requirements
 - Minimal Cost
 - ✓ ● Manufacturability
 - ✓ ● Device Qualification
 - ✓ ● Remote Accessibility
- Multiple Applications