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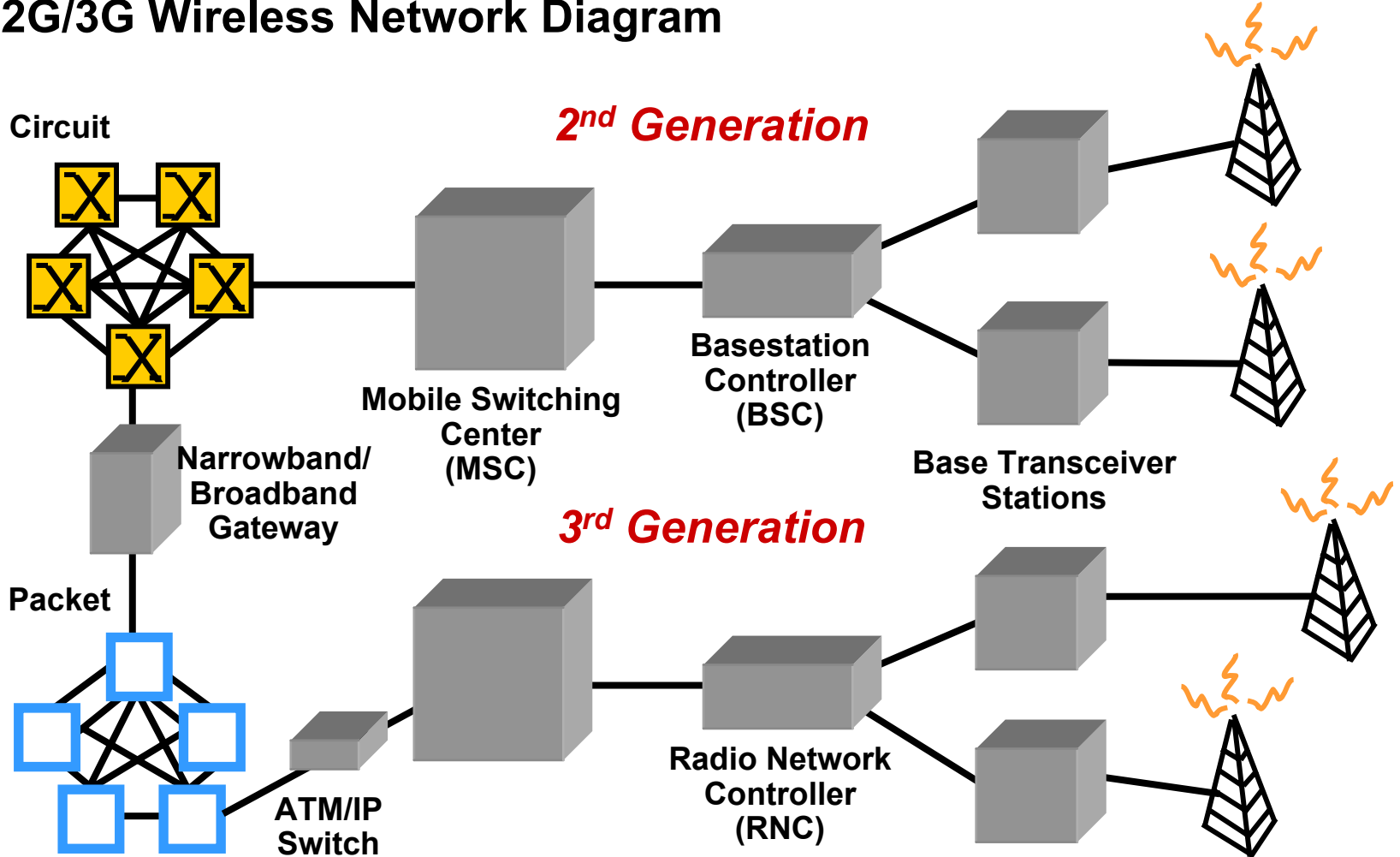


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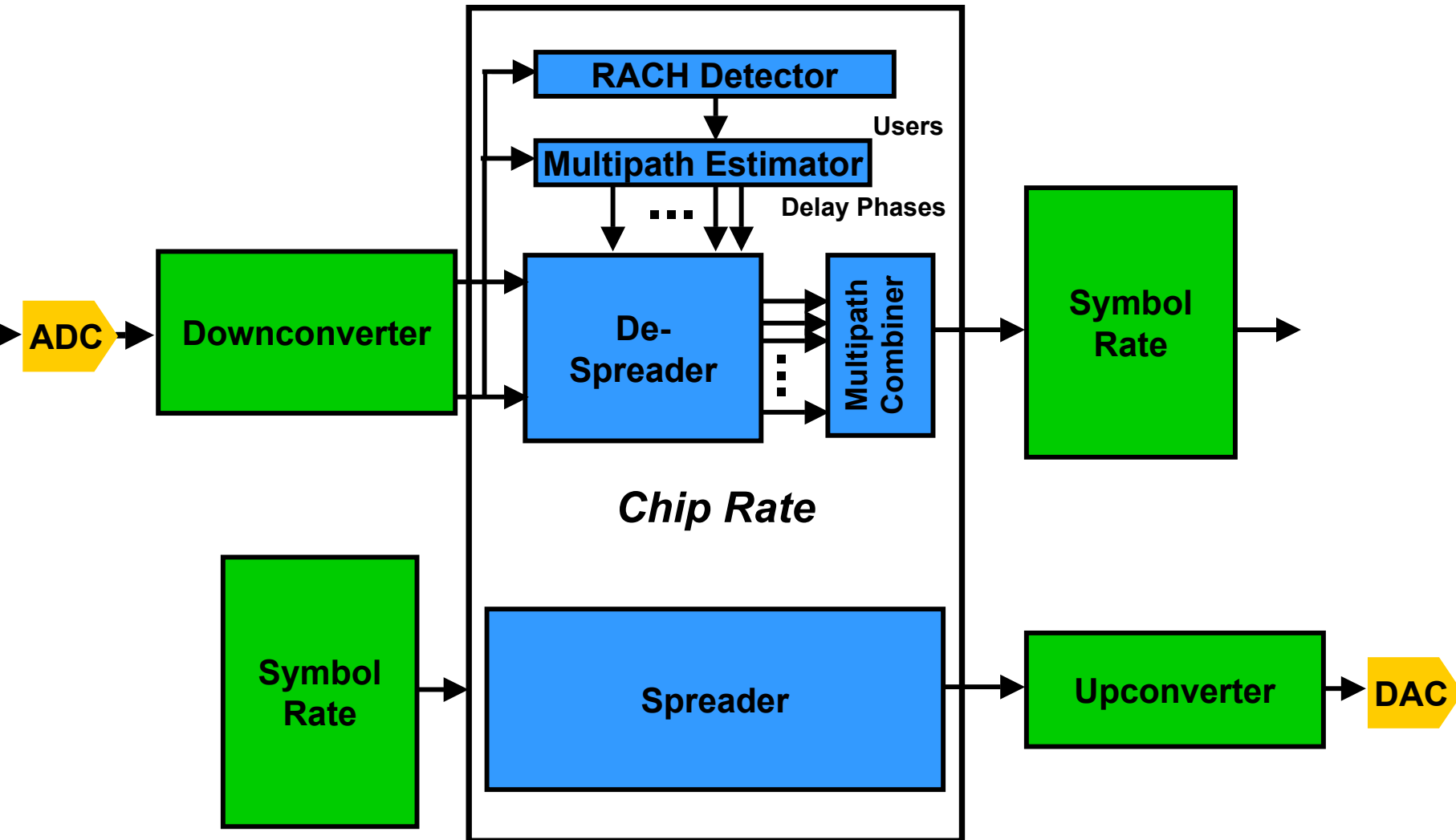
3G Modem Chip Rate Processing Design

3G Mobile Infrastructure

2G/3G Wireless Network Diagram



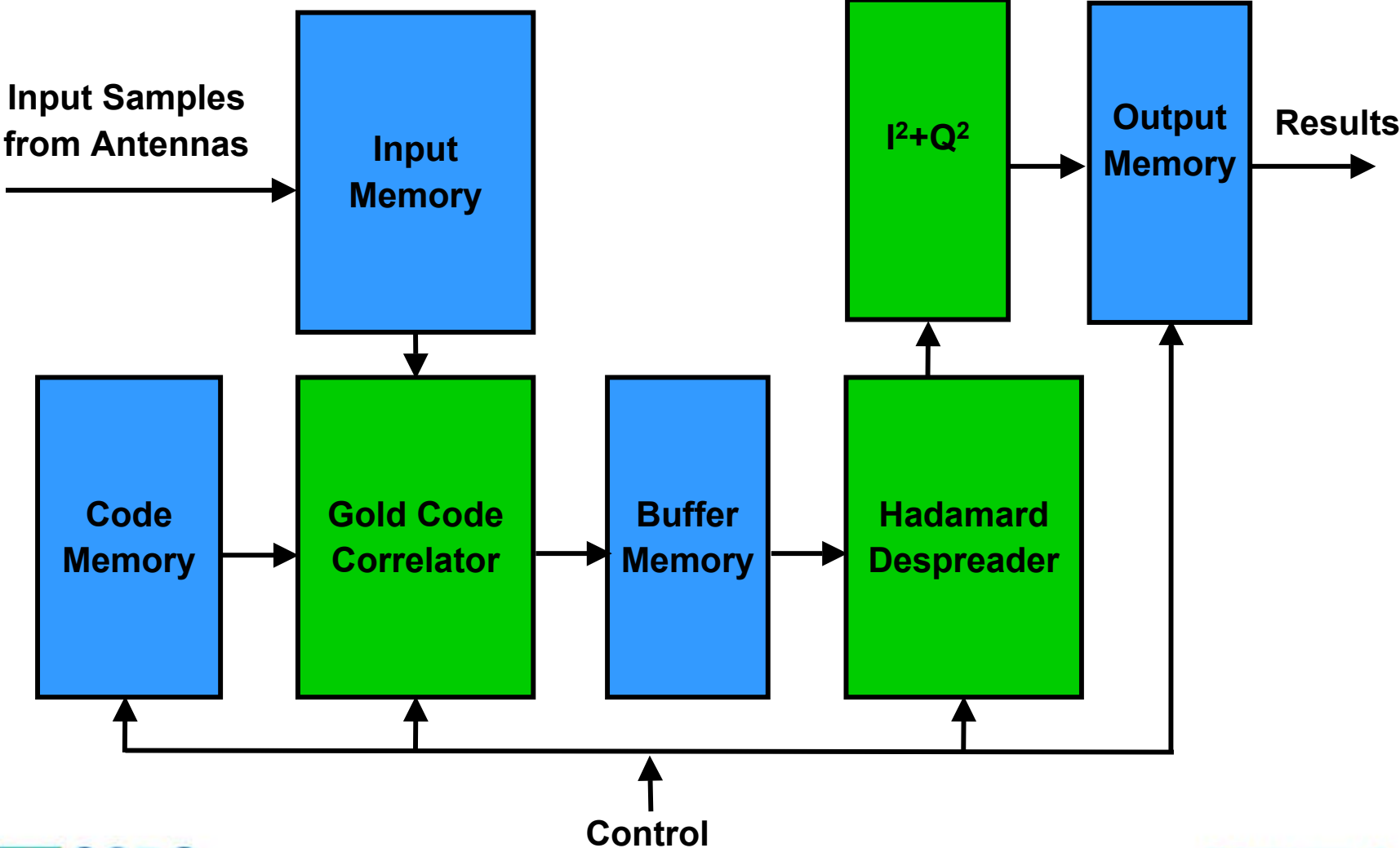
BTS Functions in 3G Basestation



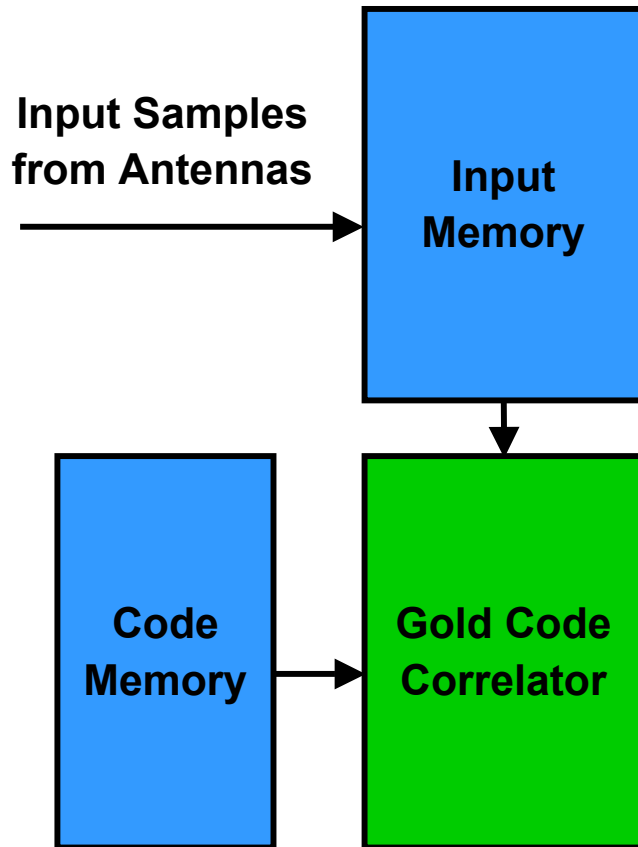
3G Chip Rate Design

- 3G Chip Rate Solutions Need to Hit Certain Objectives:
 - Performance (122.8+ MHz)
 - Density (32+ Users per Board)
 - Low Deployment Costs
- Some Companies Migrate from FPGAs to ASICs to Reduce Device Cost, But
 - Difficult to Keep up with Rapidly Evolving Standards
 - Total Cost of ASIC Solutions Not Taken into Account
 - Non-Recurring Engineering Fees (NREs)
 - Development Time
 - Revenue Impact
- Case Study Shows Stratix™ & HardCopy™ Devices Meet All Objectives

RACH Detector

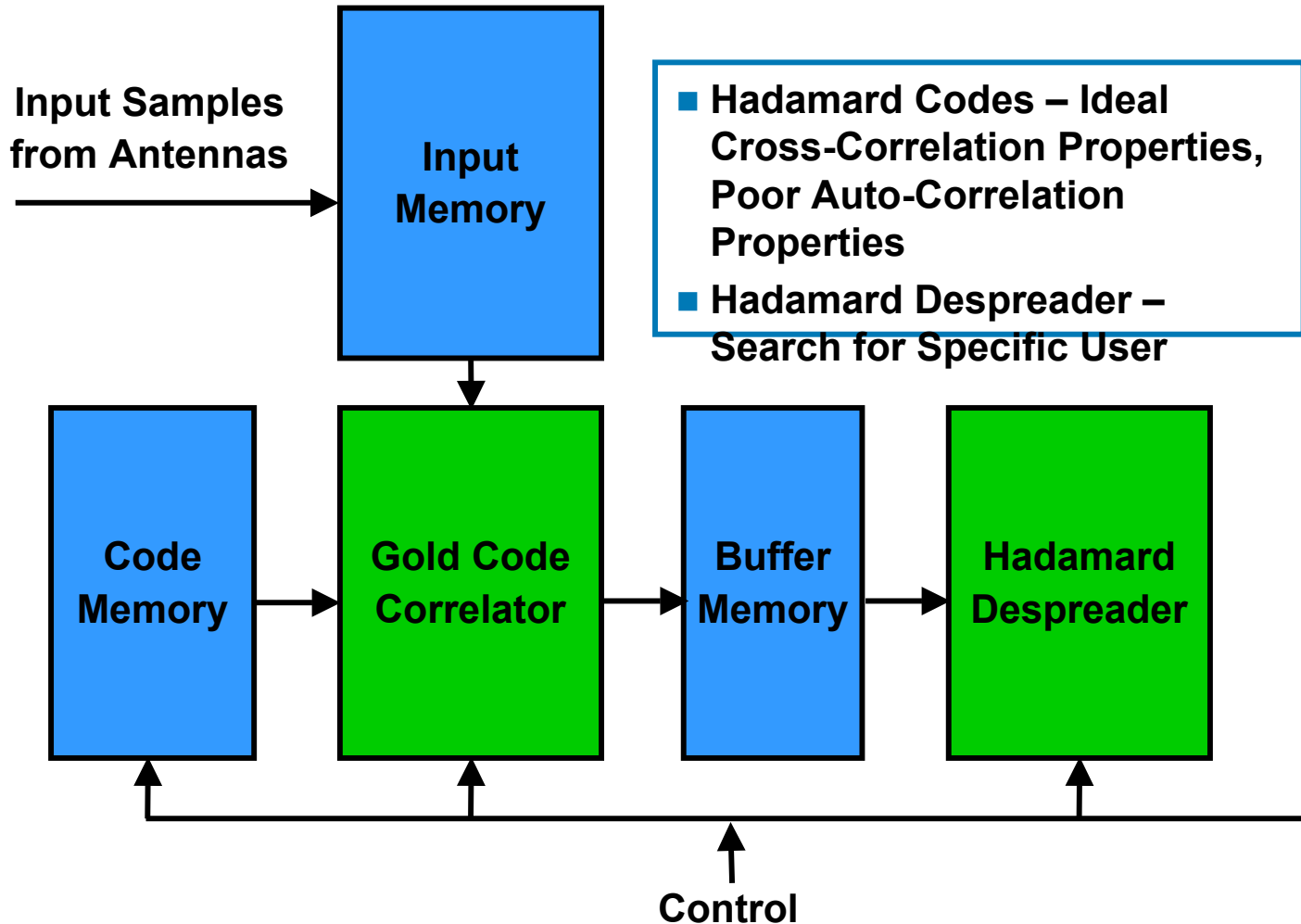


RACH Detector



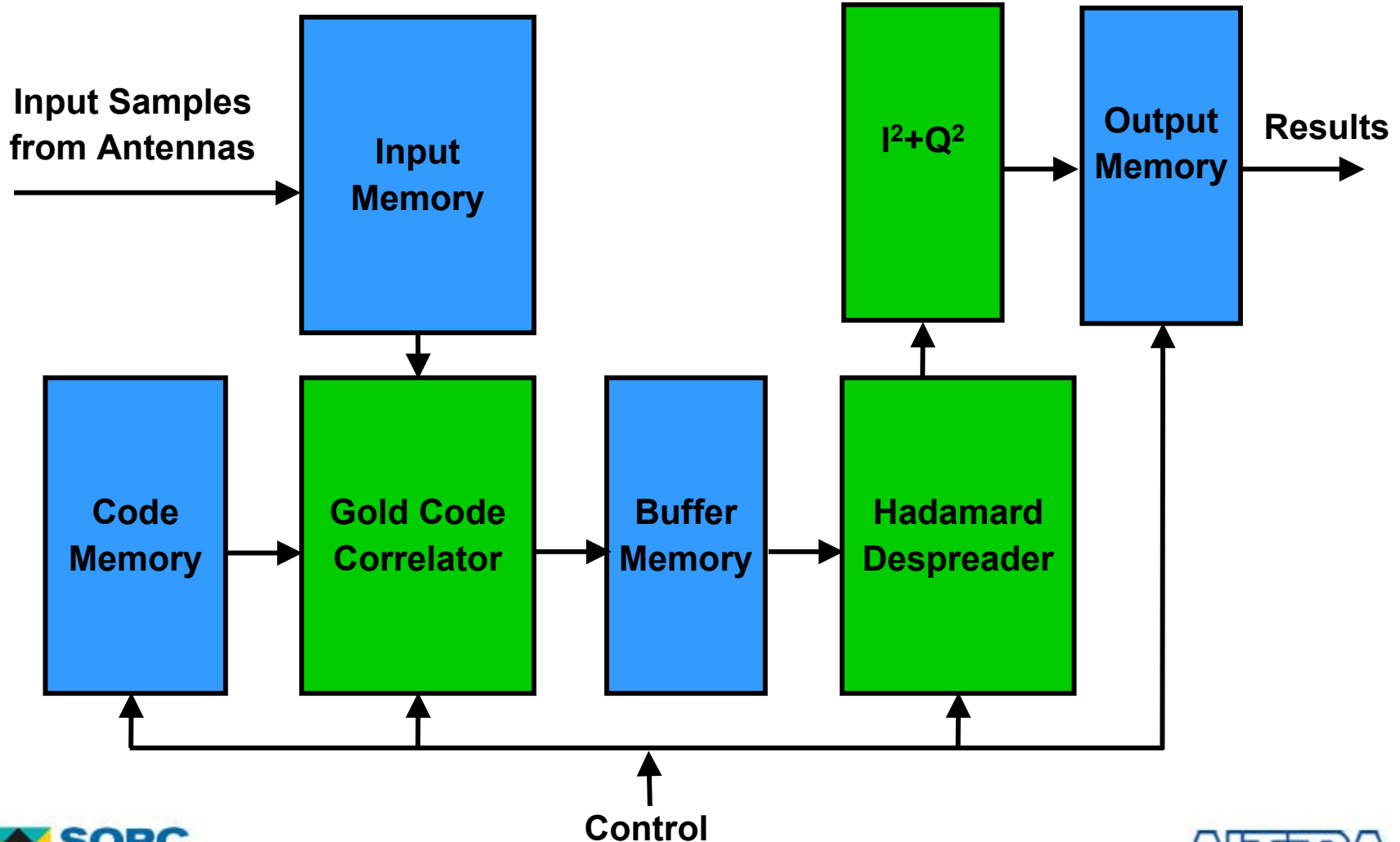
- Gold Codes – Random Noise Codes
- Good Cross-Correlation Properties
- Good Auto-Correlation Properties
- Gold Code Correlator – Compares Received Samples from Users (Handsets) against Locally Generated Gold Codes

RACH Detector

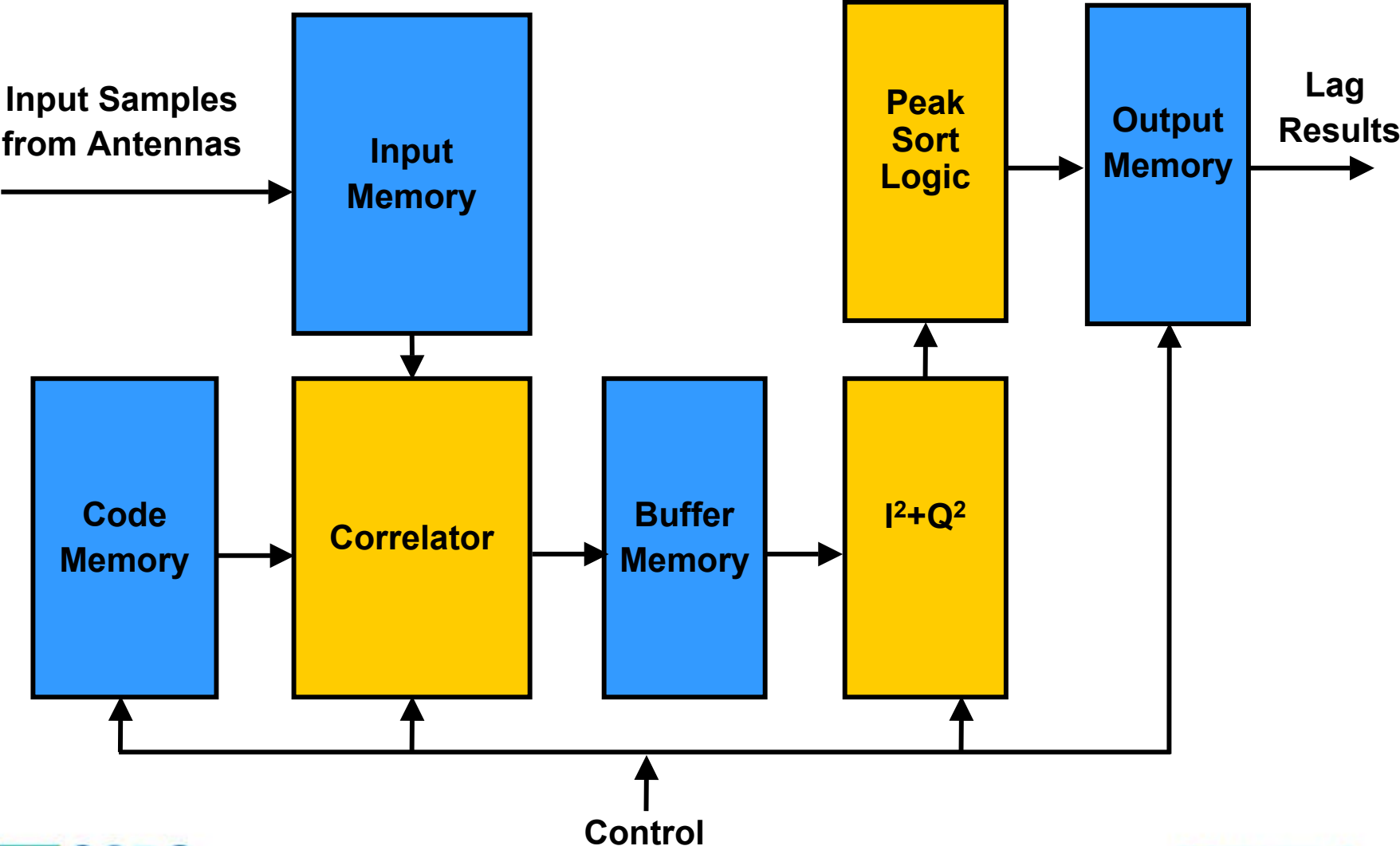


RACH Detector

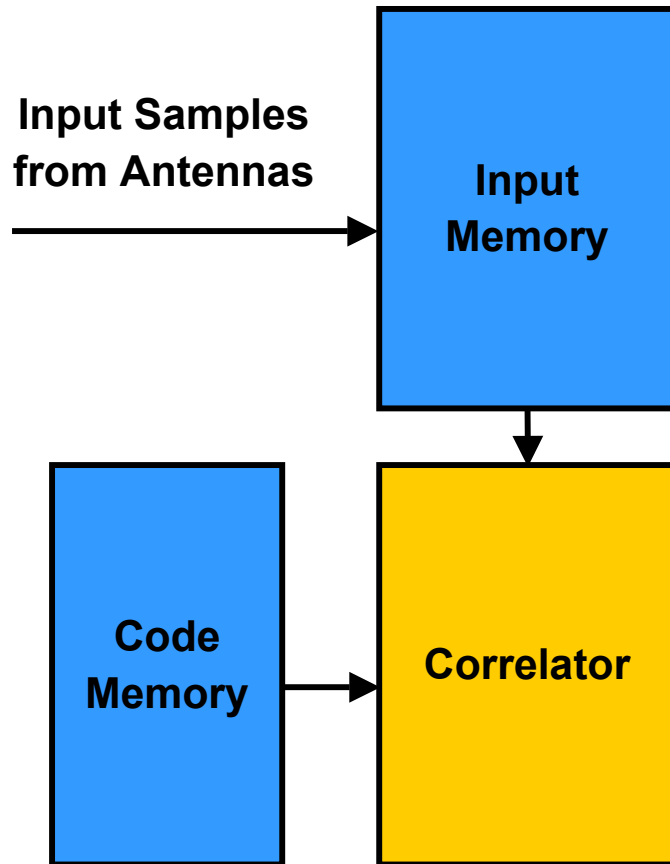
I^2+Q^2 – Calculate Power
(Magnitude) of
Correlation Results



Multipath Estimator

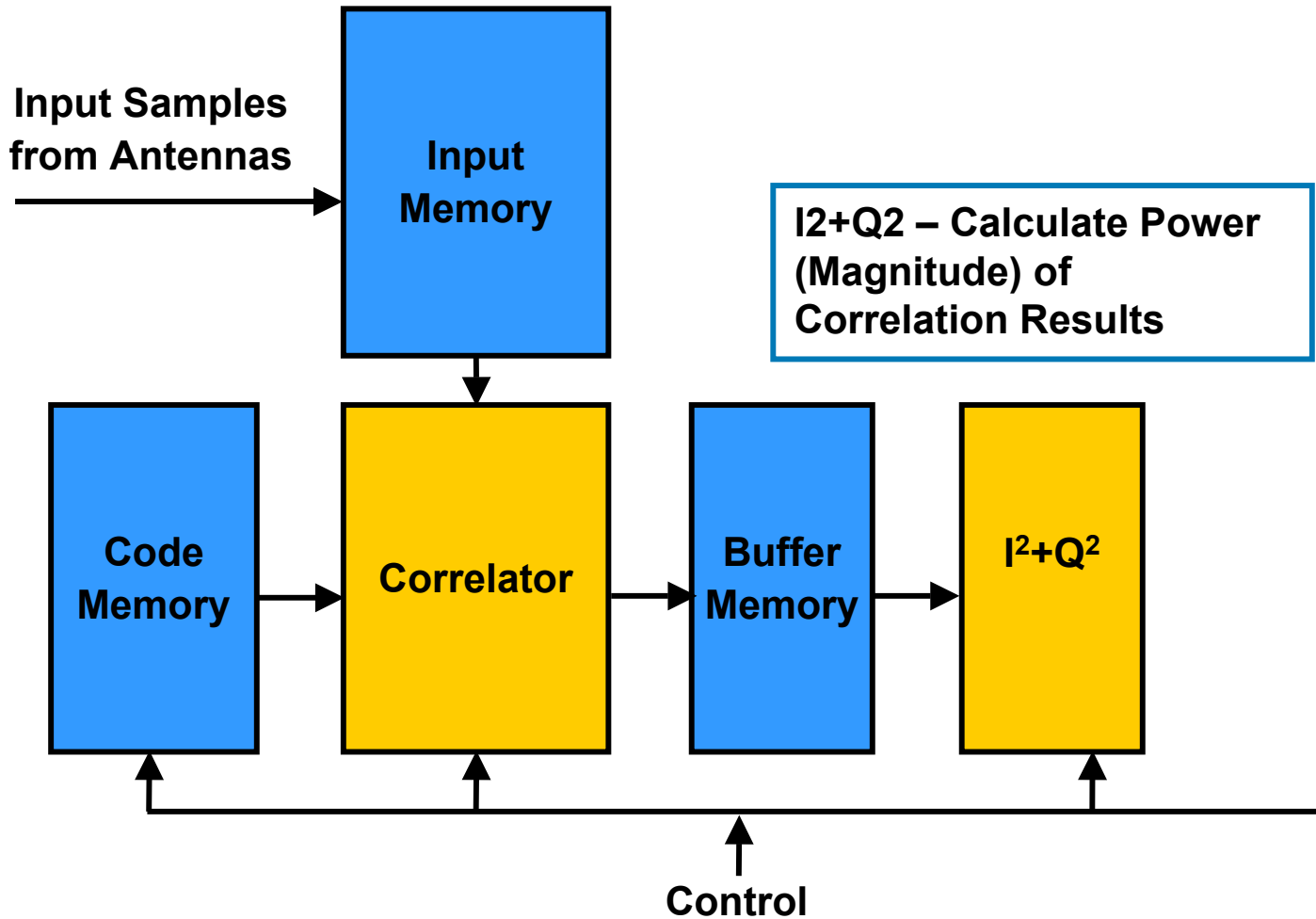


Multipath Estimator



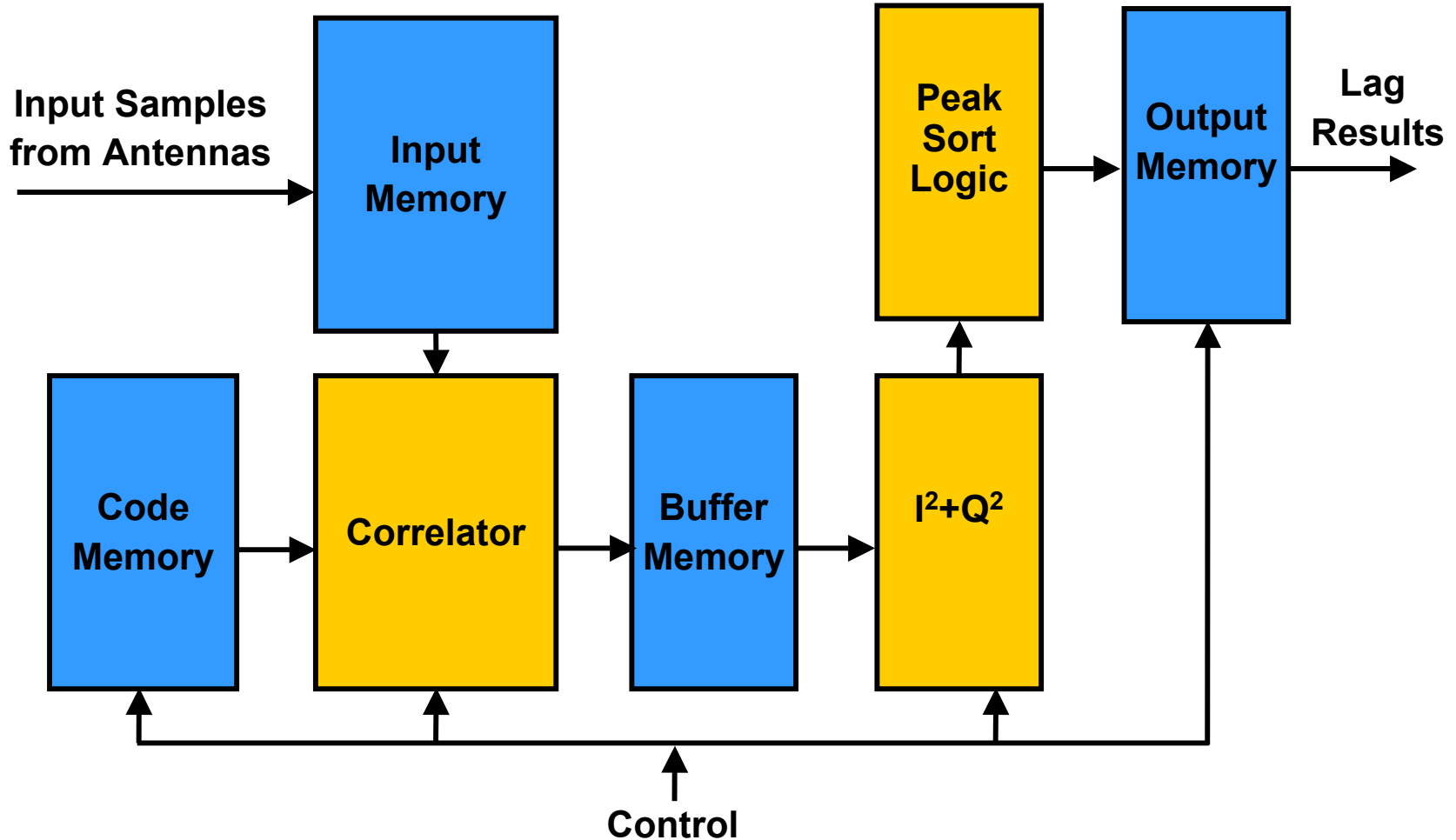
- **Correlator – Calculates Weighting Information for Receive Paths**
- **Information Is Used by Rake Fingers in Despreader**

Multipath Estimator



Multipath Estimator

Peak Sort Logic – Selects Strongest Weights from Correlator





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3G Chip-Rate Design Case Study in Stratix Devices

Case Study Assumptions

■ System Parameters

- 36 Users/Antenna
- ~2 Mbps/Antenna
- 8 Antennae
- Oversampling: 2
- Stratix PLD f_{MAX} : 138.24 MHz

■ Correlator-Based Functions Consume Most Resources

- Detailed Look at Following Functions
 - RACH Detection
 - Multipath Estimator

Key Stratix Features Used in BTS

**DSP
Blocks**

**M512
M4K
M-RAM**

PLLs



Correlator Architecture

- Distributed Arithmetic
 - Based on Shift Register
 - Most Popular Architecture for Initial 3G Designs
 - Two-Dimensional Correlator
 - Based on Block Memory
-
- Altera Has Done Extensive Research on Correlator Architecture
 - Two-Dimensional Correlator More Efficient for Typical BTS
 - Architecture Details & Comparisons
 - See Article Handout Available with Presentation
 - Altera Correlator IP Used in This Case Study
 - Based on Two-Dimensional Correlator Architecture



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Multipath Estimator

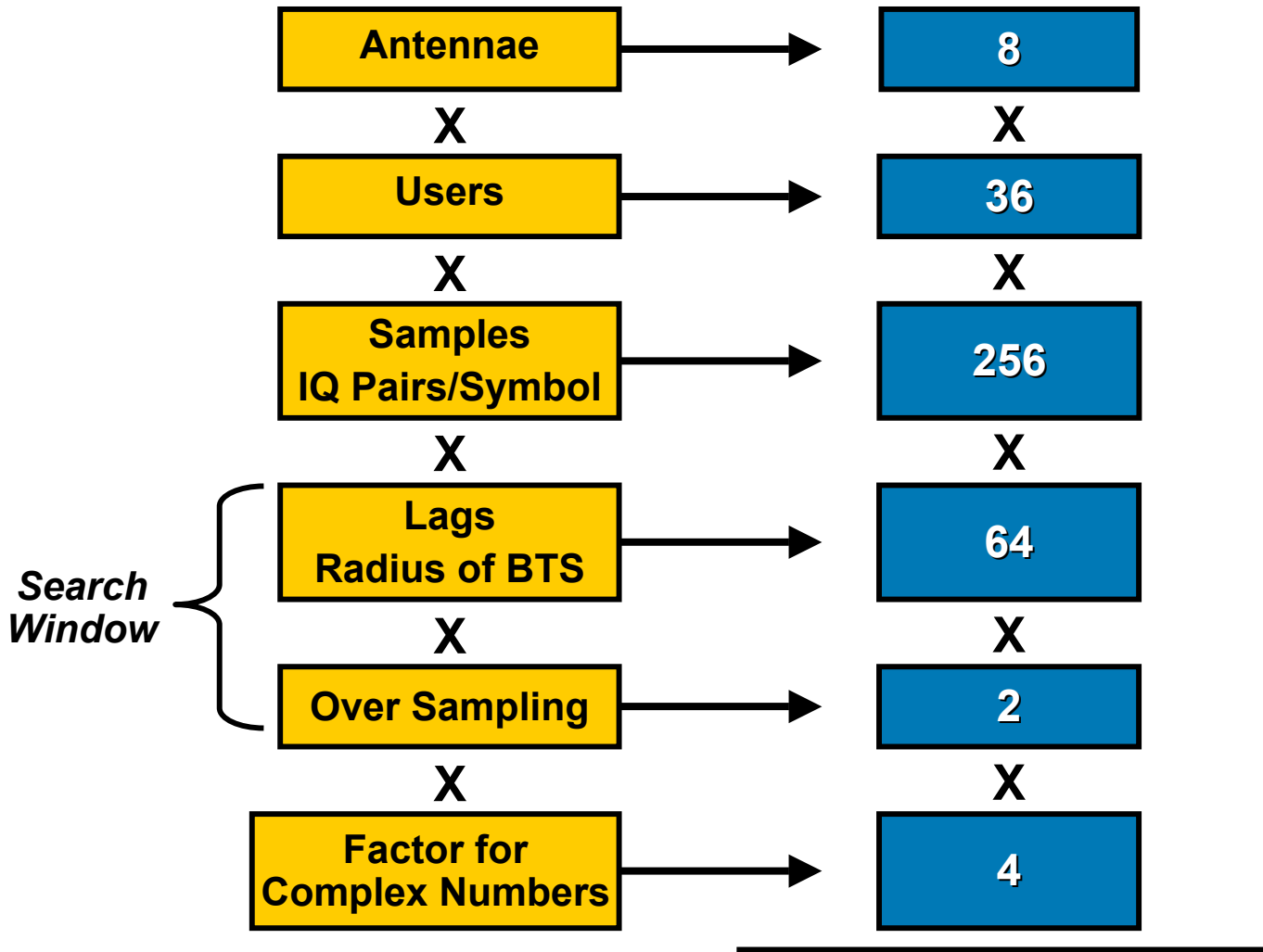
Correlator Calculations

Correlator IP Parameters

Stratix Block Diagram

Implementation

Serial Correlators Required



37,748,736

Calculating # of Correlators Required

Serial
Correlators

37,748,736

Time/Frame
Required by 3GPP

10 ms

X

/

Correlator Clock
Frequency

7.14 ns

Symbols in
3GPP Frame

150 (15*10)

Time to Calculate
Correlation per
Symbol

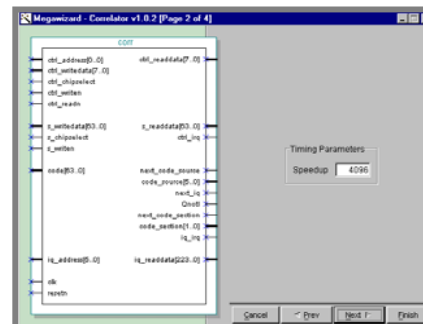
269.5 ms

Time Required
per Symbol
by 3GPP to Calculate
Correlation

0.667 ms

Parallel Correlators
Required
(Speed up Factor)

4,040
(Round to 2^n)



Multipath System Parameters

Megawizard - Correlator v1.0.2 [Page 1 of 4]

corr

- ctrl_address[0..0]
- ctrl_writedata[7..0]
- ctrl_chipselect
- ctrl_writen
- ctrl_readn
- s_writedata[63..0]
- s_chipselect
- s_writen
- code[63..0]
- iq_address[5..0]
- clk
- resetsn

ctrl_readdata[7..0]

s_readdata[63..0]

ctrl_irq

next_code_source

code_source[5..0]

next_iq

Qnotl

next_code_section

code_section[1..0]

iq_irq

iq_readdata[223..0]

System Parameters

Block Length	2048
Number Of Chips	256
OverSampling	2
Number Of Lags	128
Number Of Code Sources	40
Number Of Sample Sources	8

Cancel < Prev Next > Finish

**Specified by
3GPP**

**Chips per
Symbol
(Fractional Chip
also Supported)
Over Sampling:
1, 2, 4, 8, 16**

**Function of Expected
Frame in Which
Symbols Arrive.
Depends on Distance &
Timing Offset between
TX & RX**

**Antennae:
1, 2, ... 64**

**Users:
1, 2, ... 64**

Multipath Implementation Parameters

The screenshot shows the Megawizard interface for a correlator block. On the left, a list of signals is shown with 'x' marks indicating connections. On the right, the 'Implementation Parameters' dialog is open, showing several numerical fields and a checkbox.

Parameter	Value
Number Of Bits	5
Number Of Parallel Results	8
Input Buffer Multiplier	2
Output Buffer Multiplier	2

Quad Port

Cancel

**Bits per Symbol:
Typically 4 - 8**

**Parallel Outputs
1, 2, 4, 8, 16**

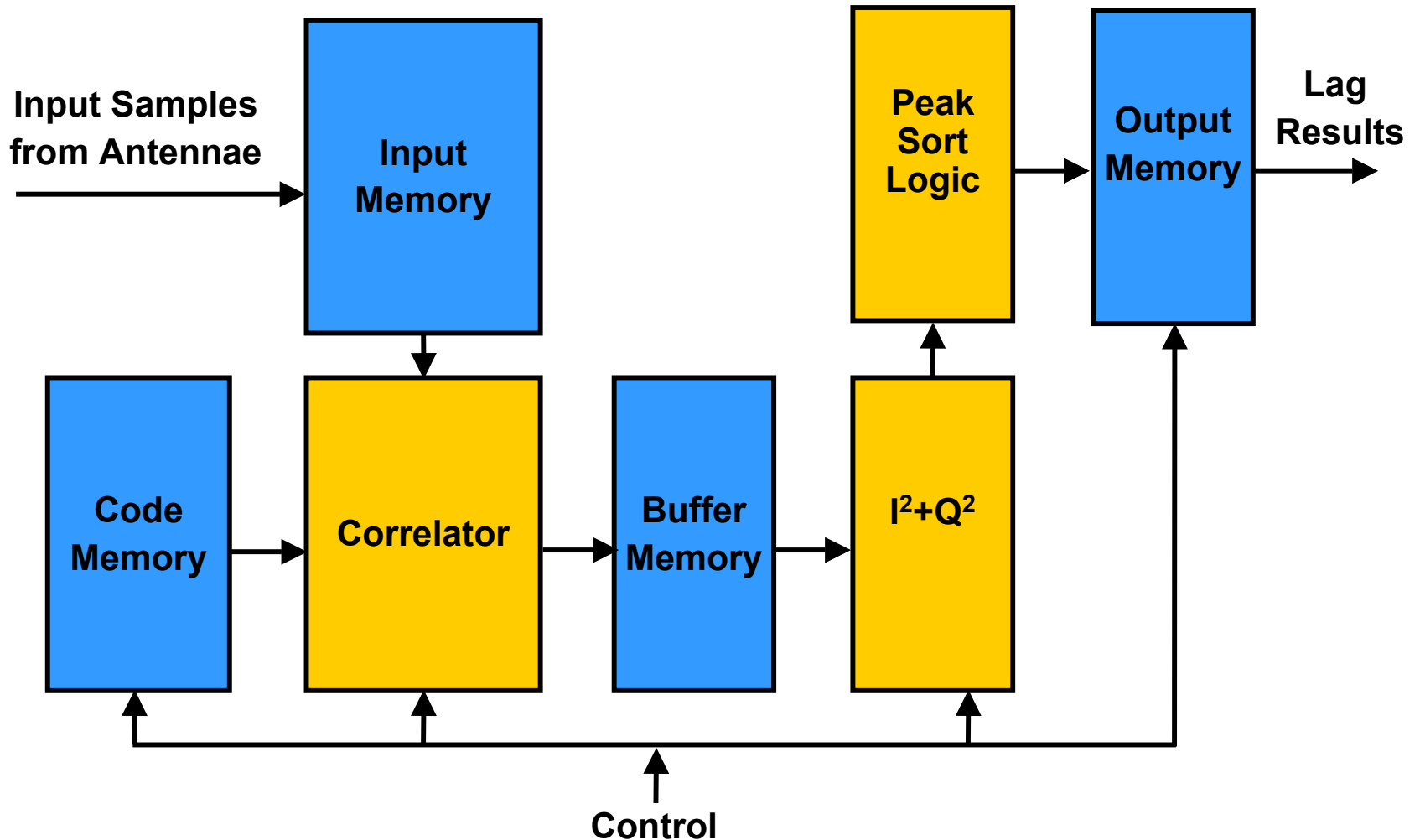
**Increase Input Storage:
Any Integer ≥ 2**

Allows for Increased Buffering of Input Data

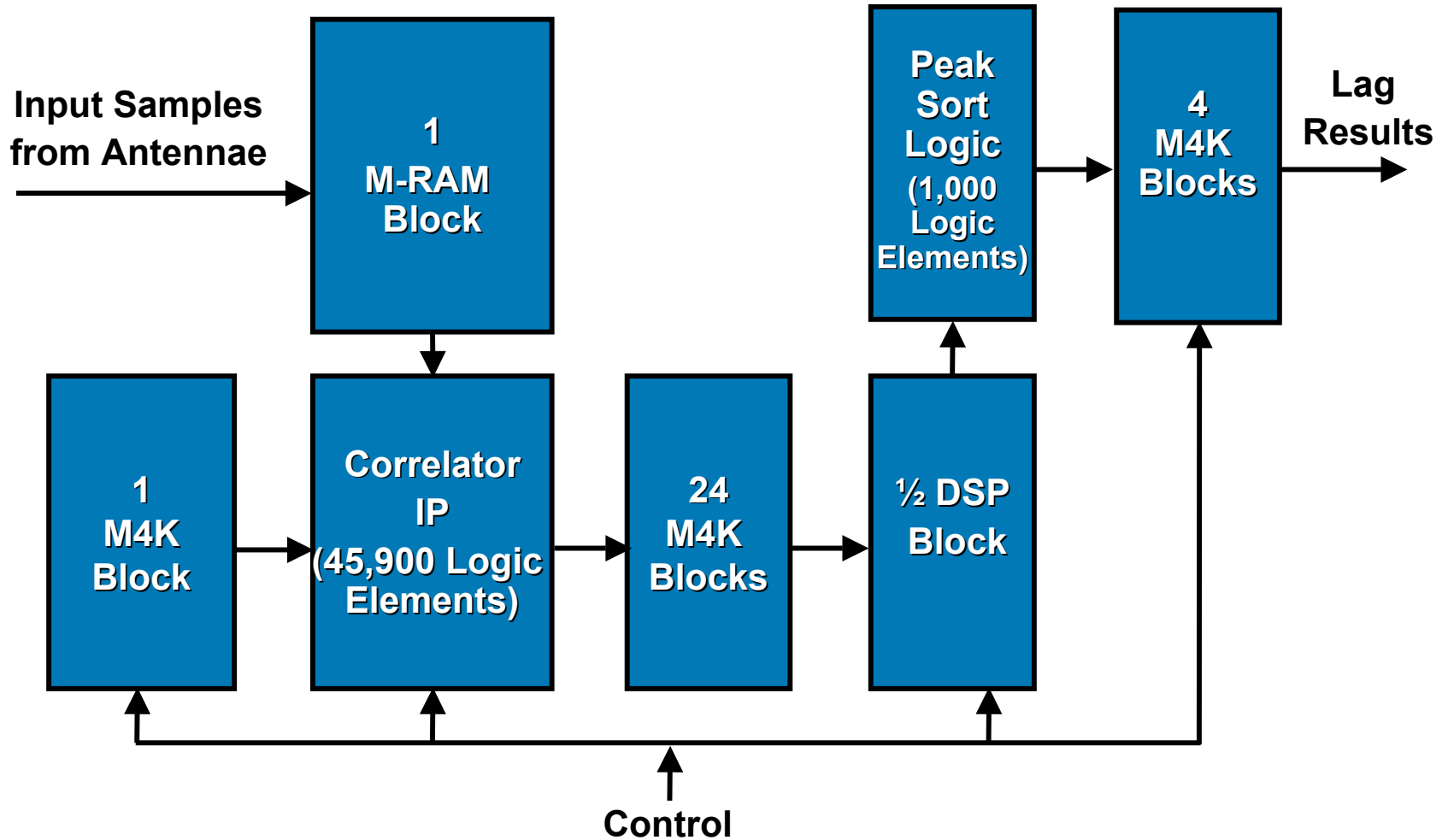
**Increase Output Storage:
Any Integer ≥ 2**

Allows for Slower Readout Since Results are Automatically Written.

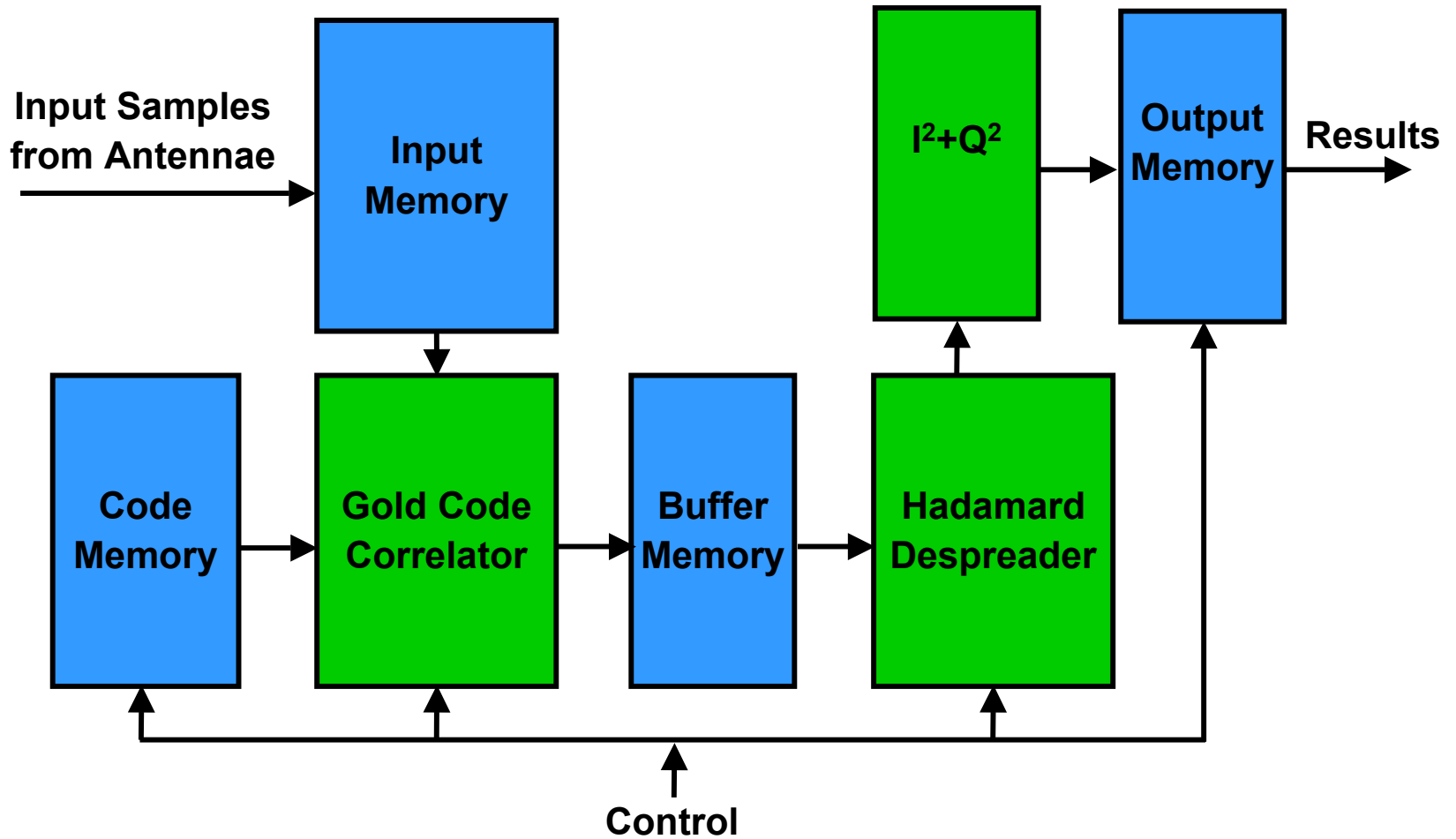
Multipath Estimator



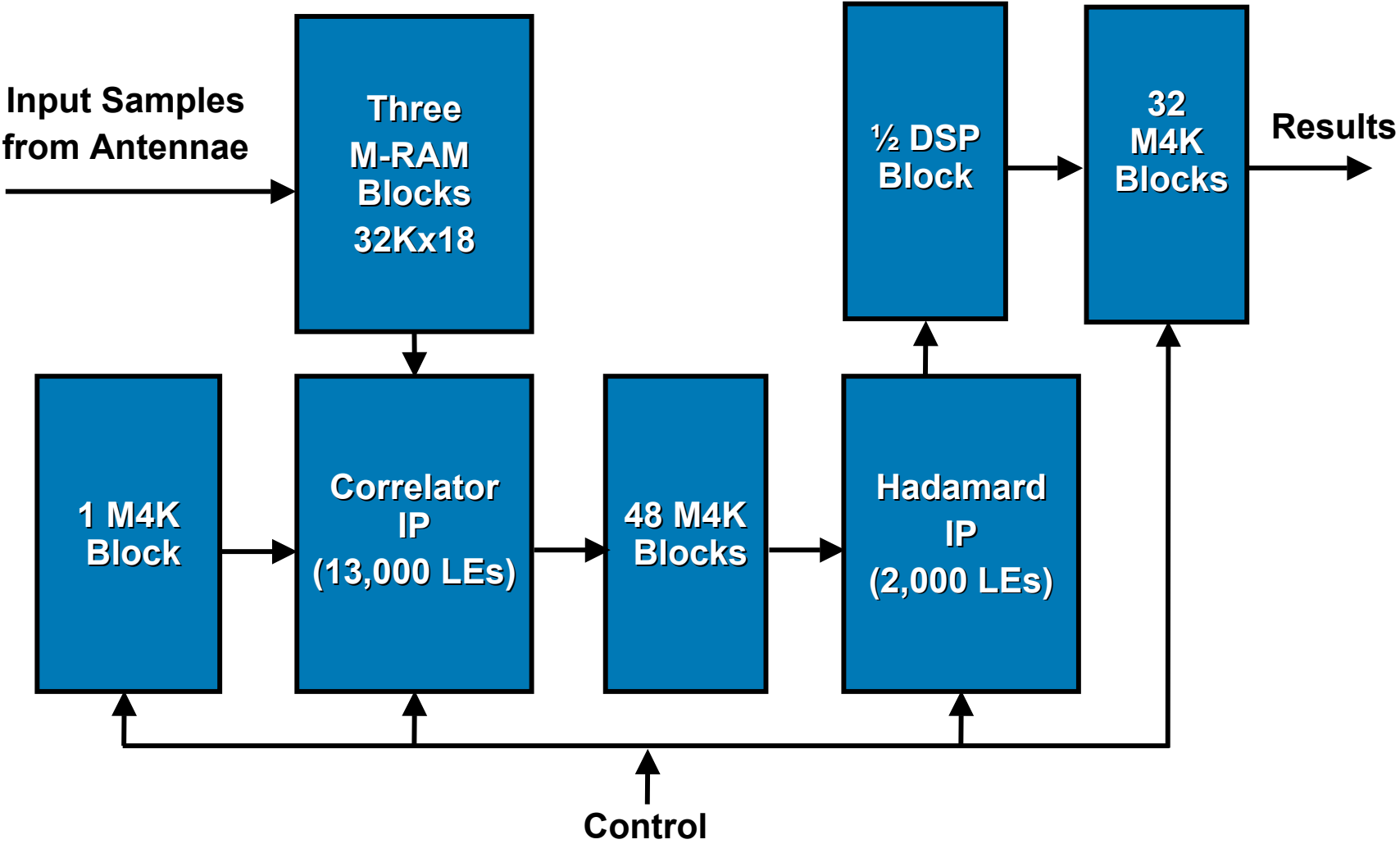
Multipath Estimator



RACH Detector



RACH Detector



Chip-Rate Resources Required

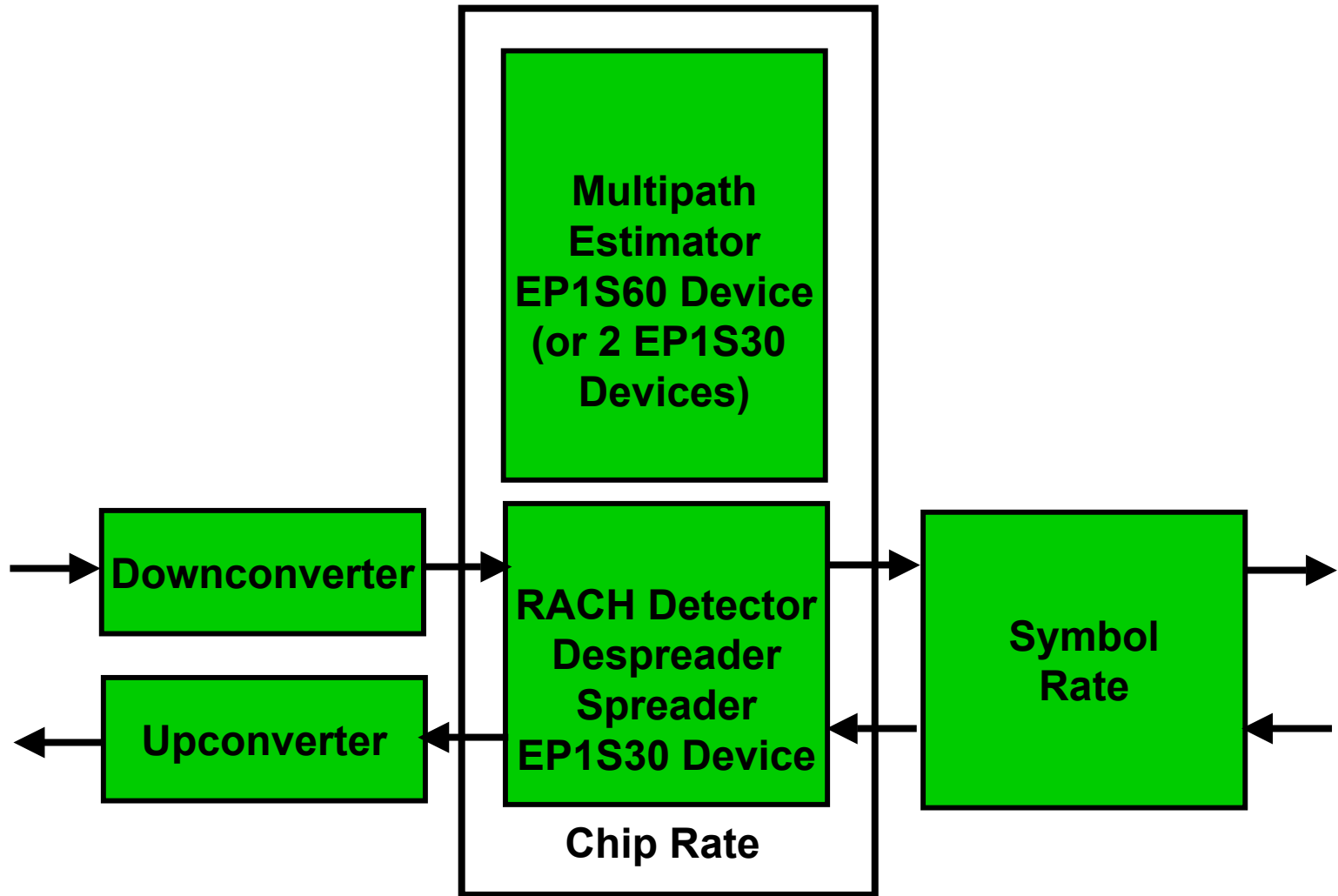
Function	LEs	DSP Blocks	Memory Bits
RACH Detector	15,700	.5*	1,634,000
Multipath Estimator	49,800	.5*	305,000
Despreader	1,800	-	168,000
Spreader	2,600	-	144,000

*DSP Blocks Can be Used for Correlator Function

Stratix Performance Impact

- Achieved 138.24 MHz with Multipath Estimator
 - Significantly above 122.88 MHz Requirement
- 138.24 MHz is 35% Improvement over APEX™ II
 - Fixed Number of Users
 - 35% Smaller Multipath Estimator
- Another Way to Look at Performance Impact
 - 35% Increase in Performance Leads to 35% More Users for Fixed Resource (i.e., 1S30)

3GPP Case Study



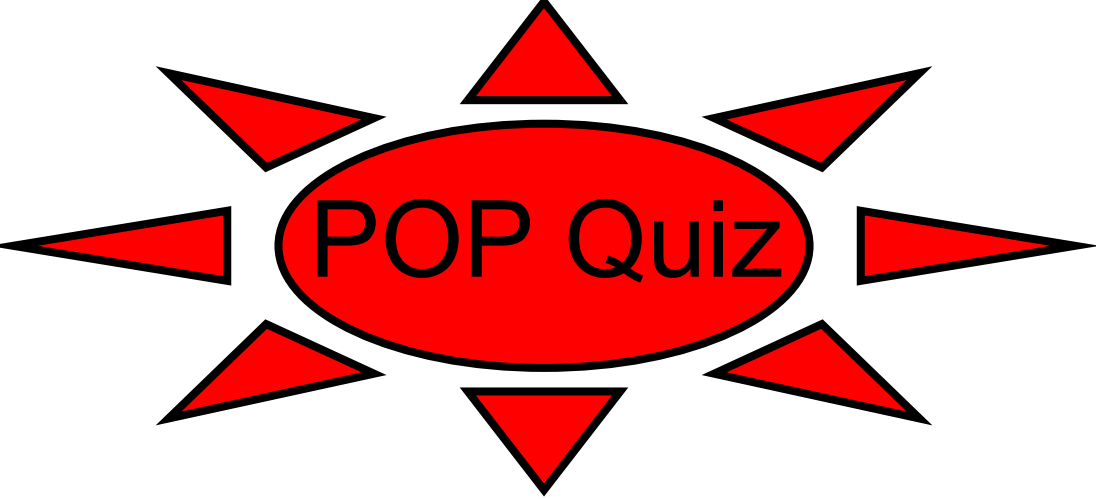
Related Stratix Reference Designs

- Direct Sequence Spread-Spectrum Reference Design
 - Targeted UMTS Specifications
 - 1 Antenna, 4 Users
 - Digital Downconverted/Upconverter
 - Chip-Rate Processing
- Multi-Channel Digital Downconverter Reference Design
 - Targeted UMTS Specifications
- QPSK Single-Channel Modern Reference Design
 - DSP Builder
 - Reed Solomon, Viterbi FEC

Chip Rate Processing Conclusion

■ Stratix Devices Meet Objectives

- \geq 122.88-MHz Performance (138.24 MHz)
- \geq 32 Users/Board (36)
- Low Cost per User in Stratix (3 1S30 Devices)
- HardCopy™ Devices Offer Further Cost Reduction
 - No Additional Development Engineering Involvement



Which is not included in Stratix Device?

1. DSP Block
2. MegaRAM
3. PLL
4. ADC