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Interfacing FPGAs with High Speed Memory Devices

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Agenda

- Memory Requirements
  - Memory System Bandwidth
  - Do I Need External Memory?
  - Altera® External Memory Interface Support
  - Memory Interface Challenges
- Memory Interface Solutions
  - DRAM
    - Single Data Rate (SDR), Double Data Rate (DDR), DDRII
    - FCRAM, RLDRAM
  - SRAM
    - Quad Data Rate (QDR)/QDRII SRAM
    - Zero Bus Turnaround (ZBT)/NoBL SRAM
- Signal Timing & Board Design

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Memory Requirements

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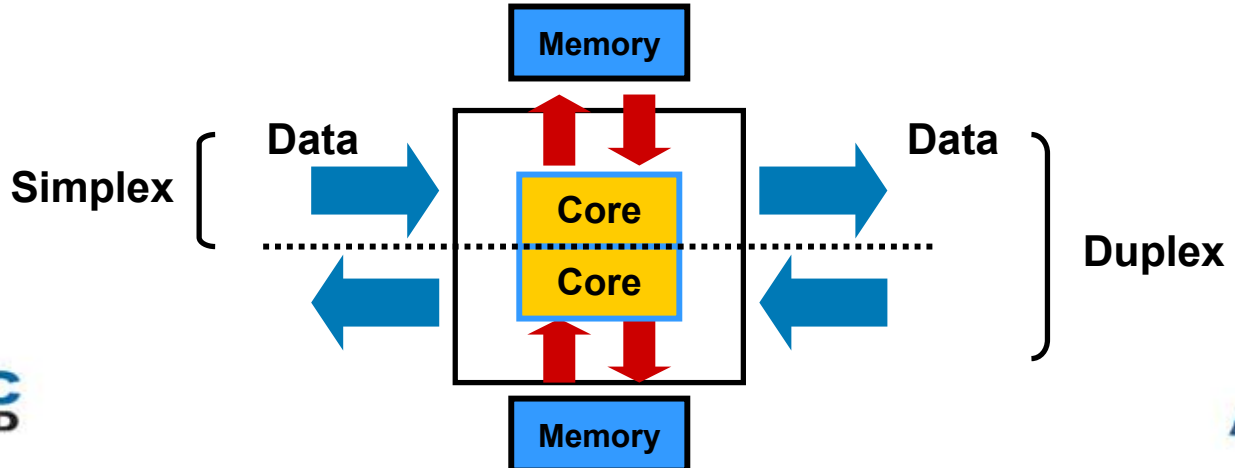
Memory System Bandwidth

Data Flow	Applications	Link Rate (Gbps)	Total Read/Write Memory Bandwidth (Gbps)	Memory Access Overhead 40% (Gbps)	Memory Banks Required		
					DDR 400 SDRAM x72	DDR 533 SDRAM x72	DDR 533 SDRAM x72
Simplex	1G Ethernet	1.25	2.5	3.5	1	1	1
	10G Ethernet	10	20	2.8	2	1	1
	40G Ethernet	40	80	112	2	1	1
Duplex	1G Ethernet	1.25	5	7	1	1	1
	10G Ethernet	10	40	56	3	2	2
	40G Ethernet	40	160	224	9	7	7



Do I Need External Memory?

- Most FPGA Architectures Now Include On-Chip Blocks of SRAM
  - Fine-Grain (< 1Kb) & Coarse-Grain (> 500Kb)
  - Densities up to 10Mb
- 300+ MHz Performance without Off-Chip Latency
- Flexible Depth, Width, & Number
- Abundant Routing between Logic & Memory
  - No off-Chip I/O Placement or Routing Issues

Altera FPGA	Max. Memory Bits
Stratix™	10,118,016
Stratix GX	3,423,744
Cyclone™	294,912

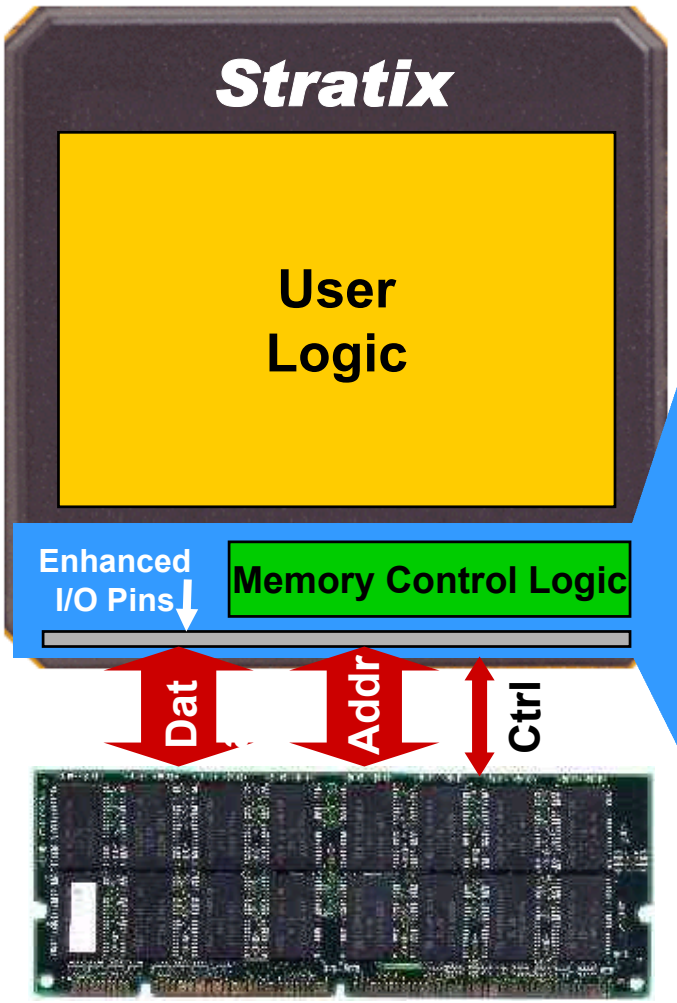
FPGAs & External Memory

- Interface to External Memory When Internal FPGA Memory Capacity is Insufficient
- FPGA Includes Enhanced I/O Circuitry to Maximize Data Access Performance
- Off-the-Shelf, Customizable Controllers Minimize Development Time

Memory Technology	Clock Speed in FPGA	I/O Type
SDR SDRAM *(1)*	167 MHz	LVTTL (3.3V)
DDR SDRAM	167 MHz	SSTL-2 (2.5V)
DDR Fast Cycle RAM (FCRAM)	200 MHz	SSTL-2 (2.5V)
Reduced Latency DRAM (RLDRAM)	200 MHz	HSTL (1.8V/1.5V)
QDR SRAM *(2)*	167 MHz	HSTL (1.5V)
QDRII SRAM	167 MHz	HSTL (1.5V)
ZBT (NoBL) SRAM (3)	200 MHz	LVTTL (3.3V)

(1) Synchronous Dynamic Random Access Memory
(2) Static Random Access Memory
(3) Zero Bus Turnaround; No Bus Latency

Altera Memory Controller IP



- Altera Memory Controller MegaCore® Functions
  - Low-Cost, Drop-In Blocks of IP
  - Hardware-Tested on Internal Test Platform
  - Fully Supported
- Altera Megafunction Partner Program (AMPP℠) Functions
  - Fully Customizable through Design Services
- Altera® Memory Controller Design Examples
  - Free, Open Source

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Memory Interface Solutions

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SDRAM Overview

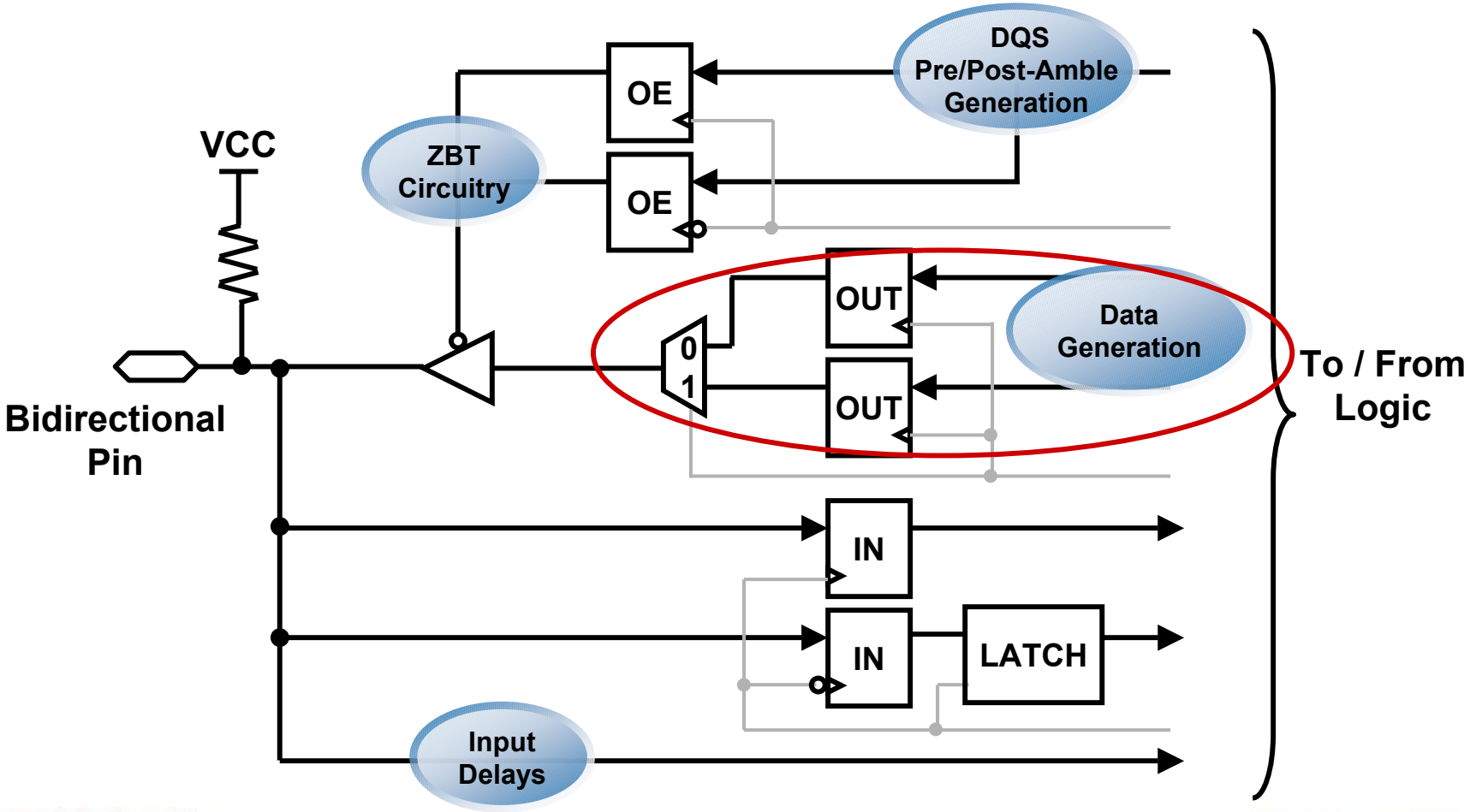
Feature	Description
Type	■ SDR & DDR/DDRII SDRAM (Commodity) ■ FCRAM & RLDRAM (Low-Latency)
Clocking	■ All (Except SDR SDRAM) Require Clocking on Both Edges of Differential Clock
Refresh	■ Requires Periodic Refresh Command to Maintain Contents
Bank Management	■ Memory Is Divided Into Multiple Banks that Require Manual Opening & Closing
Initialization	■ Initialization Command Sequence Required on Power-Up
Data Strobe (DQS) Signal	■ All (Except SDR SDRAM) Use a DQS Signal to Sample Set of Data Signals ■ DDR SDRAM & FCRAM Use Bi-Directional DQS; RLDRAM Uses DQS for Reads Only ■ RLDRAM Uses Differential DQS

SDRAM Interfacing Requirements

Issue	FPGA Solution
High-Speed Operation (133/167/200+ MHz)	■ Current Generation FPGA Supports 167+ MHz Core & I/O Speeds ■ Next Generation Supports 250+ MHz
DDR Data Generation	■ Dedicated DDR Registers in I/O Element (IOE) Eliminate Need for Clock Doubling of High-Speed Internal Clocks
Data Strobe (DQS) Signal Alignment	■ Dedicated Strobe Signal Circuitry for Precise Alignment ■ Phase Shifting Supports Data Window of Both DDR SDRAM & FCRAM
Differential DQS Signals (RLDRAM)	■ Use Dedicated I/O Circuitry for DQS & Tie DQSn to VREF through Resistor ■ Can Also Use Standard I/O Signals, Which Support Differential HSTL I/O & Delay Signal on Board

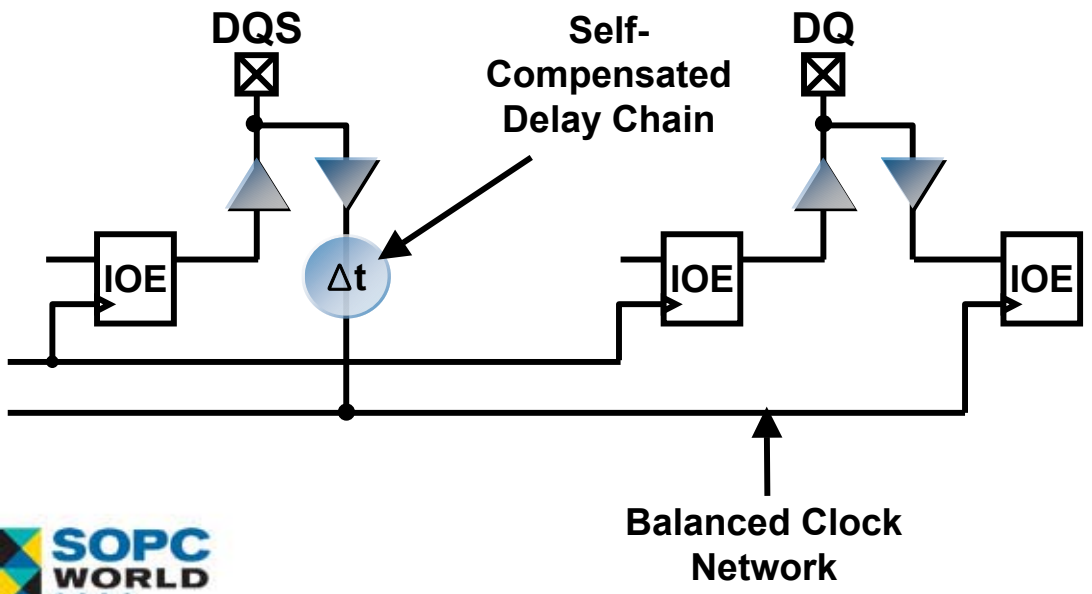
DDR Support in I/O Element

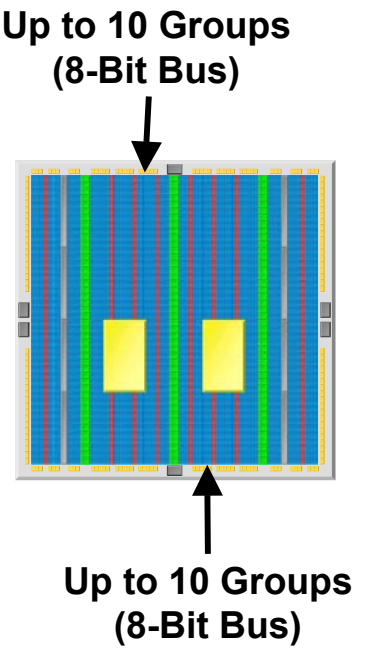
- DDR Data Generation without Doubled Clock



Enhanced Data & Data Strobe Signal Interaction

- Optimized Data Strobe (DQS) Pins
  - Self-Compensated Delay Chain Generates Shift on Data Read
  - 90 Degrees for DDR SDRAM, 72 Degrees for FCRAM
- Drive Associated Data (DQ) Pins
  - Uses Balanced, Local Clock Network





SDRAM Requirements (Cont.)

Issue	FPGA Solution
Refresh, Initialization & Bank Management	■ Complex State Machine Logic Handled by Drop-In IP Cores with SRAM-like Local Interfaces
I/O Standards	■ Multiple I/O Standards Supported by I/O Elements ■ Selectable by I/O Bank
Difficulty of Board Design	■ Board Design Guidelines Based on Hardware Proven Solutions ■ On-Chip Termination in FPGA Removes Need for Many External Resistors

SDRAM Interfaces in Altera FPGAs

Interfaces	Stratix	Stratix GX	Cyclone
f_{MAX} for SDRAM I/F	167 MHz (200 MHz in –5)	167 MHz (200 MHz in –5)	133 MHz
Dedicated DDR Registers	Yes	Yes	No
Dedicated Strobe Signal Circuitry	Yes (Up to 160 Data Signals)	Yes (Up to 160 Data Signals)	Yes (Up to 40 Data Signals)
On-Chip Termination	Yes	Yes	No

SDRAM Controller IP

Memory	Device Support	Type	Availability
SDR SDRAM	Stratix, Stratix GX, Cyclone	Free Design Example	Now
DDR SDRAM	Stratix, Stratix GX, Cyclone	MegaCore® & AMPP℠ IP	Now
DDRII	Next Generation	MegaCore IP	2003
FCRAM (DDR)	Stratix, Stratix GX	MegaCore & AMPP IP	Now
RLDRAM	Stratix, Stratix GX	MegaCore	Q1 2003

High-Performance SRAM Overview

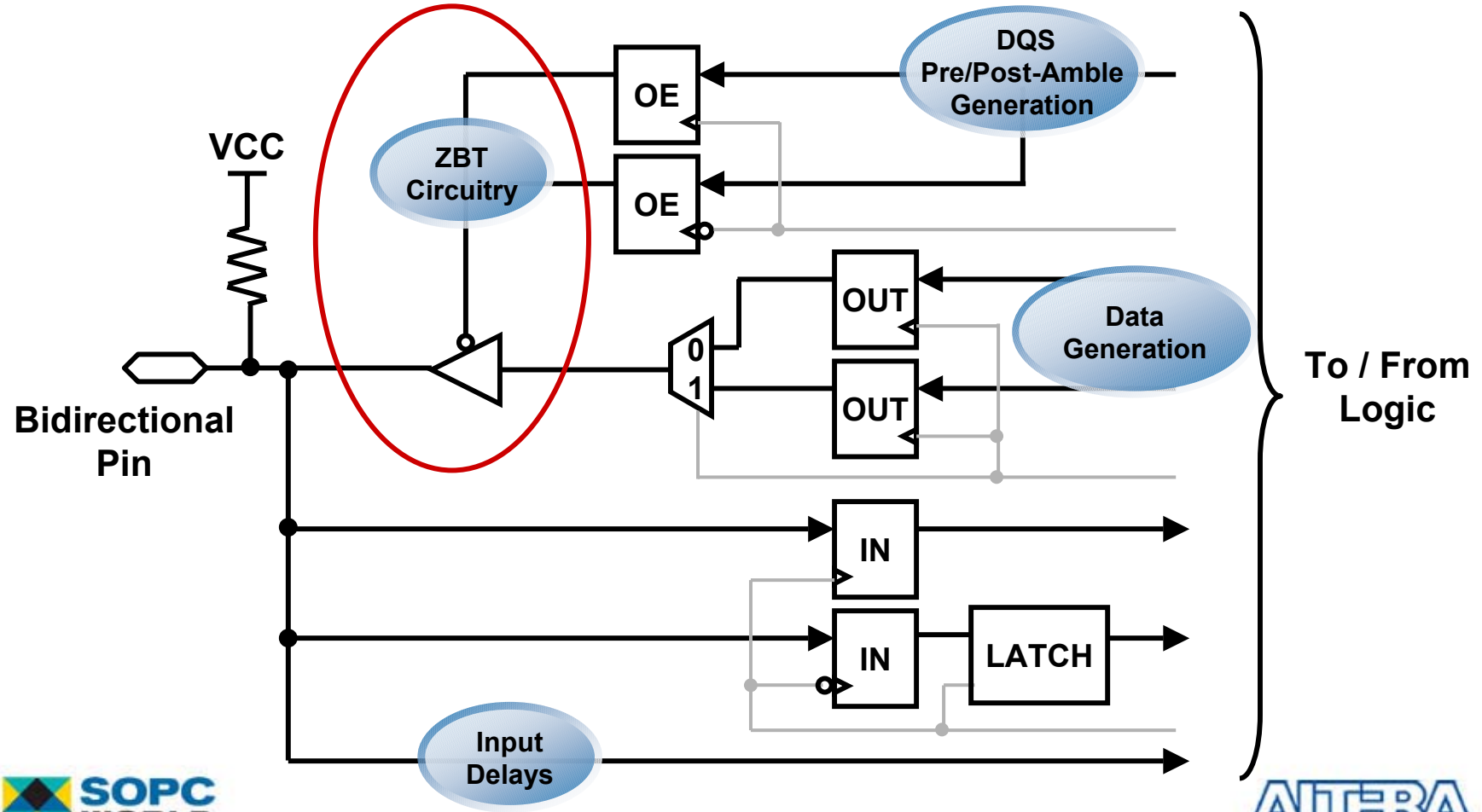
Feature	Description
Type	■ ZBT/NoBL for Higher Utilization of Shared Data Bus ■ QDR/QDRII for High-Performance DDR Access on Dedicated Read & Write Data Buses
Clocking	■ Single-Edge for ZBT, Both Edges for QDR/QDRII
Control Logic	■ Much Simpler than SDRAM

SRAM Interfacing Requirements

Issue	FPGA Solution
High-Speed Operation (200 MHz)	■ Current Generation FPGA Supports 200 MHz I/O and HSTL Signaling ■ Next Generation Supports 300+ MHz
DDR Data Generation (QDR/QDRII)	■ Dedicated DDR Registers in I/O Element Allows DDR Transfers without Requiring Clock Doubling
Bus Contention (ZBT/NoBL)	■ Dedicated ZBT Circuitry for Increasing t_{ZX} to Avoid Contention on Read-to-Write Transition
Tight t_{CO} & t_{SU} Specifications	■ Internal Phase-Locked Loops (PLLs) Enable Fast t_{CO} & t_{SU} Clock Shifting Feature Permits Accurate Data Capture on Reads
Clock Generation	■ PLL Generates Differential HSTL Clock for Memory Device

ZBT Support in I/O Element

- Increase t_{ZX} to Avoid Bus Contention



SRAM Interfaces in Altera FPGAs

Interface	Stratix	Stratix GX
f_{MAX} for SRAM Interface	200 MHz	200 MHz
Dedicated DDR Registers	Yes	Yes
Dedicated ZBT Circuitry	Yes	Yes
HSTL I/O Support (Class I & II)	Yes	Yes
PLLs (for Clock Management & Generation)	6-12	4-8

SRAM Controller IP

Memory	Device Support	Type	Availability
QDR	Stratix, Stratix GX	Free Design Example	Now
QDRII	Stratix, Stratix GX	Free Design Example	Now
ZBT/NoBL	Stratix, Stratix GX	Free Design Example	Now

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Signal Timing & Board Design

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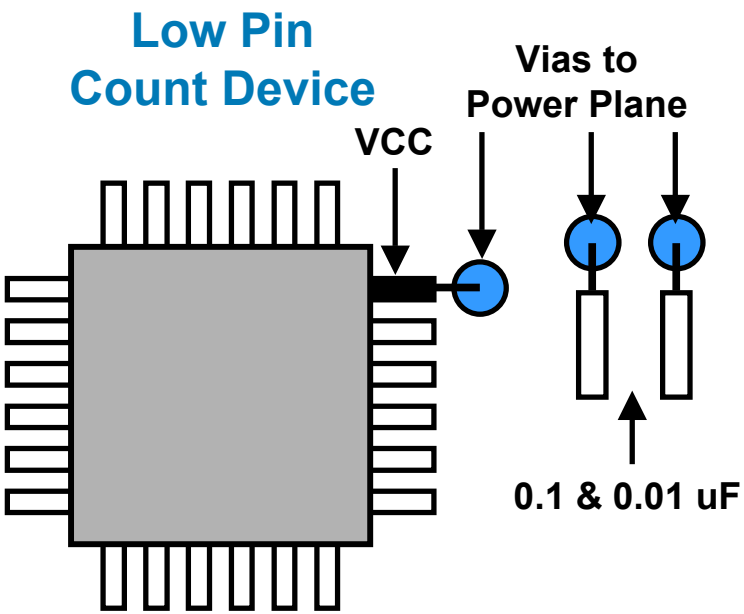
Board Timing Issues

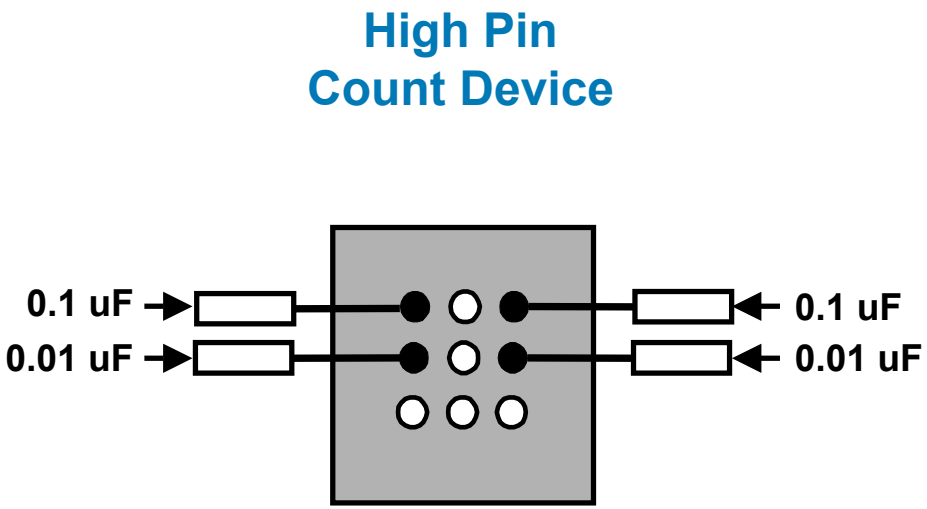
Issue	FPGA Resolution
Clock Generation	Use FPGA PLLs to Generate & Distribute Clocks for Greater Control & Simplified Routing
Clock Skew	Use External Feedback Mode of PLLs to Synchronize Source & Destination Clocks
t_{CO}, t_{SU}, t_H Violations	Use PLLs to Shift Clock Edges inside FPGA
t_{ZX}, t_{XZ} Violations (Bus Contention)	Use Dedicated ZBT Circuitry to Delay t_{ZX} of FPGA
DQS Signal Alignment	Match DQS & DQ Trace Lengths, Then Use Dedicated DQS Delay Circuitry to Provide Appropriate DQS Phase Shift

Altera® Always Recommends Performing Board Timing Analysis for High-Speed Memory Interface Designs

Decoupling Guidelines

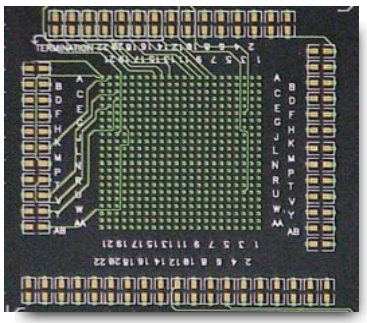
- Improve Signal Integrity through Decoupling Capacitors
- Recommend Using 0.1 & 0.01 µF Capacitors per Power Pin on Low Pin Count Devices
  - Faster Edge Rates (>100 MHz) May Require 0.001 µF As Well
- For High Pin Count Devices, Can Alternate between 0.1 µF & 0.01 µF on Adjacent Power Pins
  - Hardware Tested on Altera® Internal Memory Test Board
  - Larger Benefit than Placing Capacitors Farther from Pin



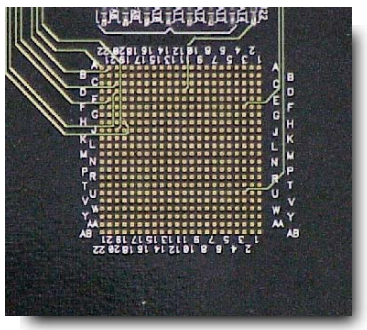


Other Board Design Guidelines

- Ensure FPGA I/O Meets JEDEC Spec of 1v/ns with Class 1 & Class 2 Loads for Optimal Signal Integrity
  - Altera FPGAs are Compliant
- Impedance & Termination
  - Match Lengths Where Possible
    - At a Minimum, Match Address/Control As One Group, Data As Another
  - Match I/O Termination with Trace Impedance
    - Follow Memory Vendor's Guidelines
    - Use On-Chip Termination (Terminator™ Technology)



External Termination



Terminator Technology

DIMM Design Guidelines

- Dual In-line Memory Modules (DIMMs) Available For:
  - SDR & DDR SDRAM
  - RLDRAM
- Ensure FPGA Can Drive Large Capacitive Loads
  - Altera FPGAs Can Drive Up to 25 pF
- Ensure FPGA Can Support 72-Bit Wide DDR I/O Per DIMM
  - Stratix & Stratix GX Devices Can Support Two 72-Bit DIMMs with Dedicated DDR Circuitry
  - Can Support Additional DIMMs, But May Require Lower Frequency or Careful Board Design

For More Information

- Visit http://www.altera.com
- Intellectual Property
  - OpenCore® Evaluation Downloads for All Memory Controller IP
  - Downloads for Memory Controller Free Design Examples
  - Detailed Test Board Documentation Available on Request
- Literature
  - AN 212: Implementing Double Data Rate I/O Signaling in Stratix Devices
  - AN 209: Using Terminator Technology in Stratix Devices
  - AN 256: Implementing Double Data Rate I/O Signaling in Cyclone Devices