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Technology Roadmap

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Agenda

- Investing in Our Future
- Advanced Process Technology
- Rising Costs of ASIC Development
- Core Technology Improvements
- Product Family Roadmaps
- Development Tools
- Programmable Systems

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Investing in Our Future

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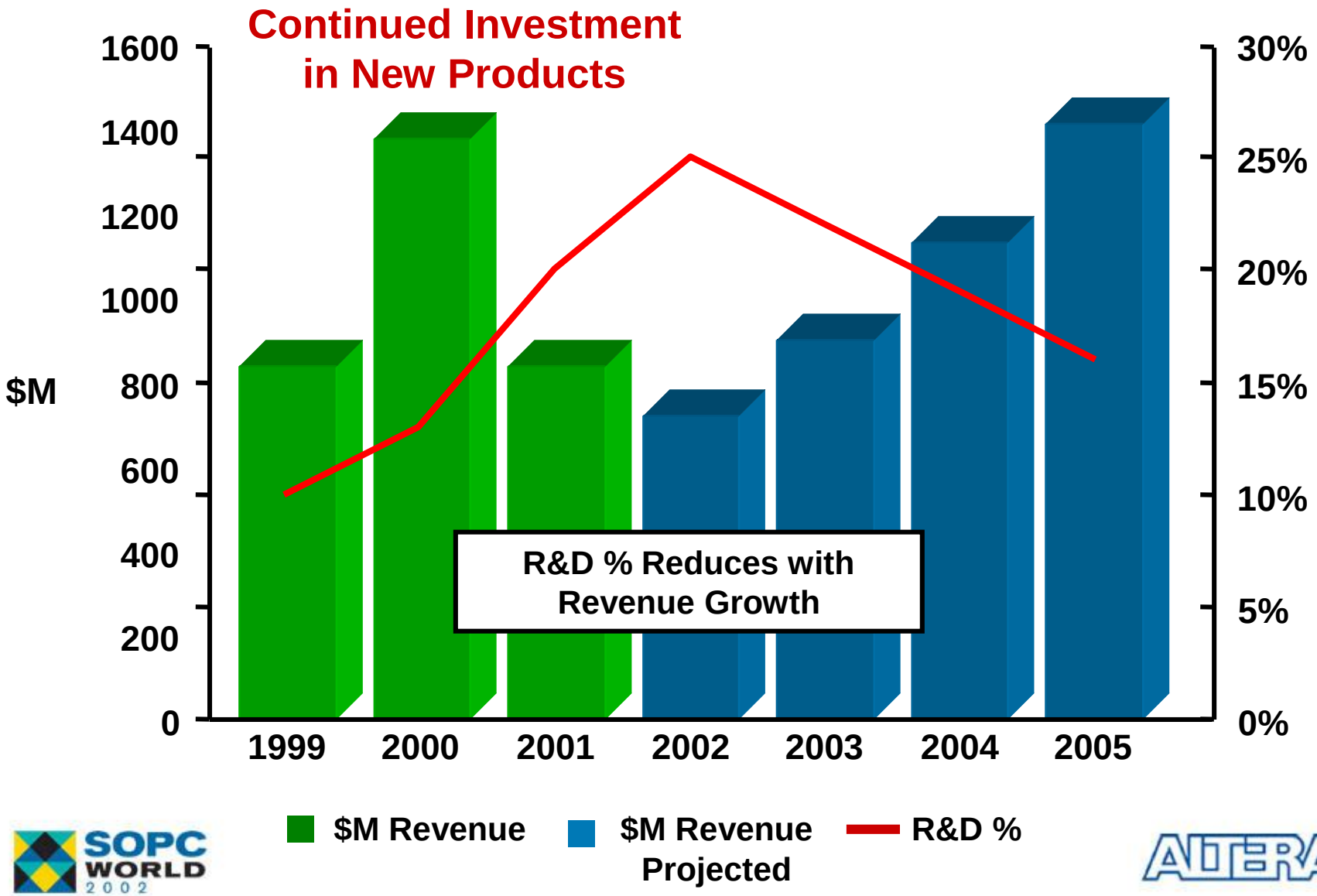
Revenue & R&D Investment



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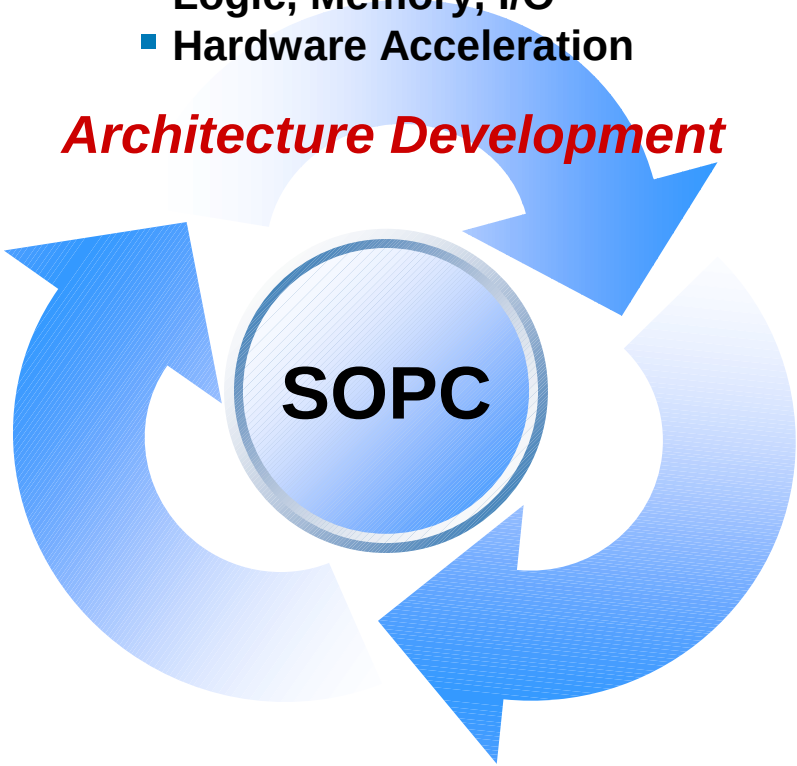
Product Development

- Process Technology
- Interconnect Structure
- Logic, Memory, I/O
- Hardware Acceleration

Architecture Development

Customer Feedback Requirements

- SOPC Value
- Features, Pricing
- Power, Packaging



IP Integration

- Hard vs. Soft Functions
- Cost, Performance, Power, Complexity
- Stability

Quartus Development Tools

- Design Methodology
- Synthesis, Simulation
- Verification, Debug

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Accelerated Architecture Development – 15 Months

October 2001

Project Concept

June 2002

Requirements Refined & Architecture Defined

Beta Software

December 2002

First Silicon

April 2002

Customer Requirements Defined

September 2002

Design & Layout Complete

Over 60% of Time Invested with Customers!

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Advanced Process Technology

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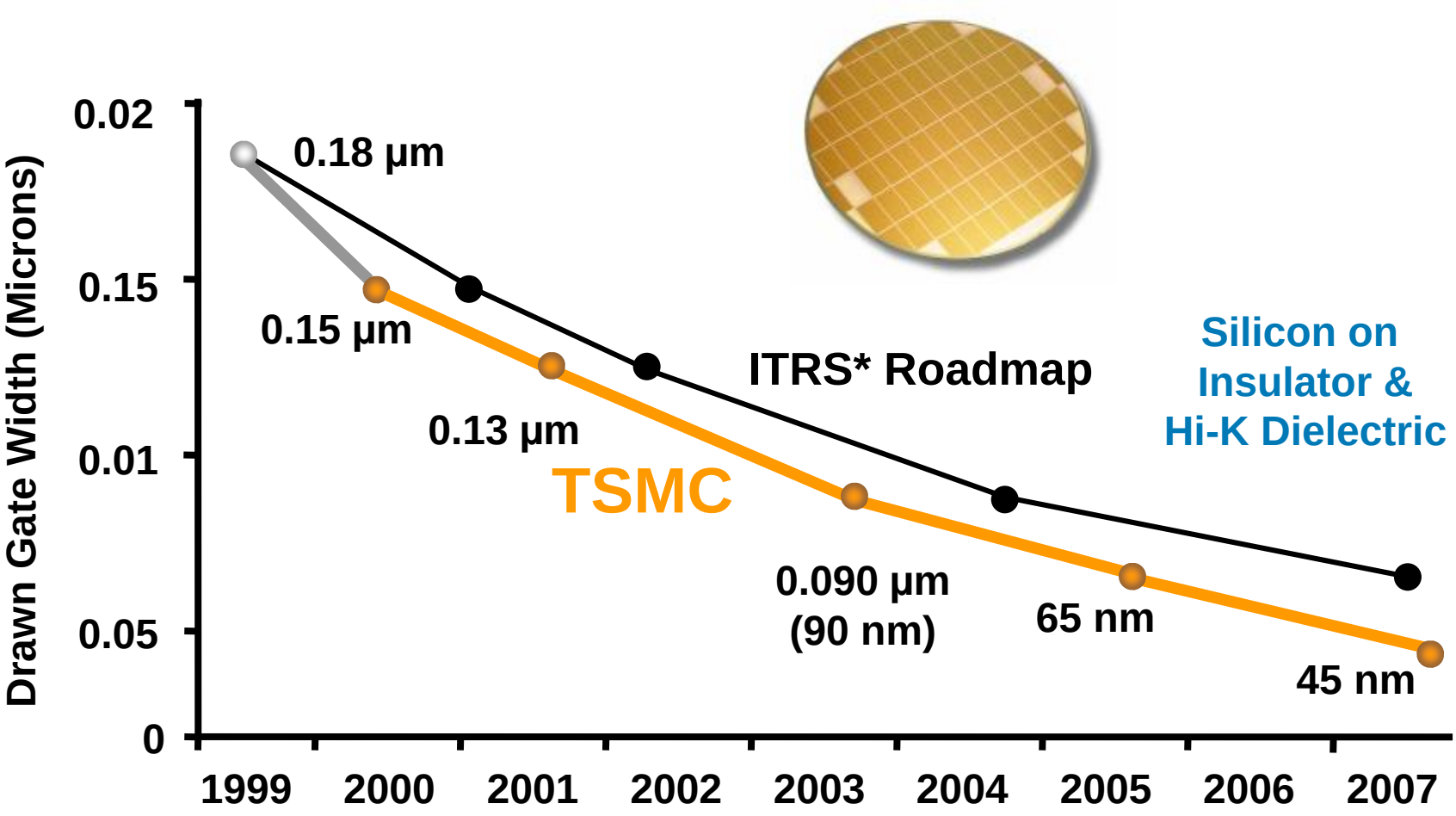
TSMC Roadmap Outpacing ITRS



Source: *International Technology Roadmap for Semiconductors 2001 TSMC 2002 Technology Seminar

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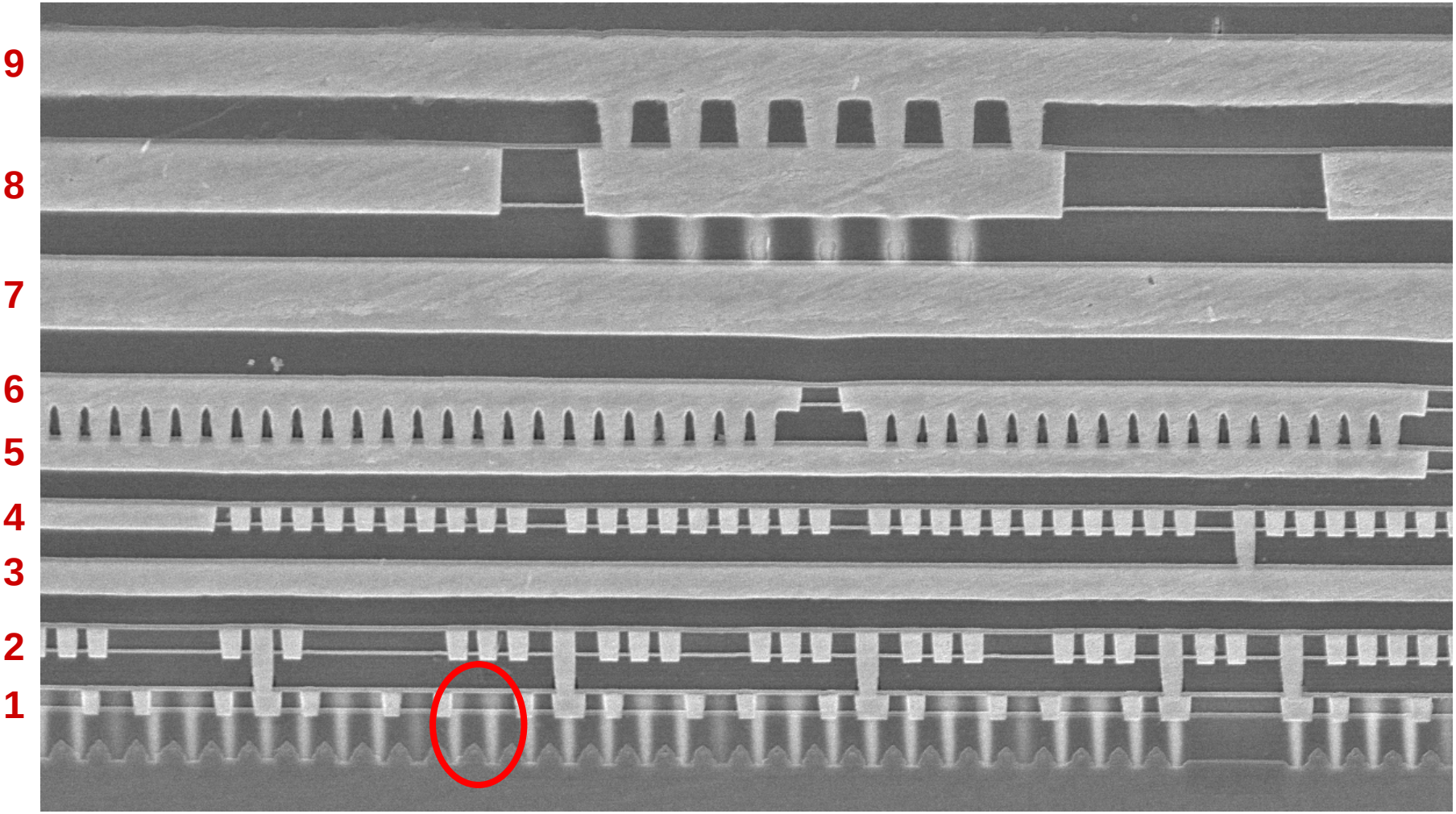
0.13µm Status

- Process
  - 9 Layers of Metal
  - Copper / FSG
  - High Performance Device
  - Lithography: 248nm / 193nm
- Altera Ramp Up
  - 9 Months Production APEX II
  - Stratix: 4 Products Already Shipped 1S80 ~ 230 Million Transistors

Stratix 9-Layer Copper Interconnect



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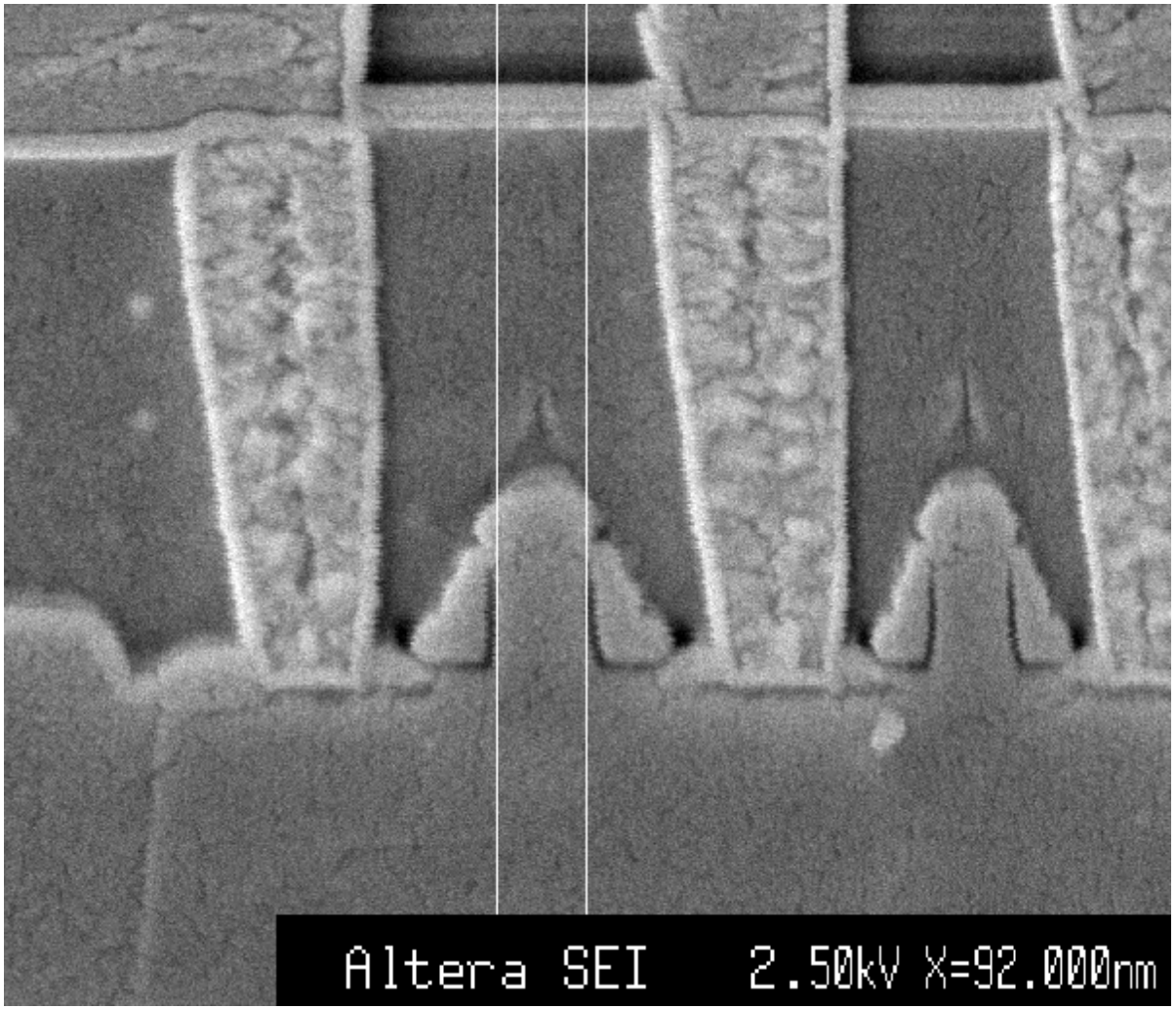
Stratix Transistor Leff 90nm



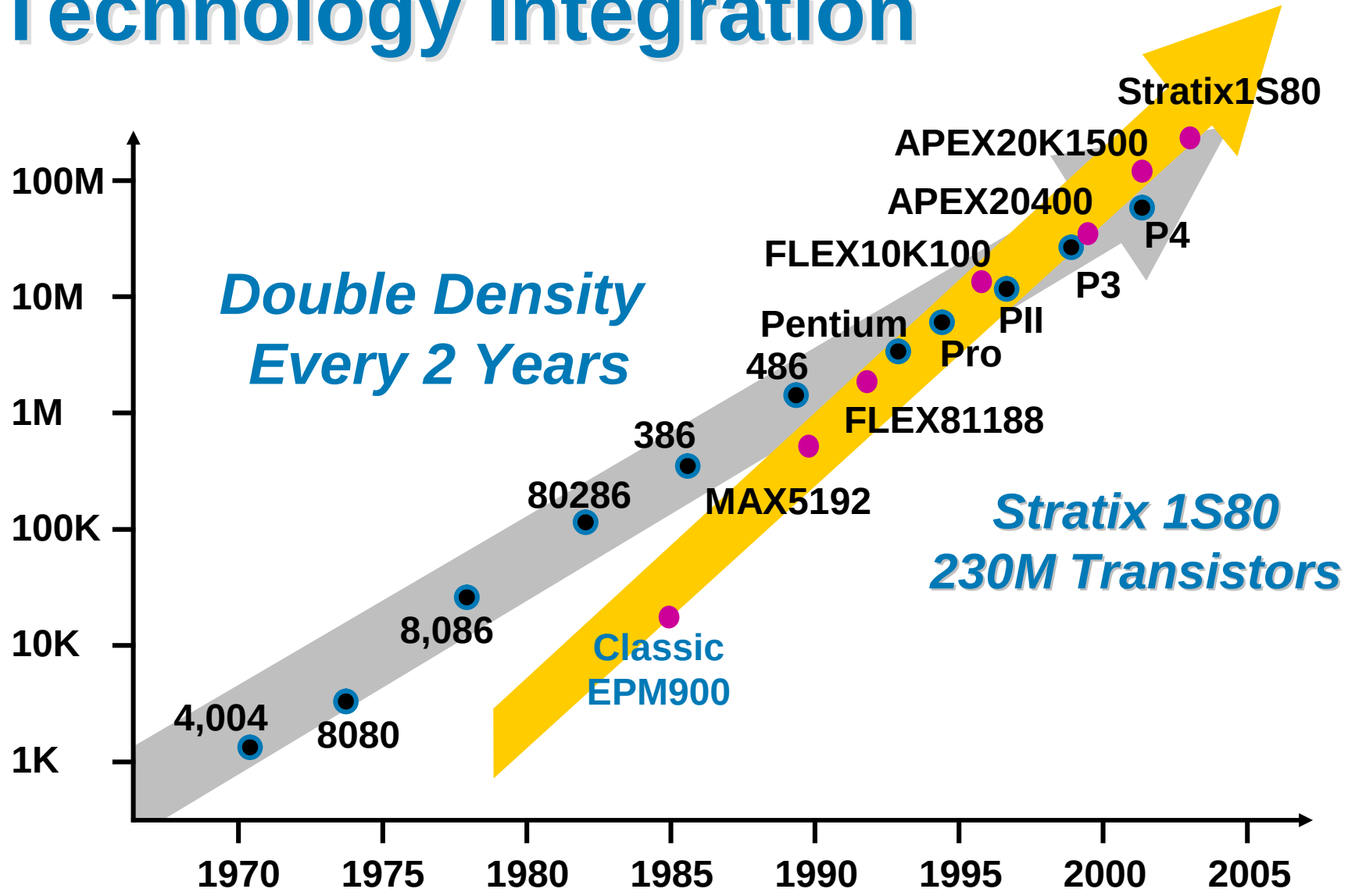
90nm Status

- Process
  - Up to 10 Layers Of Copper
  - Second Gen. Low-k (K < 3)
  - Vcc: 1.2V (16A Tox)
  - Lithography: 193nm
- Project Status
  - Started In May 2001
  - Actively Optimizing Process with TSMC
  - Process Available Early 2003
  - Production Targeted 2H 2003

300mm Status

- Development & Qualification Completed in 2001
- Production Ready for 2002-2003 as Demand Increases
  - Provide Cost Reduction (Lower Defect Density)

Technology Integration



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Rising Costs of ASIC Development

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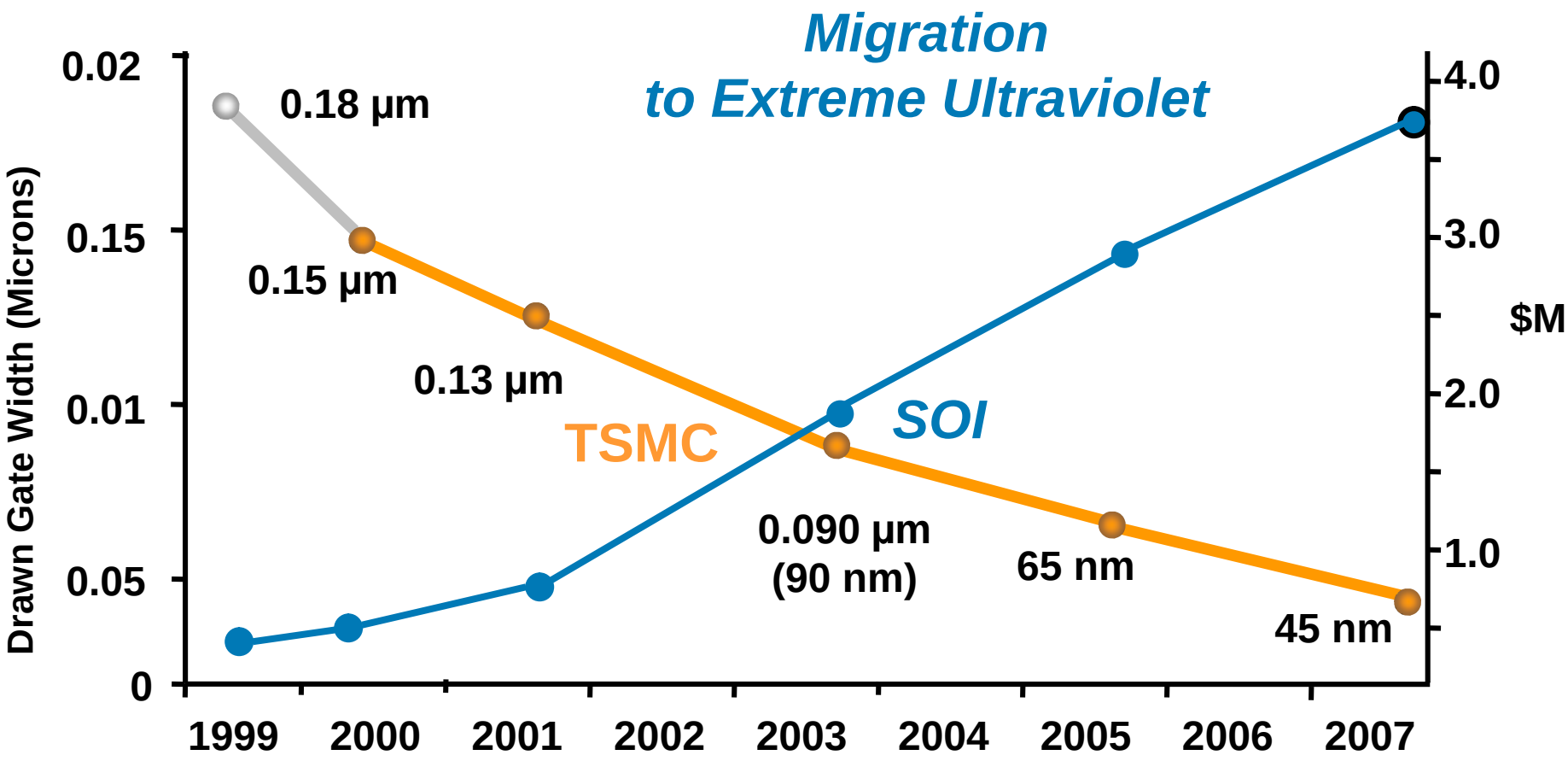
Dramatic Mask Cost Increase



Source: International Technology Roadmap for Semiconductors 2001
TSMC 2002 Technology Seminar

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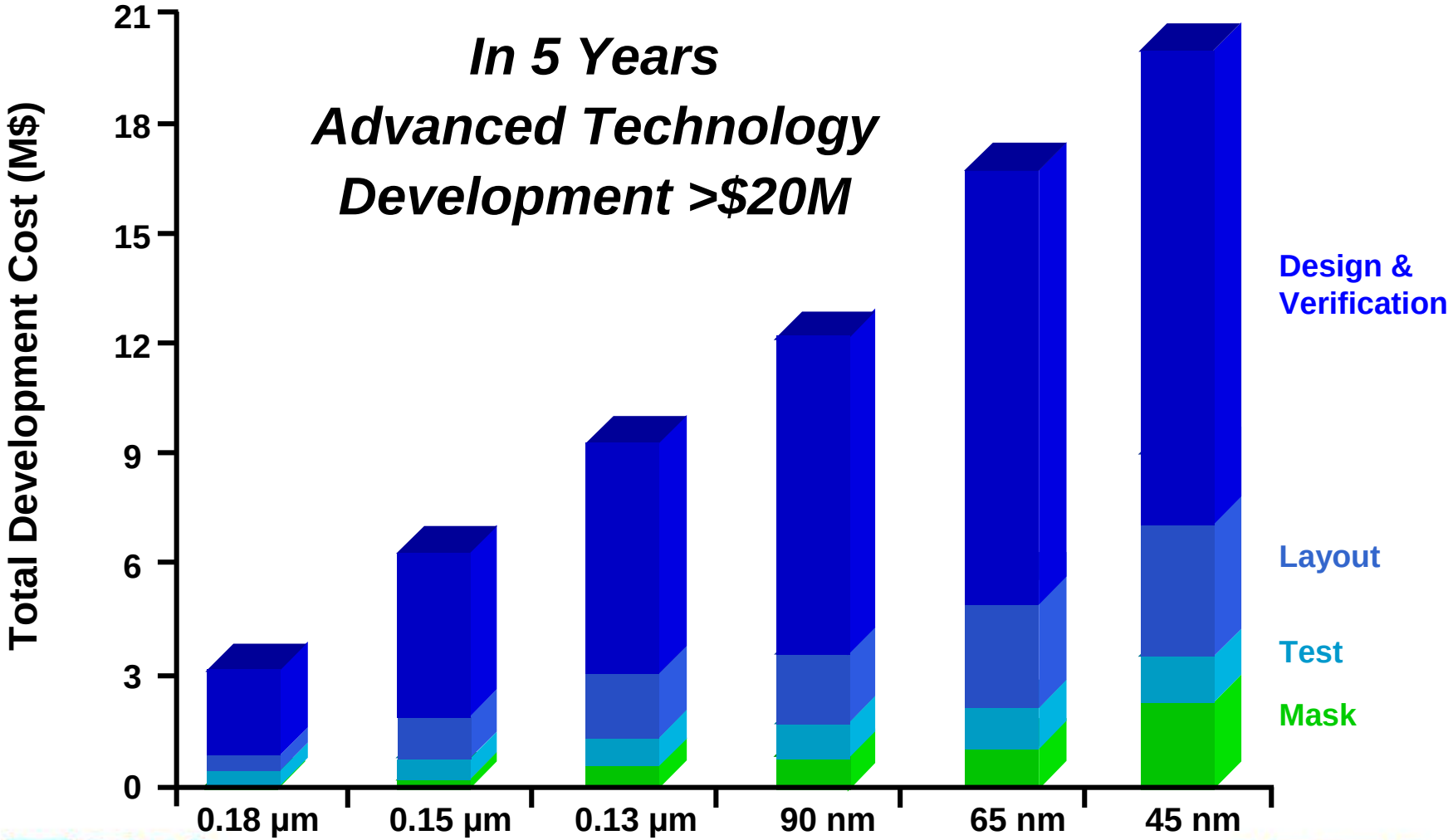
Increasing Development Cost



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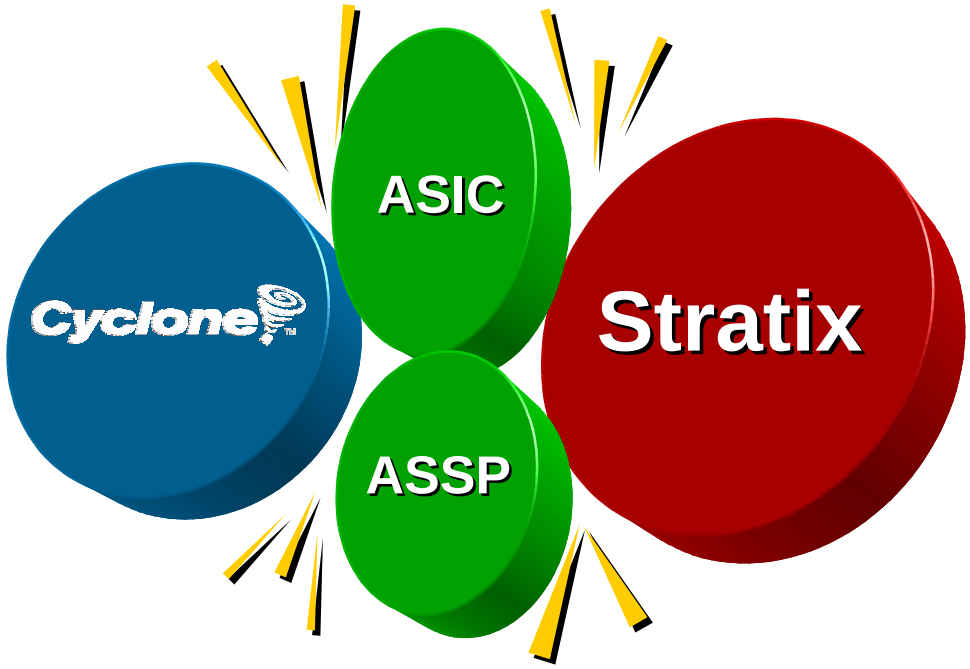
Increased Market Opportunities



Rising Technology & Development Costs Favour SOPC Design

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Core Technology Improvements

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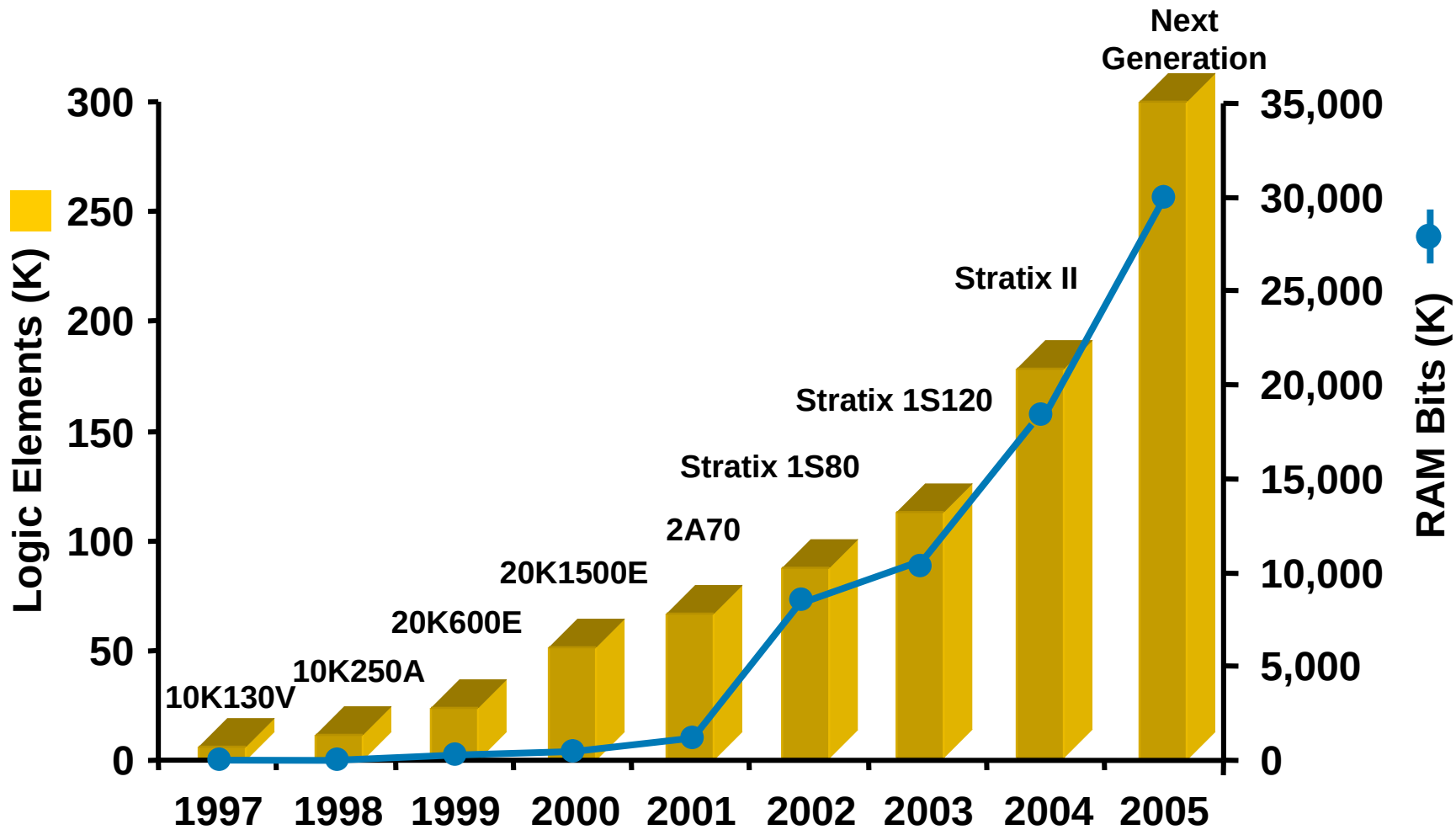
Logic Resource Growth Roadmap



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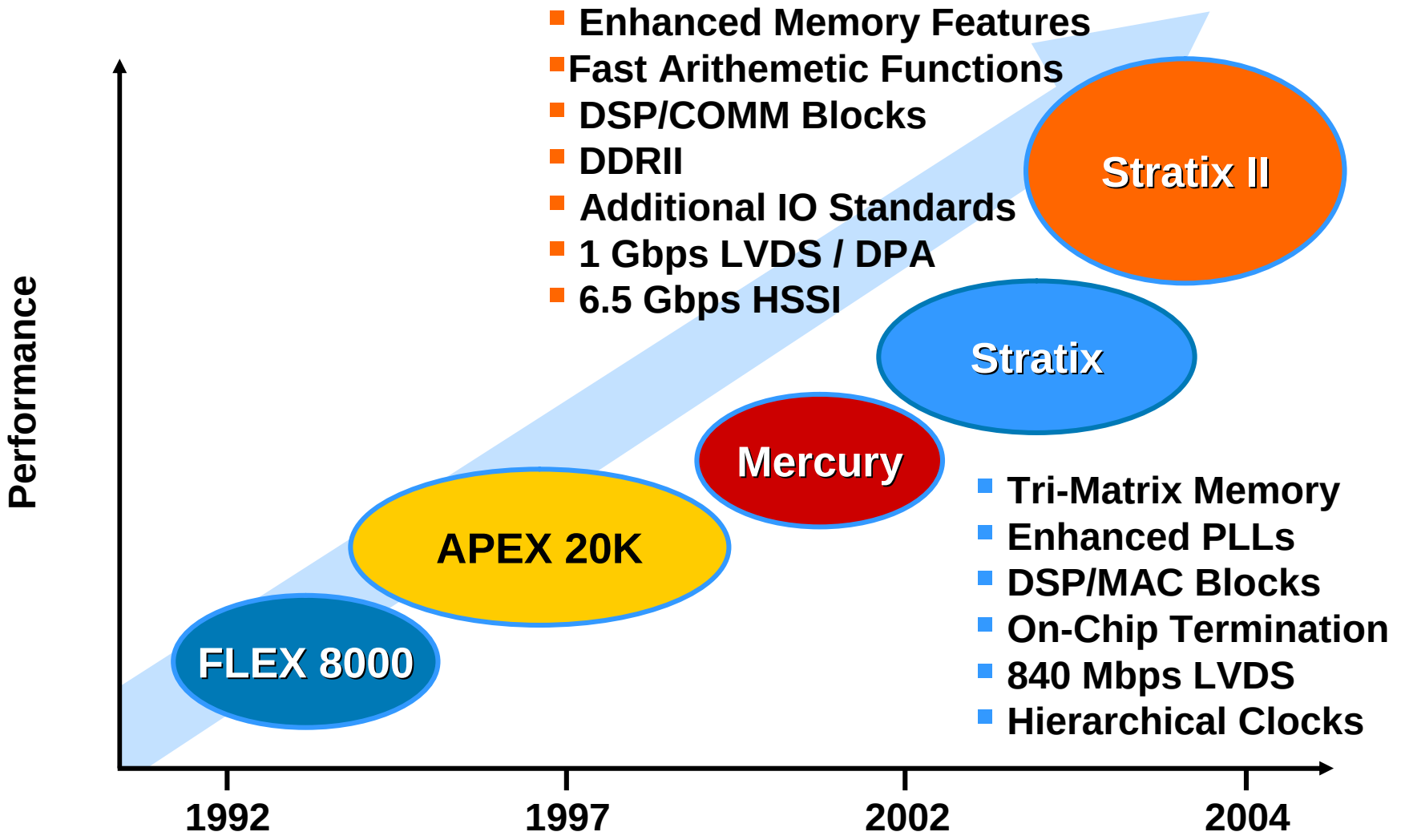
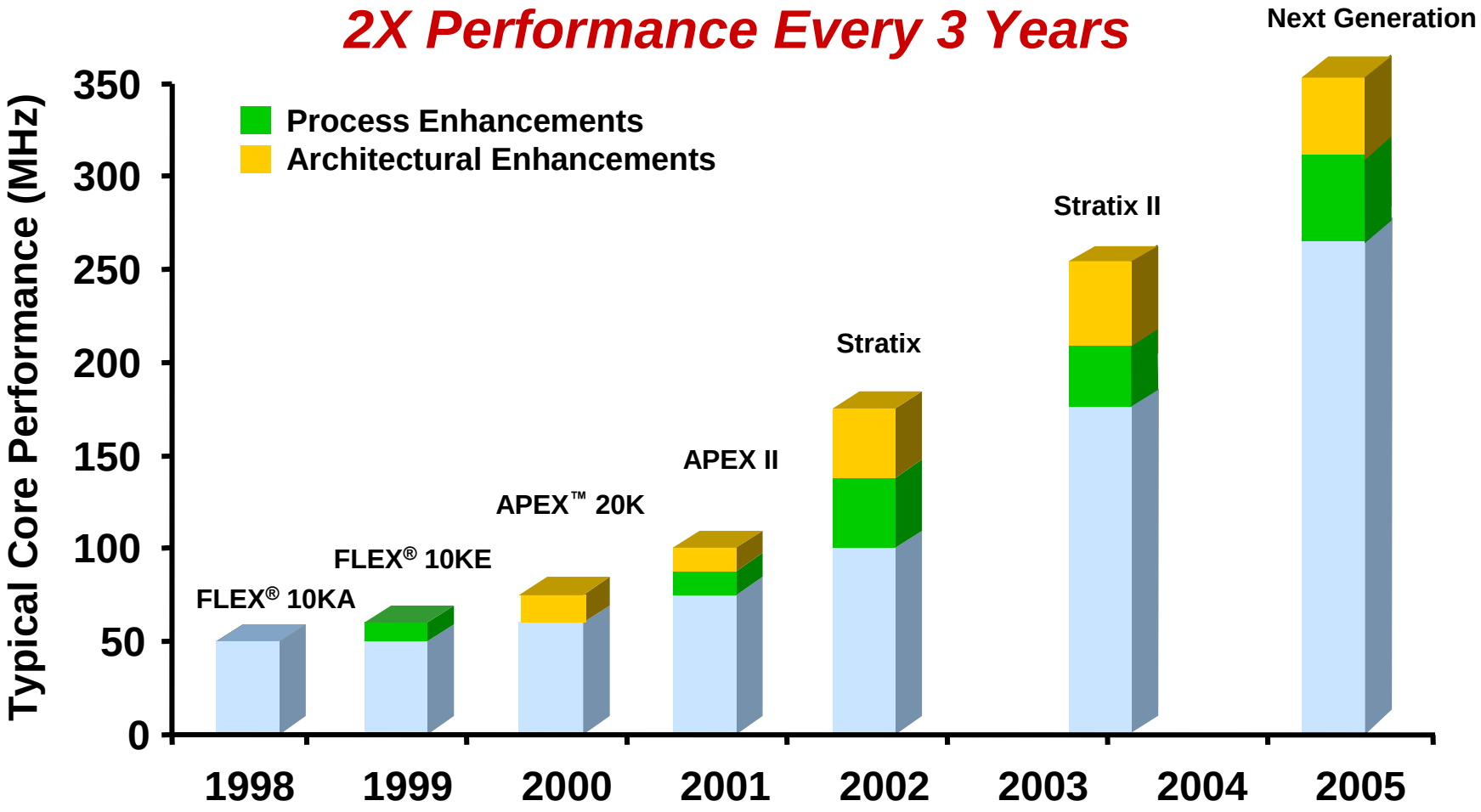
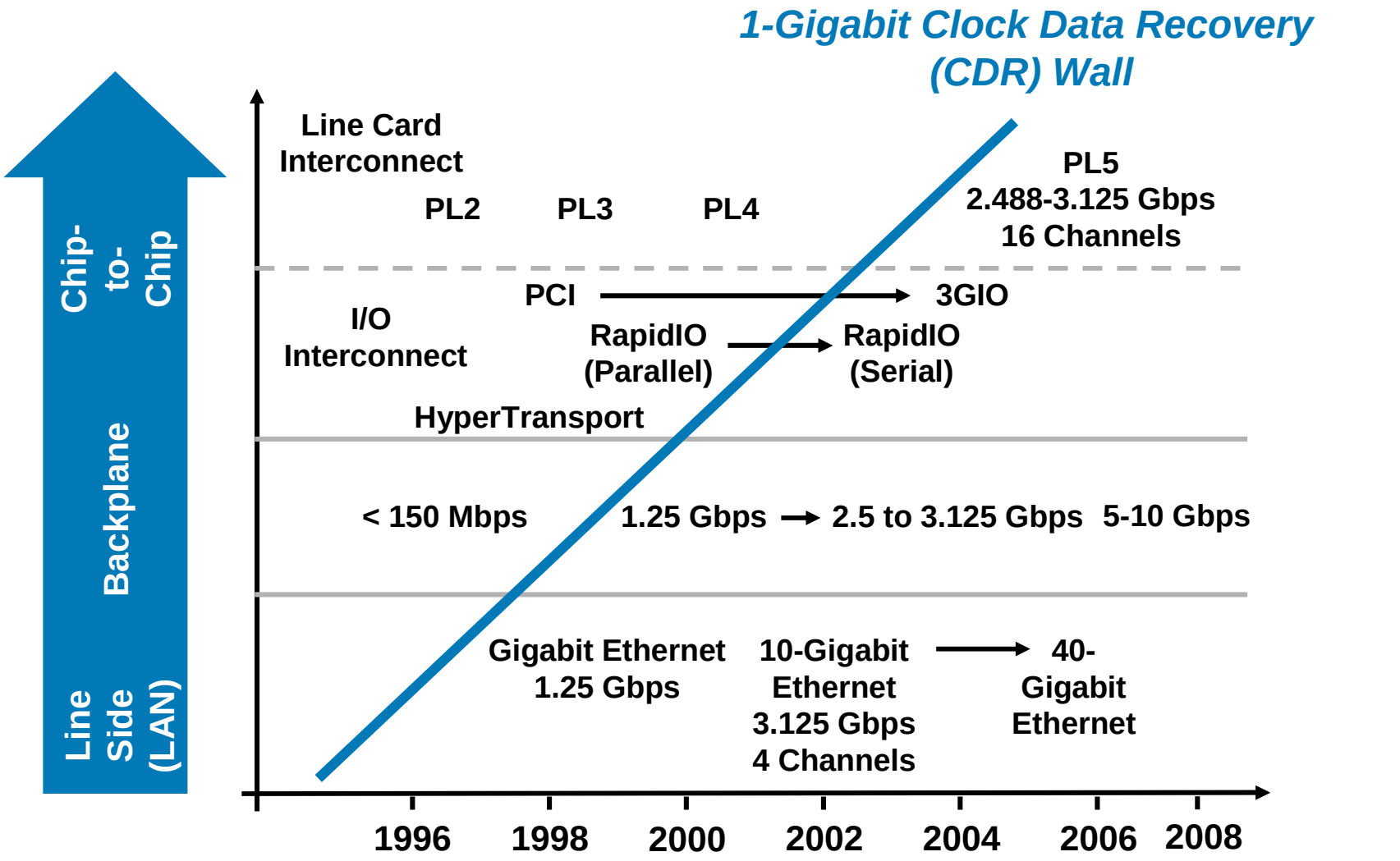
Core Logic Evolution



LUT Core Performance Roadmap



High-Speed Interface



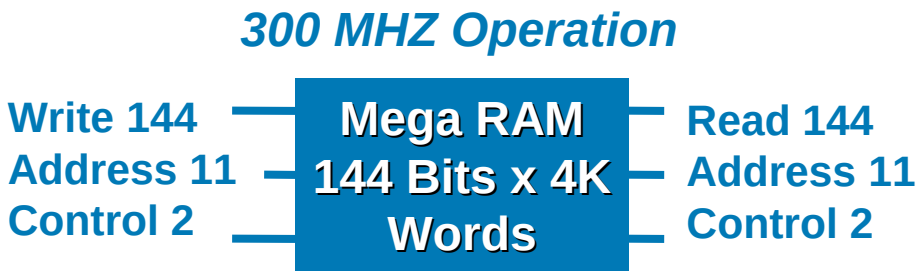
High-Speed I/O Roadmap

	Mercury™ APEX™ II	Stratix GX	Stratix II GX	Next Generation
Architecture				
Channel Performance	1.25 Gbps	3.125 Gbps	6 Gbps	12 Gbps
Electrical Standards	▪ 1.25-Gbps CDR ▪ 1.25-Gbps LVDS ▪ 1.25-Gbps PCML ▪ 1.25-Gbps LVPECL ▪ 1-Gbps HyperTransport ▪ 250-MHz HSTL ▪ PCI-X	▪ 3.125-Gbps LVDS With CDR	▪ 3.125-Gbps CML With CDR	▪ PAM
Bus Protocols	▪ SPI-4 Phase 2 ▪ Gigabit Ethernet ▪ 1-Gbps Fibre Channel ▪ 1-Gbps RapidIO ▪ 415-Mbps Utopia IV ▪ 200-MHz CSIX	▪ RapidIO Serial/Parallel ▪ 1G, 2G Fibre Channel ▪ InfiniBand ▪ 10G Ethernet (XAUI) Lineside Backplane ▪ SONET Backplane	▪ RapidIO ▪ FChannel ▪ InfiniBand ▪ SPI5, 3GIO ▪ SONNET	▪ Chip-Chip ▪ Backplane ▪ Emerging High Speed Standards
	2001	2002	2003	2004 2005

Integrated Memory

- High Speed Data Processing & Communications
  - Faster Wire Speeds
  - High Port Integration
  - More Latency
  - Example: Stratix EP1S80 9 Mega RAMs

- ***86G Bits/Sec***
- ***314 Pins /RAM***
- ***2800 Pins Provide Same External Memory Bandwidth***



Embedded Memory Roadmap

Architecture	APEX II	Stratix	Stratix II	Next Generation
Features	▪ True Dual-Port Mode ▪ Packing Mode ▪ Mixed Width Mode	▪ Embedded Shift Register Mode ▪ DDR Mixed Width Mode ▪ Three Sizes of Blocks ▪ Byte Enable ▪ Mixed Clock Mode ▪ Preload	▪ Embedded Error Control Circuitry (ECC) ▪ DDR ▪ Tri-Matrix	▪ Embedded CAMs ▪ Embedded Error Control Circuitry (ECC) ▪ High Density Storage
Performance	250 MHz	300 MHz	550 MHz	750 MHz
Technology	SRAM	SRAM	▪ SRAM	▪ SRAM ▪ Embedded DRAM
	2001	2002	2003	2004 2005

Excalibur™ Nios™ Roadmap

	Nios Version 2.0	Nios Version 3.0	Nios II
Processor			
Performance	80 MHz / 40 DMIPS	150 MHz / 75 DMIPS	250 MHz / 167 DMIPS
Features	▪ Simultaneous Multi-Master Bus • Intelligent Peripherals ▪ User-Defined Instructions ▪ SDRAM Controller ▪ 10/100 Ethernet I/F ▪ PCI MT32 ▪ Software IDE ▪ On-Chip Debug ▪ Software Trace ▪ Linux, ATI Nucleus ▪ Speed / Size Optimizations	▪ Communication Controller • HDLC, T1/E1 Framer • Time-Slot Assigner ▪ Integrated MMU ▪ Configurable On-Chip Cache ▪ High-Speed Memory Interface ▪ C-Level Simulation • Hardware & Software ▪ Multi-Processor Support • Inter-Processor Communication • Software Debug	▪ Application-Specific Processor Extensions ▪ System Profiler • Hardware & Software • Optimized Extensions Based on Target Application (Critical Loop) ▪ Speed Enhancements ▪ Additional Peripherals
	2001	2002	2003

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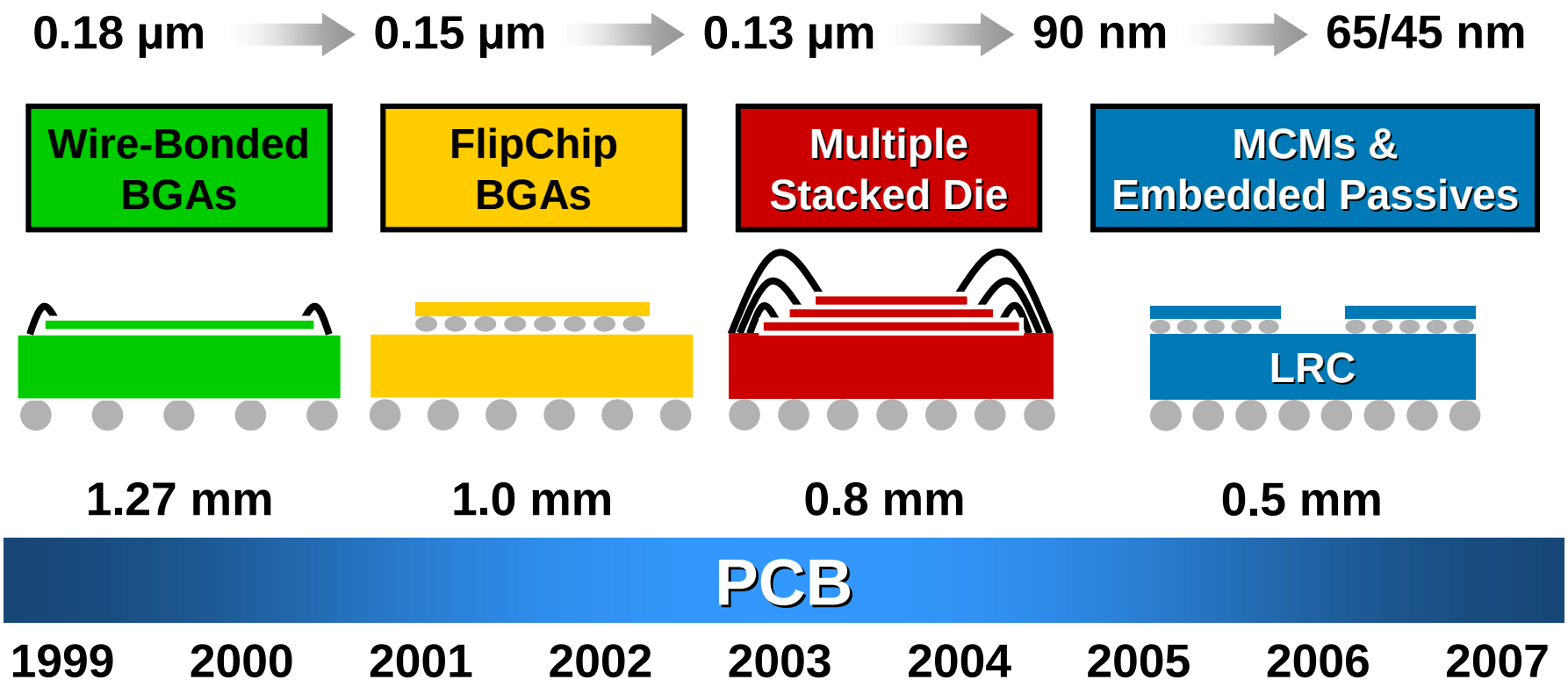
Packaging Technology Roadmap



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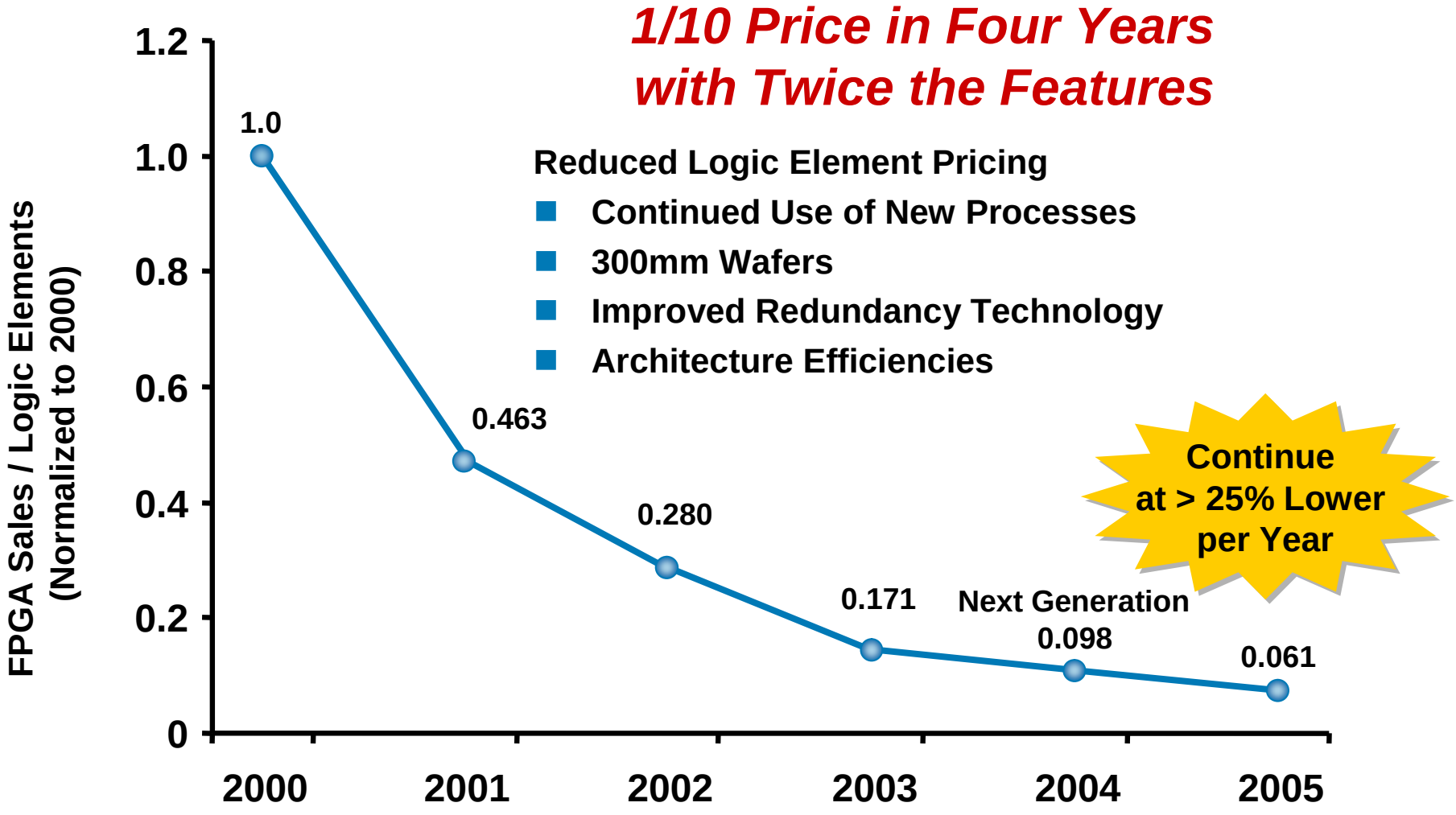
Pricing Roadmap



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Product Family Roadmaps

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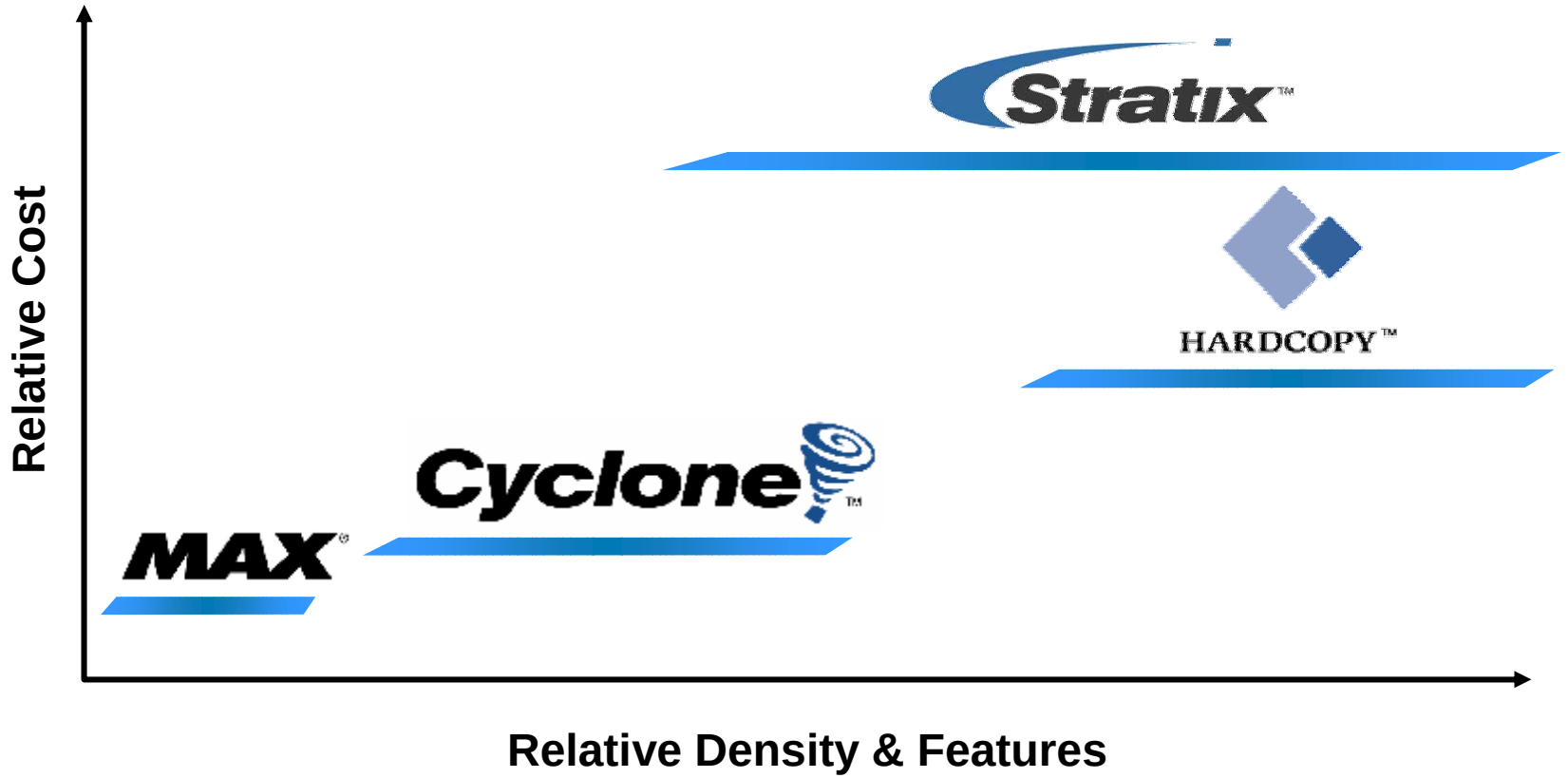
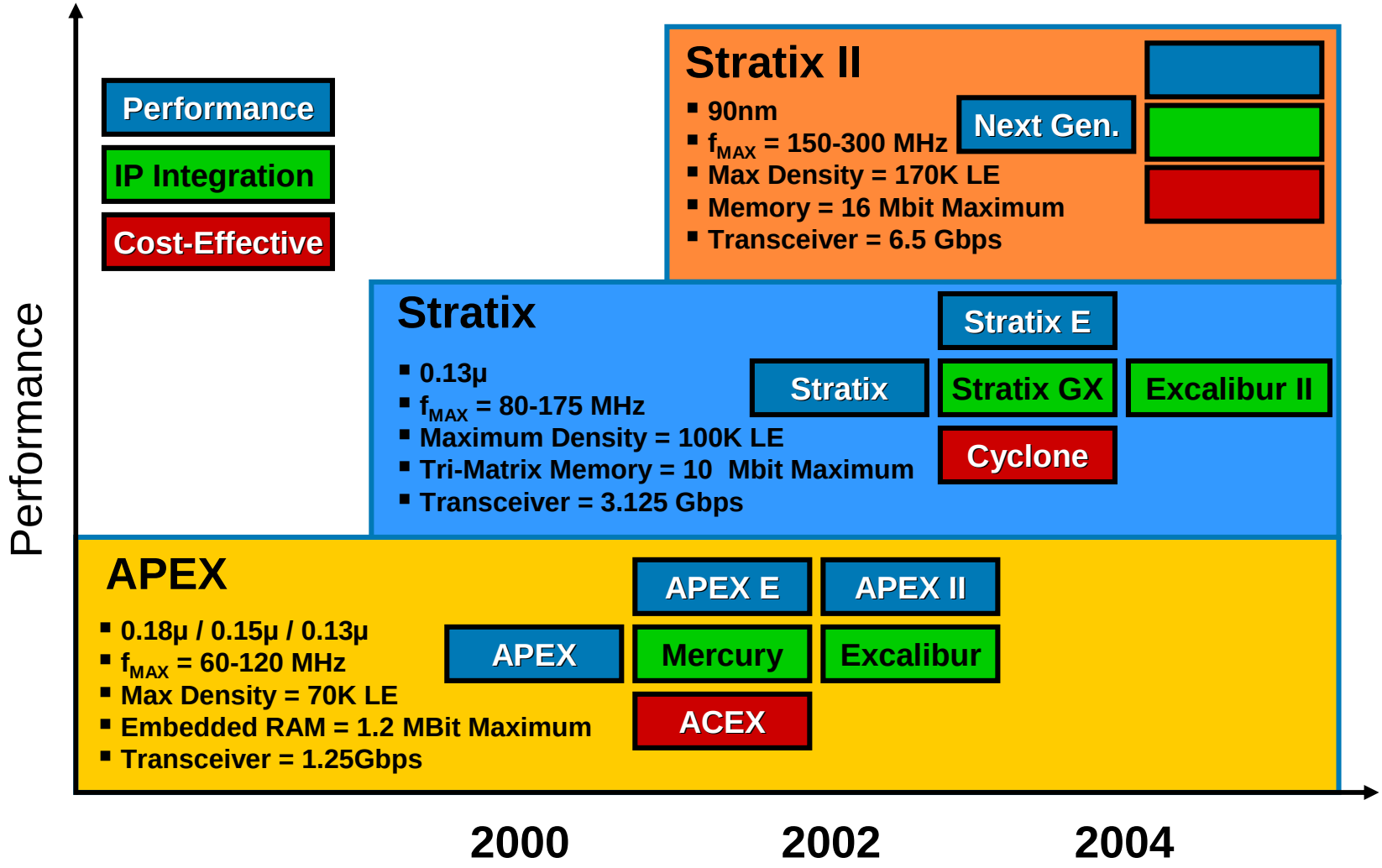
Altera's General-Purpose Product Portfolio



Addressing Features & Cost

Altera FPGA Roadmap



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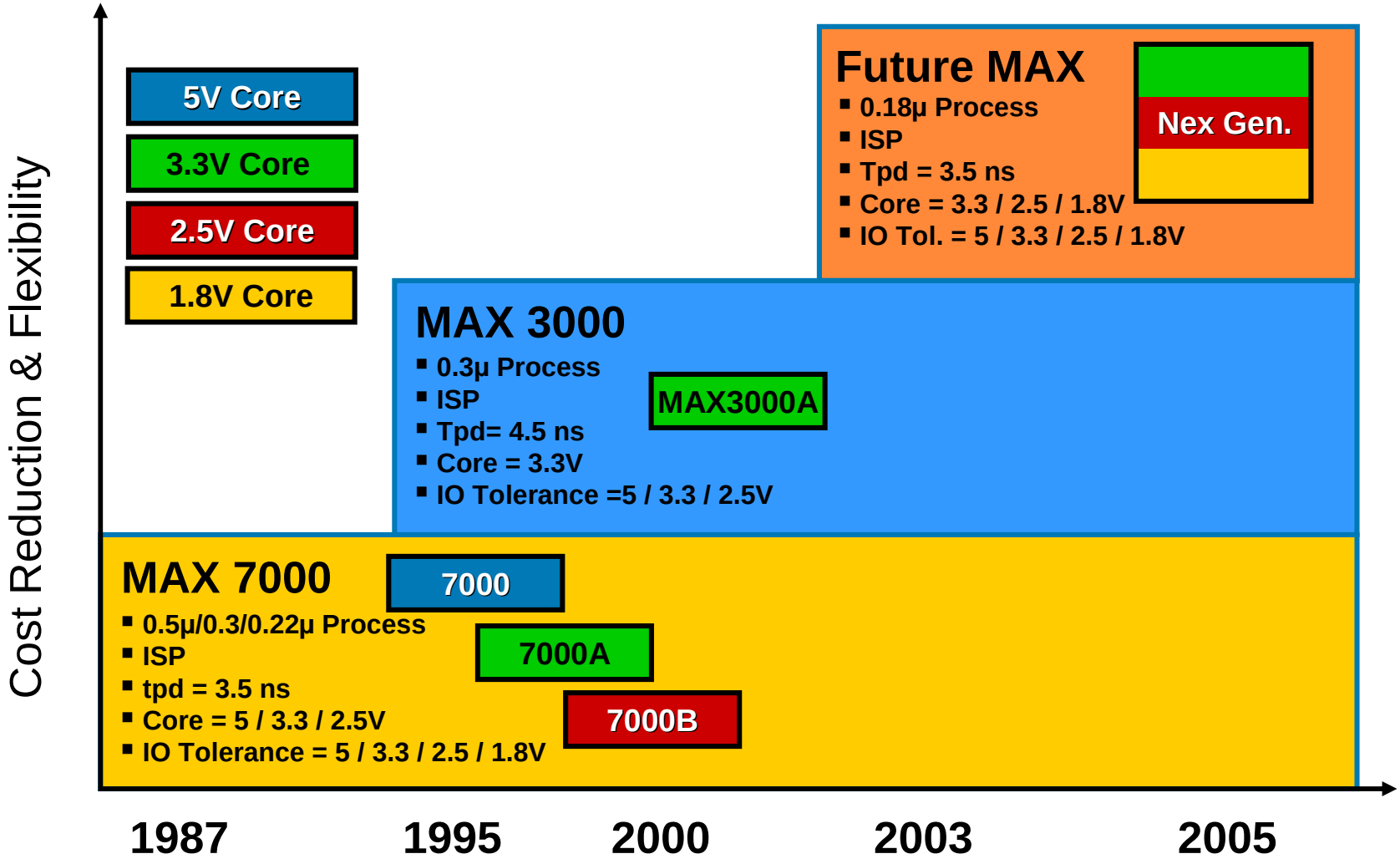
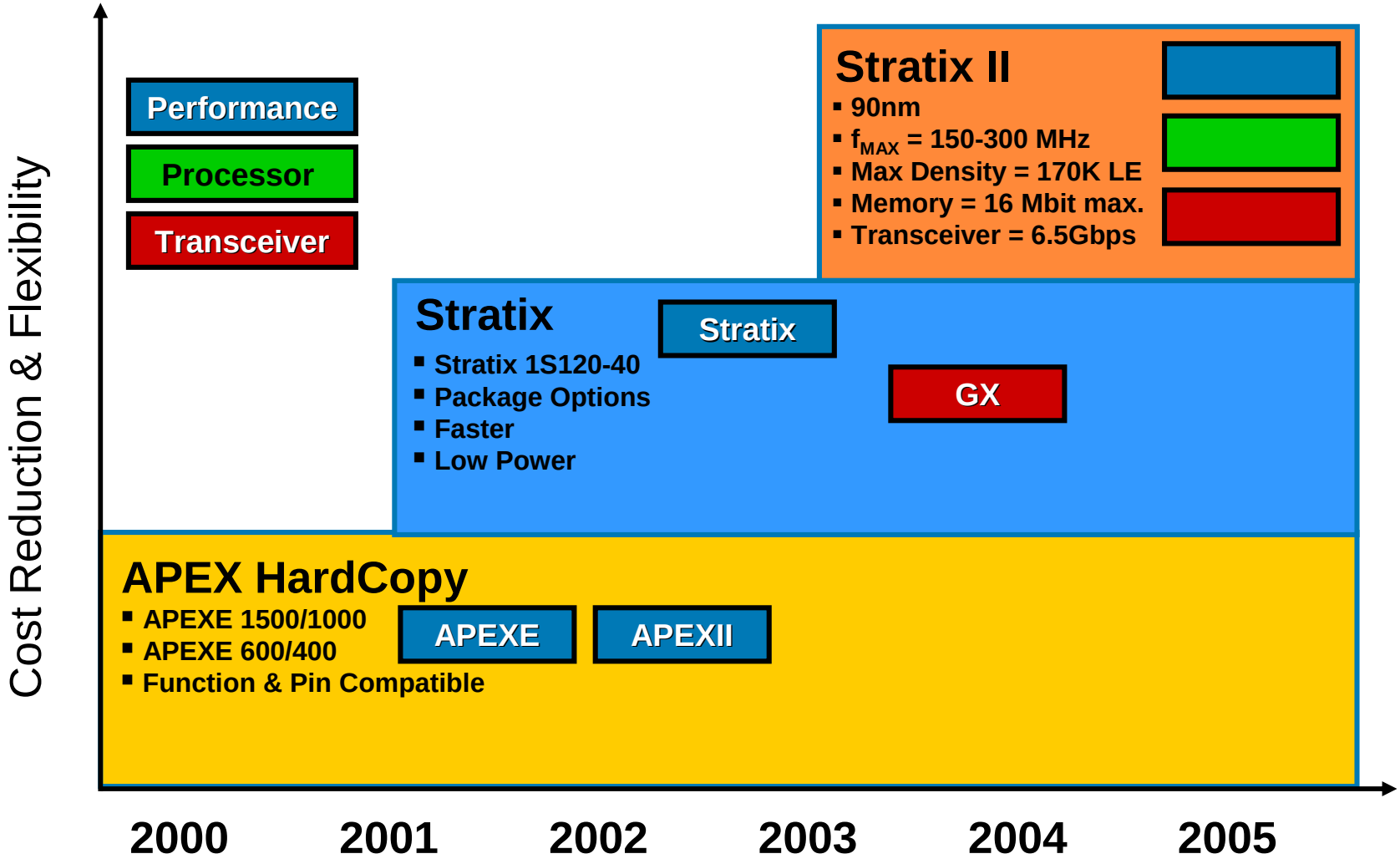
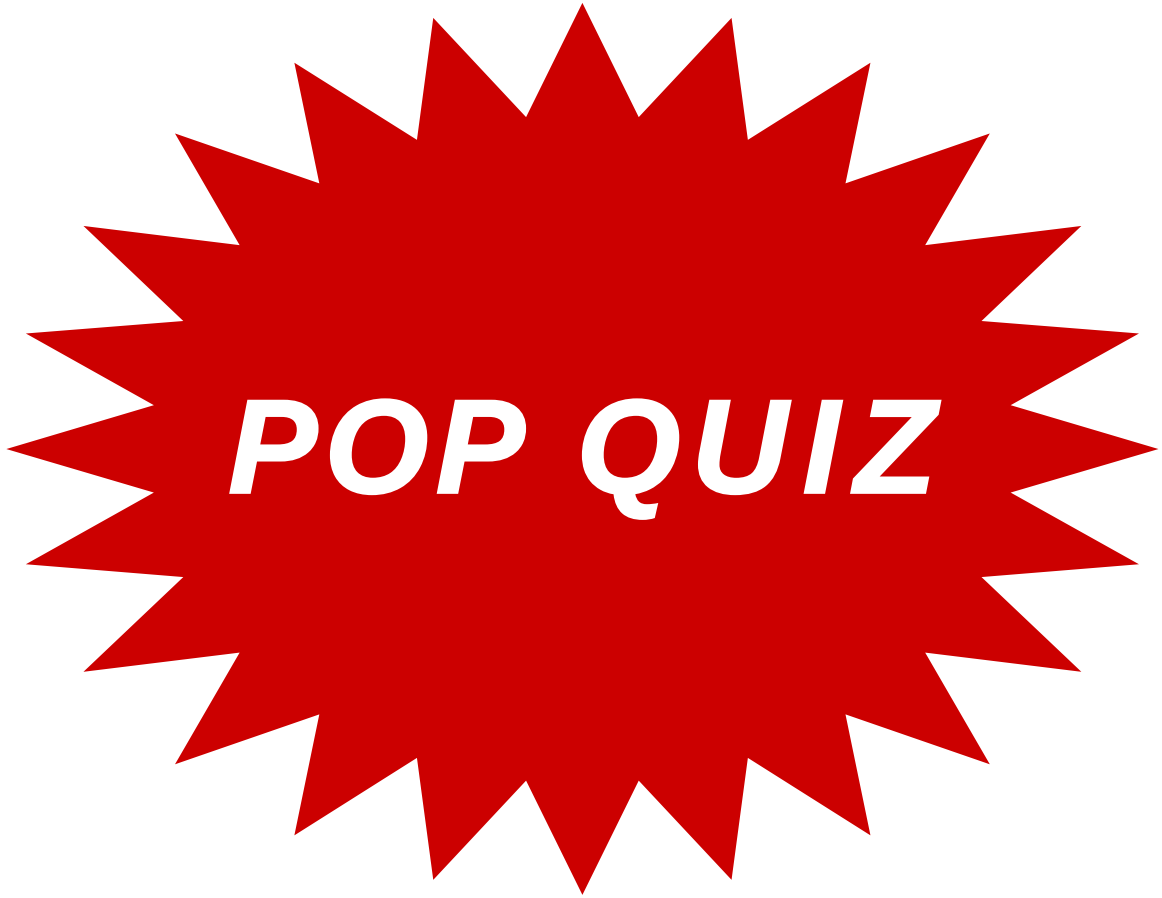
Altera CPLD Roadmap



Altera HardCopy Roadmap




POP QUIZ

Pop Quiz

- Stratix 의 생산 공정과 Core Voltage 로서 맞는 것은 ?

1. 0.25um, 2.5V
2. 0.18um, 1.8V
3. 0.15um, 1.8V
4. 0.13um, 1.5V

Pop Quiz

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3. 0.15um, 1.8V
4. 0.13um, 1.5V

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Development Tools

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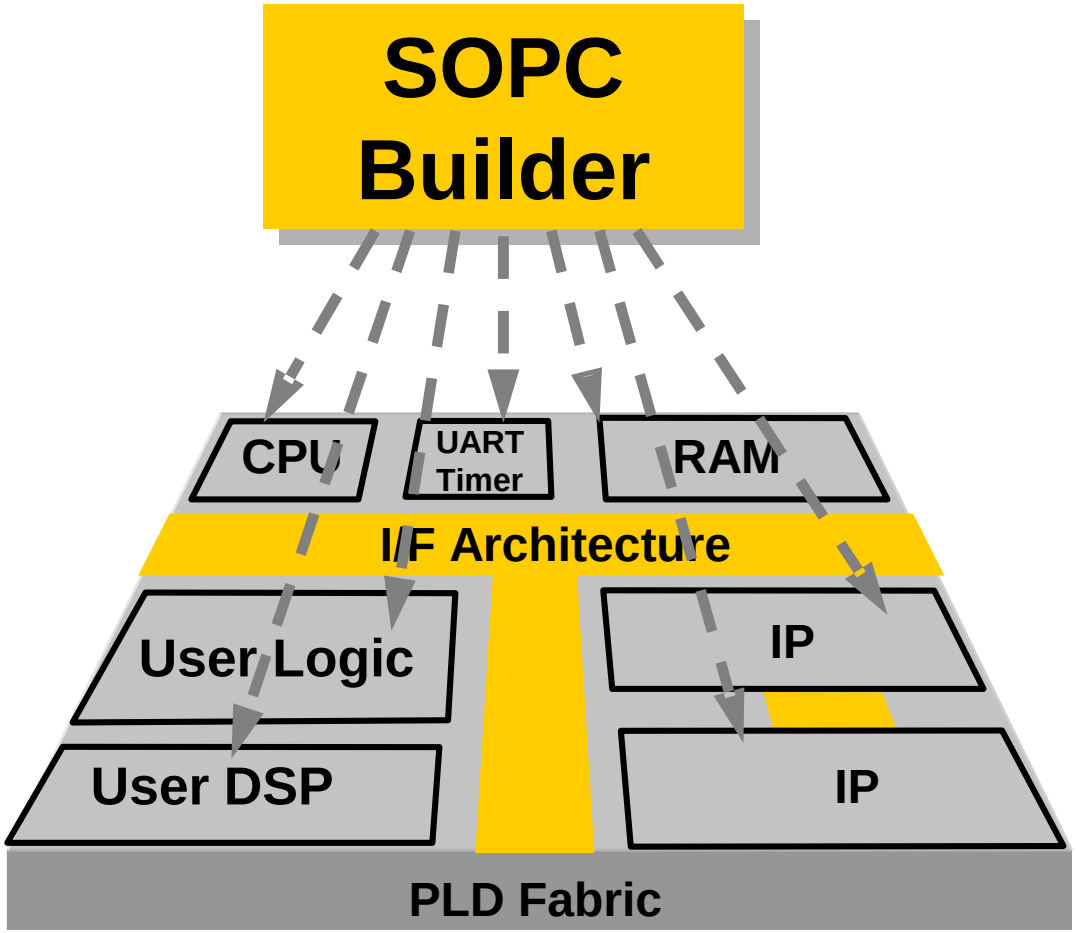
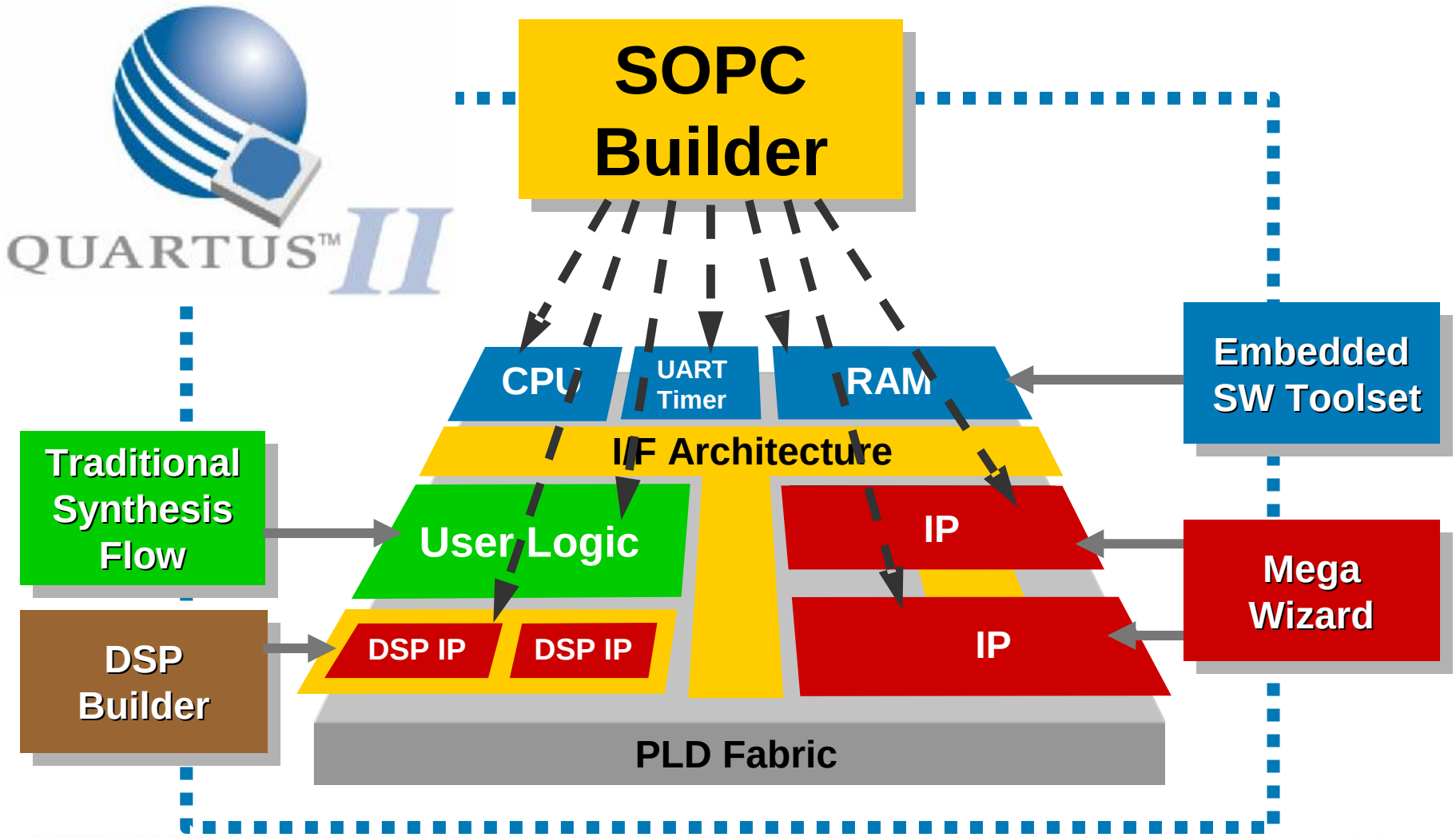
Tools Roadmap

- Altera Will Continue to Focus on Areas Where We Add Most Value
- Continue to Partner with Leading 3rd Parties Where They Provide Incremental Expertise & Focus
- SOPC Builder & System Design Automation Will Be Our Major Focus

SOPC Design Tools



SOPC Design Tools



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SOPC 3.0 Builder

- Build Custom Companion Chip for Your Processor-Based System with SOPC Builder
  - Interface to Popular Microprocessors
    - PowerPC
    - TI DSP
    - PCI
  - Custom Peripheral Content
    - Communications IP
    - Signal Processing Algorithms
    - Memory Interfaces
  - Hardware Acceleration Functions
    - Security IP
    - Image Processing
    - Traffic Management / Routing Algorithms

SOPC Builder Roadmap

Quartus II v 2.2
SOPC Builder 2.7

- Native Synthesis Support
- Cyclone Device Support

Quartus II v. 3.0
SOPC Builder 3.0

- External Device Bus Standards
  - PowerPC (60x Bus)
  - TI C6X
  - PCI
- IP Bus Standards
  - AMBA
  - PVCI
  - Wishbone
- DSP Builder Integration
- Atlantic Bus Support
- SignalTap II Support
- Web Update

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Programmable Systems

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Programmable System Reconfiguration

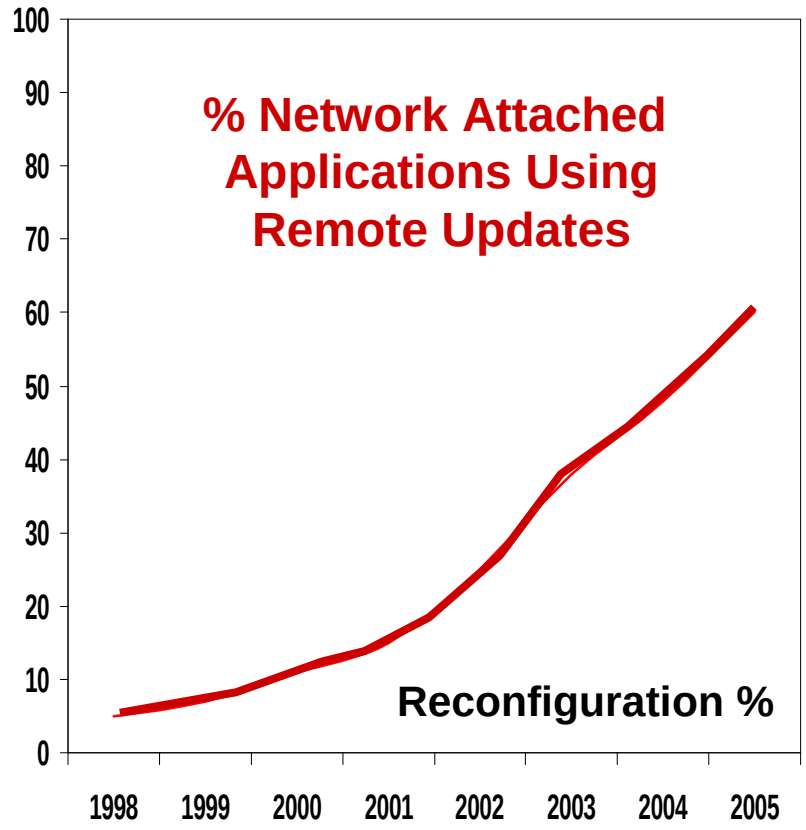
In Production Today Using Altera FPGAs

Requires Complex Hardware/Software Support

Group 1	*Group 2*	*Group 3*	*Group 4*
1 Year – Months	**Days - Hours**	**Mins-100mS**	**1ms-1us**
■ System Upgrades ■ Bug Fixes ■ Feature Upgrades ■ Remote System Monitor	■ Reboot & Upgrade ■ Multifunction Platform for Different Users	■ Reuse Hardware to Perform Multi-Functions ■ Reduce Redundant Hardware Costs	■ Reconfigurable Computing ■ Context Switch Based Upon Function Under Real-Time Software Control

Re-Configurable Solutions

- Increasing Use of Remote System Updates
- FPGA Images Uploaded Over Internet or Private Network
- Mainly Using Ethernet
- Both System Upgrades & Remote Monitoring Using Programmability of FPGAs
- Bug Fixes, System Upgrades, New Features
- Significant Cost Advantages over Technician Visit



Programmable Logic Differentiates Production Solution

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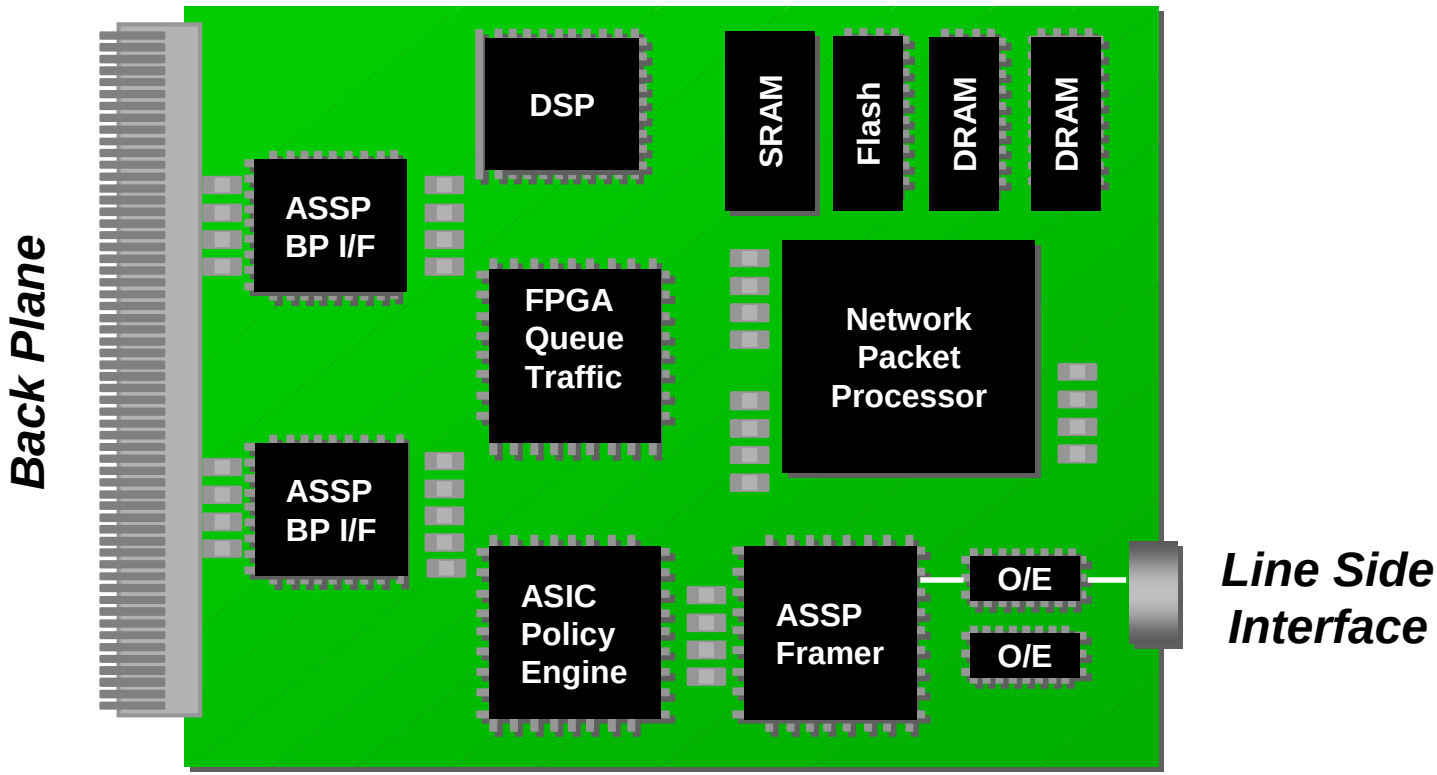
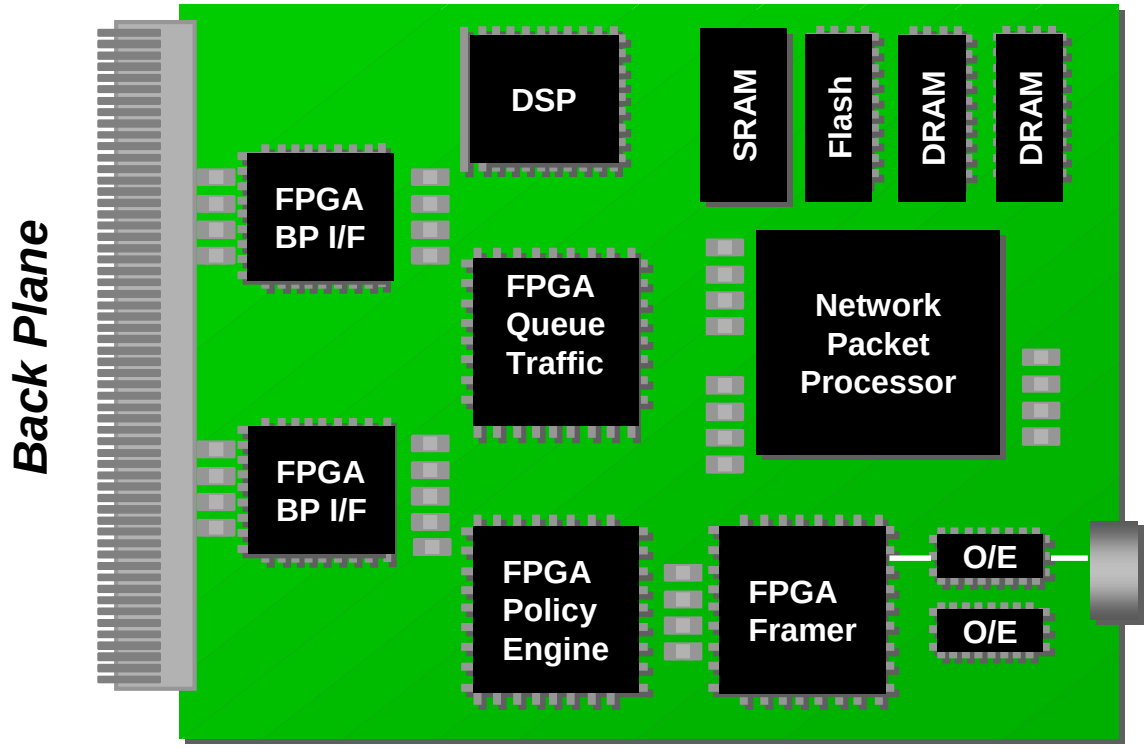
Future System Design



Future System Design

- Microprocesor
- DSPs
- Memory
- SOPC
- Analog
  - ASIC & ASSP for High-Volume Projects



Conclusions

- Altera Continues to Innovate & Deliver Compelling SOPC Solutions
- Focused on Complete Solutions
  - Programmable Device Families
  - Leading Design Automation Tools
  - Broad Range of IP
  - Comprehensive Worldwide Technical Support
- Performance, Price, Integration Will Dramatically Expand SOPC Market

Altera SOPC
Solution for Rapid Growth