SOPC WORLD 2002

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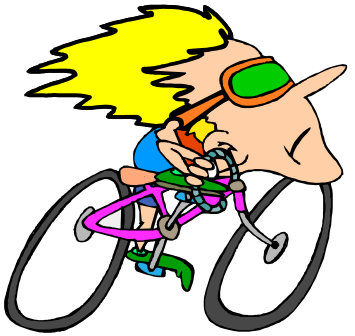
SOPC Builder

From Concept to System
in Minutes!

ALTERA.

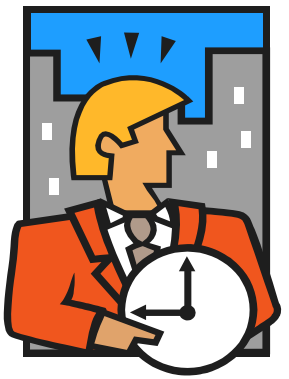
Lure of System-on-a-Chip

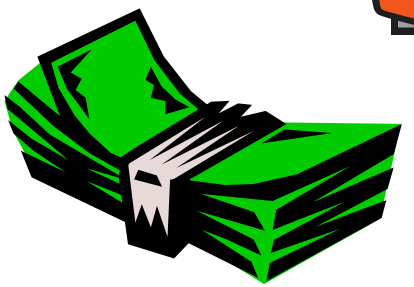
- Smaller, Faster, Cheaper, Better
- Integration
  - Lower Device Count
  - Lower Board Cost
- Performance
  - High Speed
  - Low Power
- Exact-Fit Solution for Custom System



Realities of ASIC Development

- High Barrier to Entry
  - Time: 12 to 18 Months
  - Money: >$1,000,000
  - Tools: >$100,000
  - Experience
    - Co-Simulation
    - Co-Verification
    - Prototype
  - High Risk

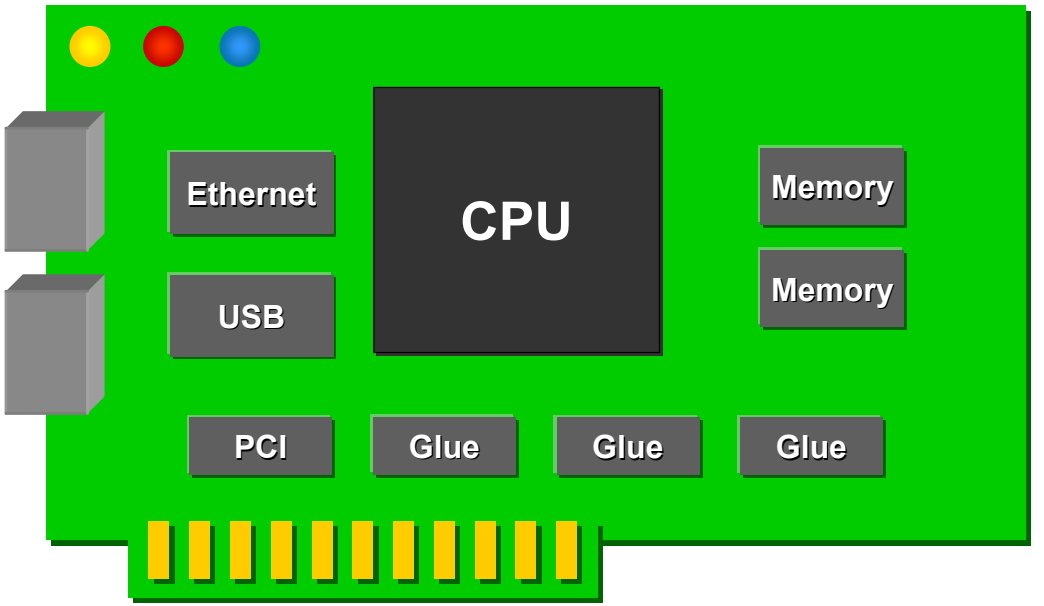




Alternatives?

Traditional Alternative to SOC

- Board-Level Integration
- Use Off-the-Shelf Parts
  - Processor
  - Memory
  - Peripherals
  - Glue Logic



Selecting Microprocessor/Controller

Encryption Decryption 100BaseT	Data bus width, bits	Address bus width, bits	Supply voltage, minimum	Supply voltage, maximum	Maximum current consumption, mA	Max. stdby. current consumption, µA	Max. sleep current consumption, µA	Maximum clock speed, MHz	Size of on-board RAM, bytes	Size of on-board masked ROM, bytes	Size of on-board EPROM in bytes	Size of on-board flash, bytes	No. of on-board counter/timers	No. on-board asynchronous serial ports	No. on-board synchronous serial ports	Number of on-board ADCs	Number of bits of resolution per ADC	Maximum number parallel I/O pins	Number of PWM outputs	Number of watchdog timers	Maximum number of chip select outputs	Number of interrupt pins to chip	Number of interrupt priority levels	Number of DMA channels	Typical price (thousands)
	16	24	4.5	5.5	140	5		28.7	4K	64K, 128K	0	128 K	5	2		8	10	82	8	1	4	7	16	2	$17
	16, 32		4.5	5.5	230	5		28.7	4K	256 K	0	256 K	7	2		8	10	106	8	1	4	9	16	4	$22.50
	8		4.5	5.5				50	8KB	128 KB	0	25K B		3	3	16	10	69	16	1	1	5	16	N/A	$23
	32		3.0	3.6	1000	990	250	62.5	8KB	N/A	N/A	N/A	8KB	n/a	n/a	n/a		29	n/a	1	5	5	16	4	$23
	32		3.0	3.6	1000	990	250	100	8KB	n/a	n/a	n/a		3	3	4	10	96	n/a	1	5	9	16	4	$22.50
	32		3.0 I/O; 1.75 core	3.6 I/O; 2.05 core	400	50/ 260	130	133	0	0	0	0	3	2	2	4	10	96	N/A	1	6	7	16	4	$15
	32		3.0 I/O; 1.75 core	3.6 I/O; 2.05 core	400	260	130	200	0	0	0	0	3	3	3	8	10	96	0	1	7	7	16	4	$16.25
	32		3.0 I/O; 1.75 core	53.6 I/O; 2.05 core	644	50	248	160	0	0	0	0		4	4	8	10	104	N/A	1	4	11	16	4	$23

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Excerpt from Embedded Systems Programming 2002 Buyer's Guide

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SOPC Builder Development Tool

System-on-a-Programmable-Chip (SOPC) Solution

Benefits of SOC without ASIC Penalties

Screen Capture from SOPC Builder Version 2.5

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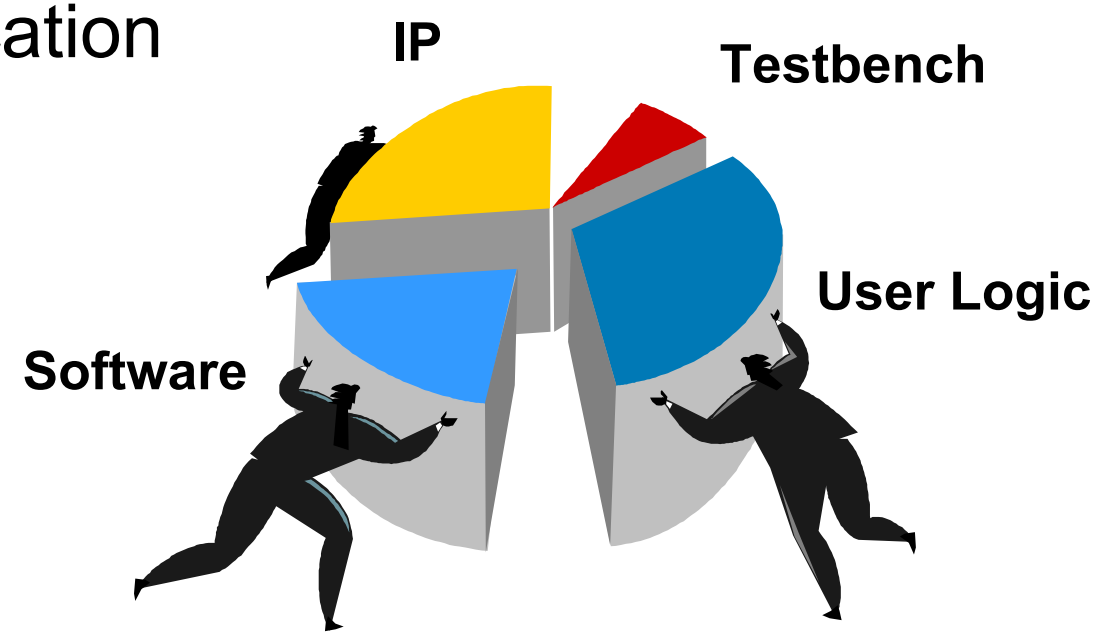
SOPC Builder Design Tool

- System Customization
- Component Integration
- Software Generation
- System Verification



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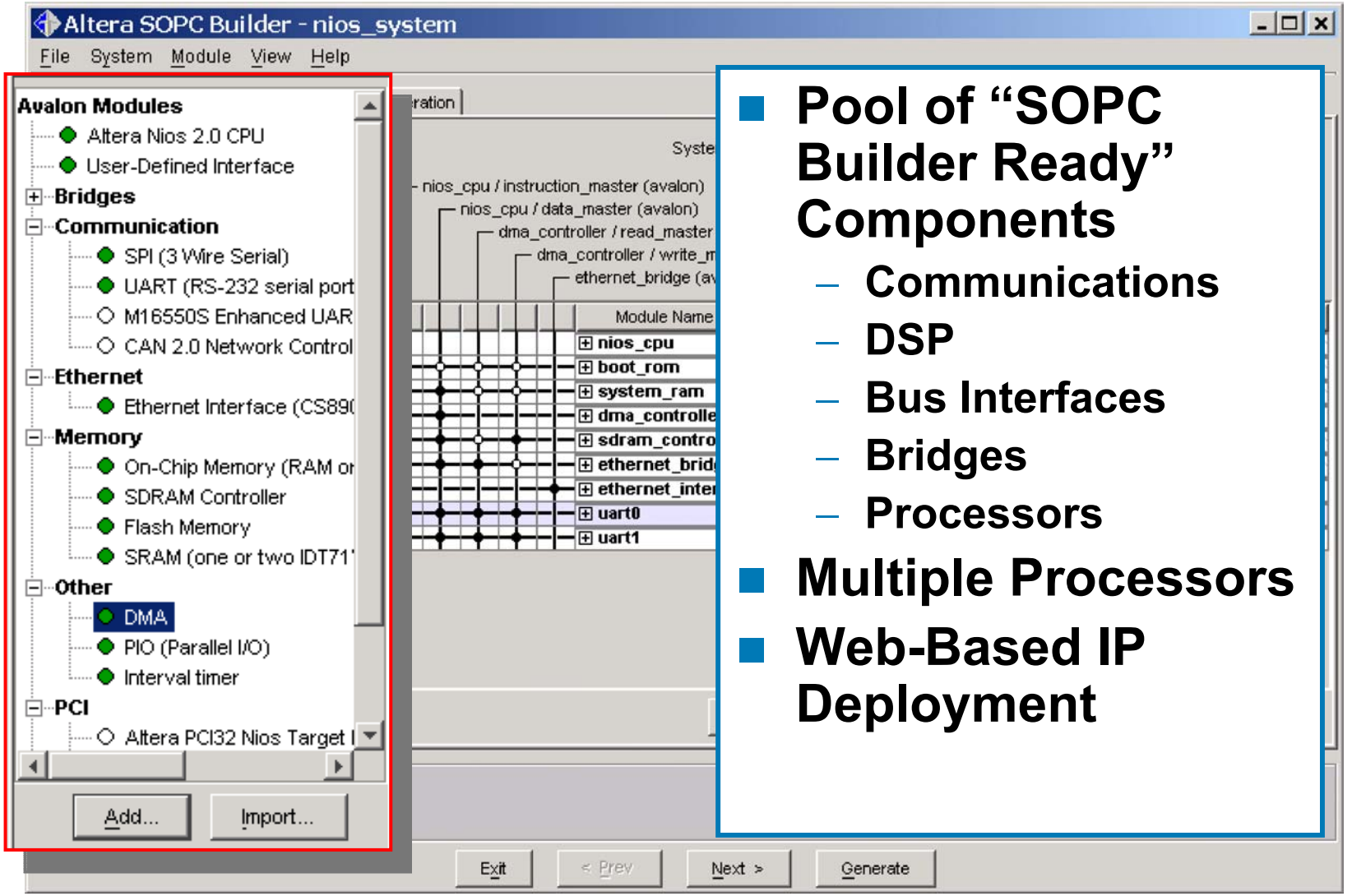
SOPC Builder Demo

ALTERA.

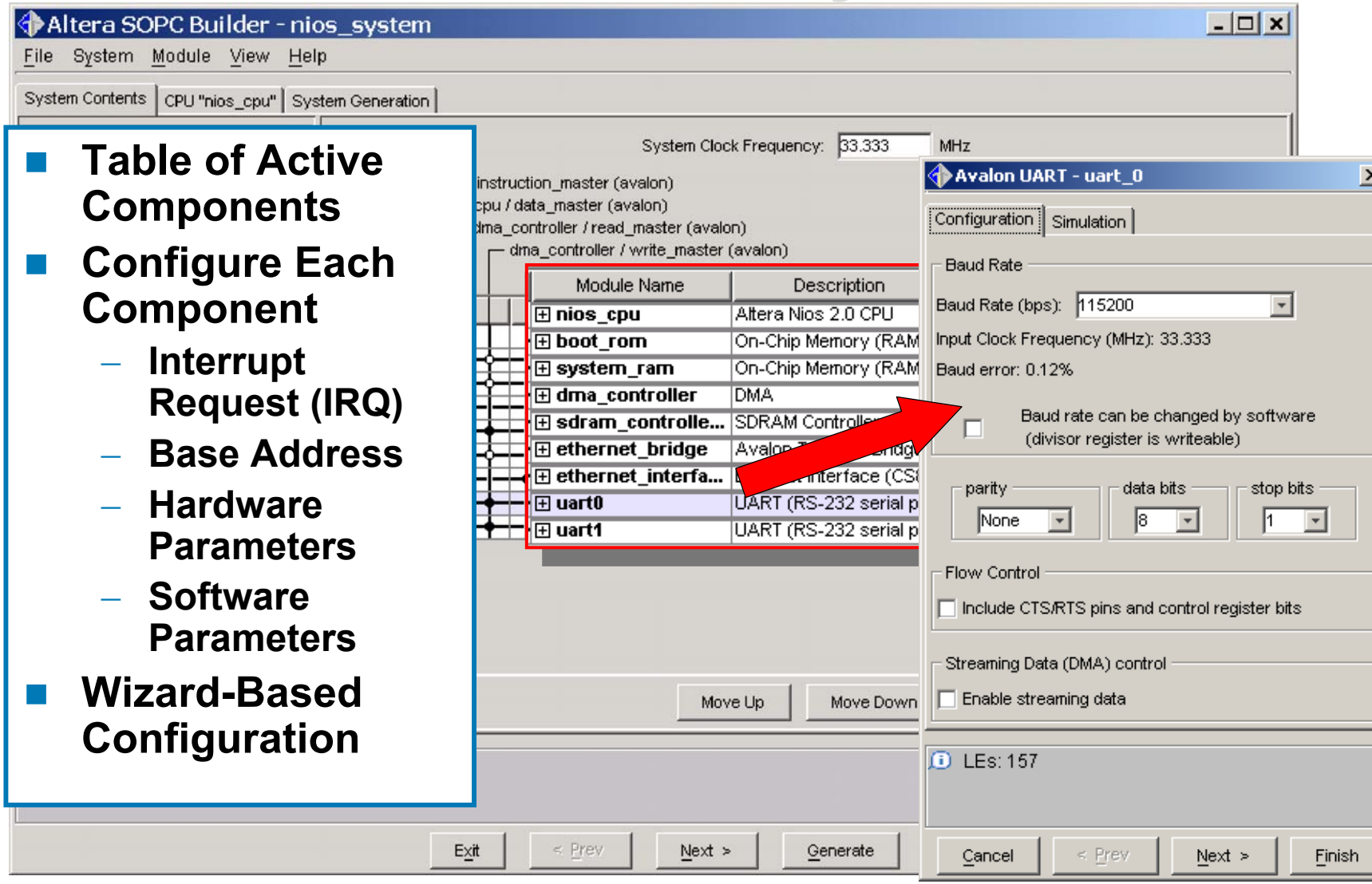
Customization - Just What You Need



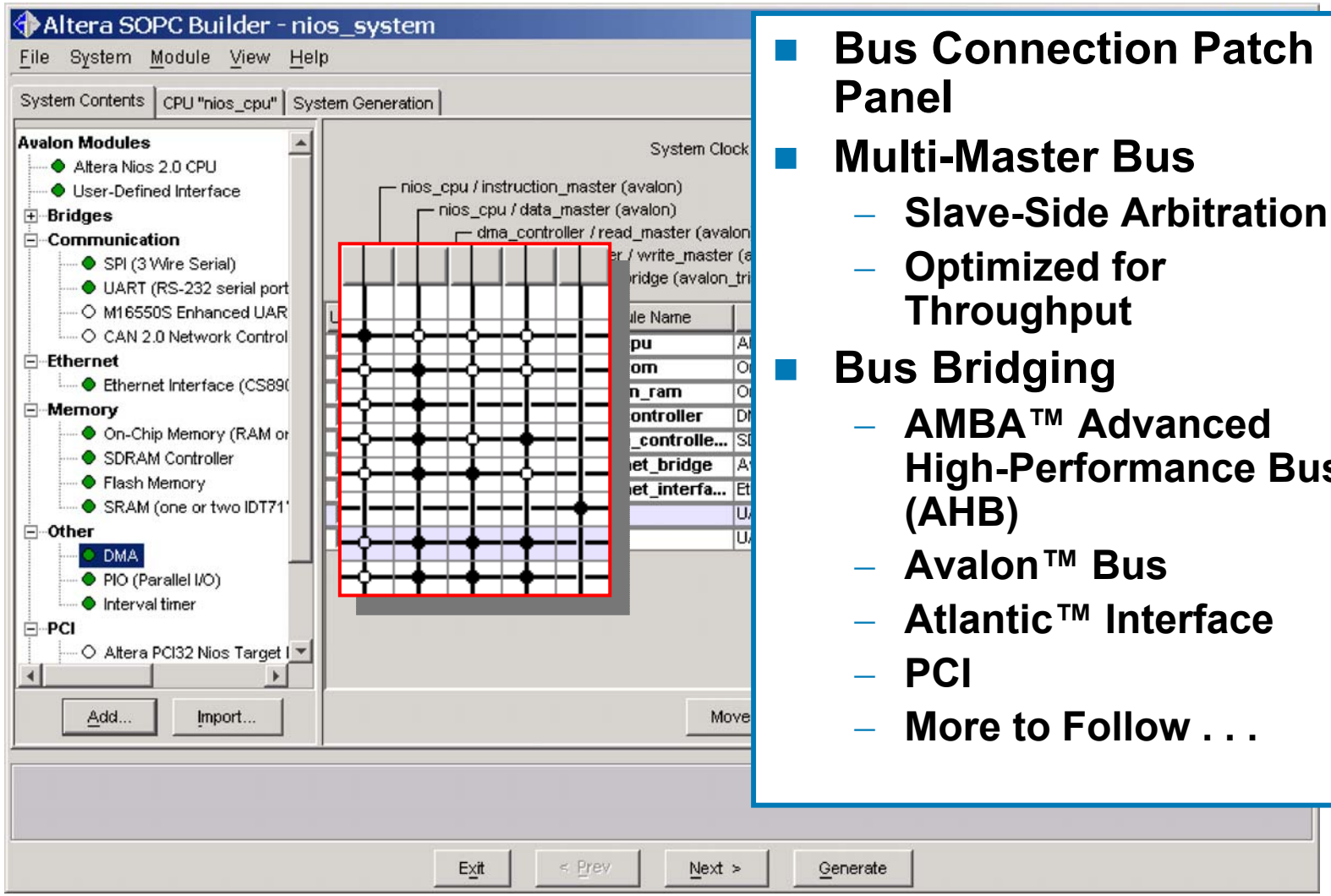
- Pool of "SOPC Builder Ready" Components
  - Communications
  - DSP
  - Bus Interfaces
  - Bridges
  - Processors
- Multiple Processors
- Web-Based IP Deployment

Customization - The Way You Want It

- Table of Active Components
- Configure Each Component
  - Interrupt Request (IRQ)
  - Base Address
  - Hardware Parameters
  - Software Parameters
- Wizard-Based Configuration



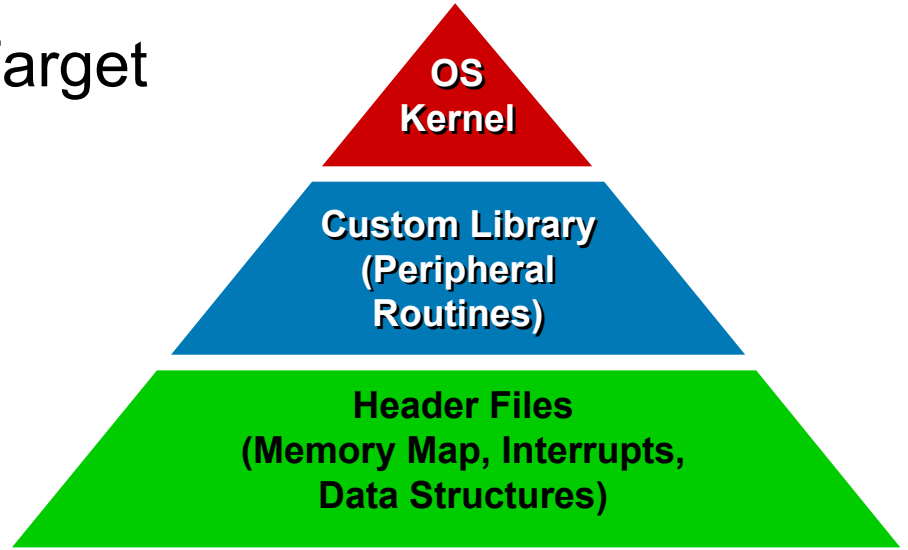
Integration



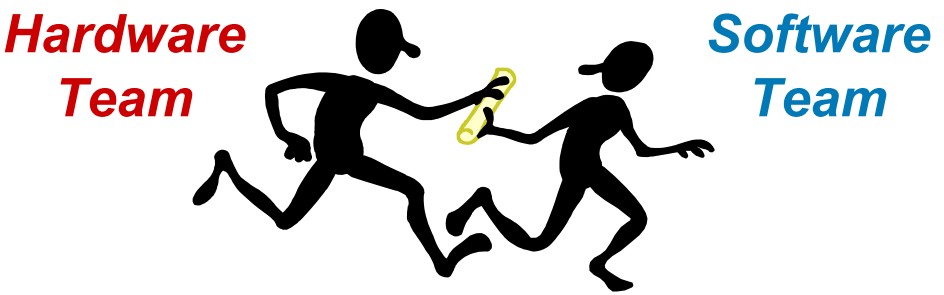
- **Bus Connection Patch Panel**
- **Multi-Master Bus**
  - **Slave-Side Arbitration**
  - **Optimized for Throughput**
- **Bus Bridging**
  - **AMBA™ Advanced High-Performance Bus (AHB)**
  - **Avalon™ Bus**
  - **Atlantic™ Interface**
  - **PCI**
  - **More to Follow . . .**

Automatic Software Generation

- Software Matches Target Hardware

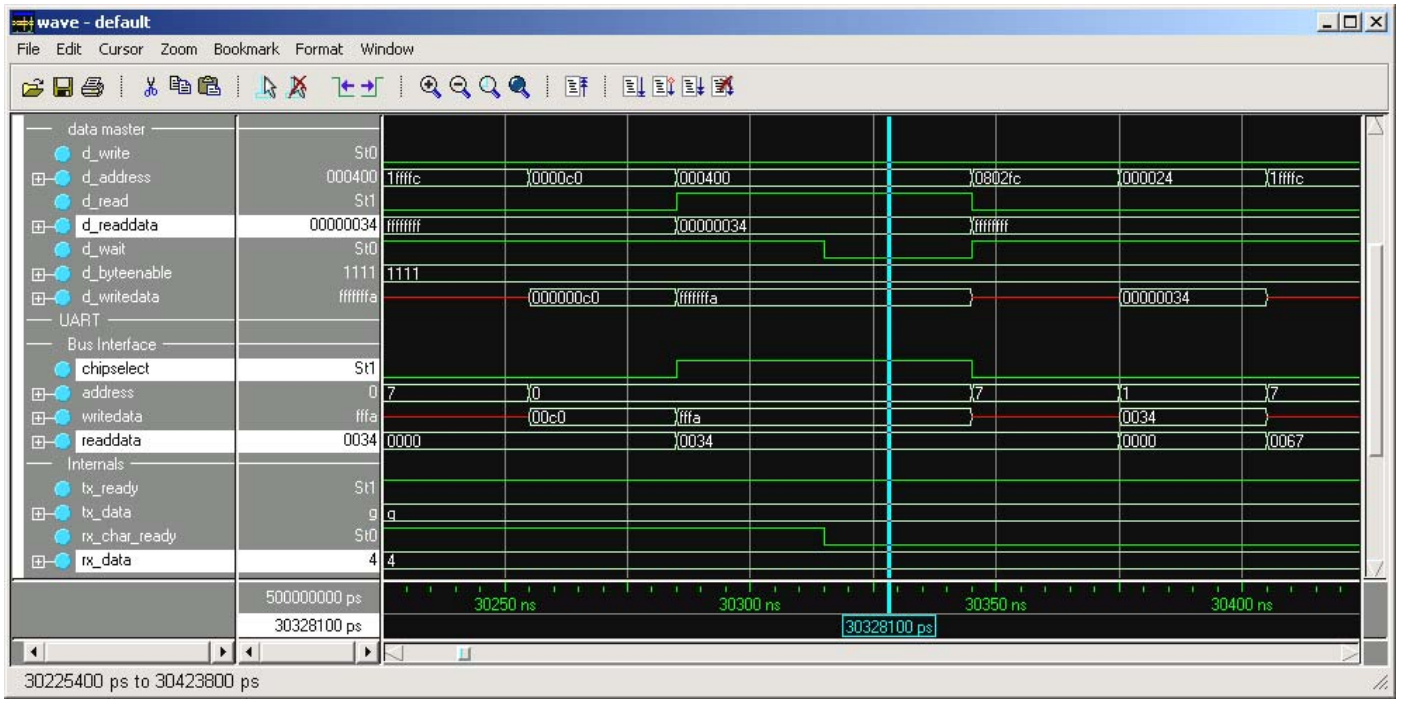


- Promotes Design Coherency (Hardware & Software)
  - Hardware Changes Do Not “Break” the Software



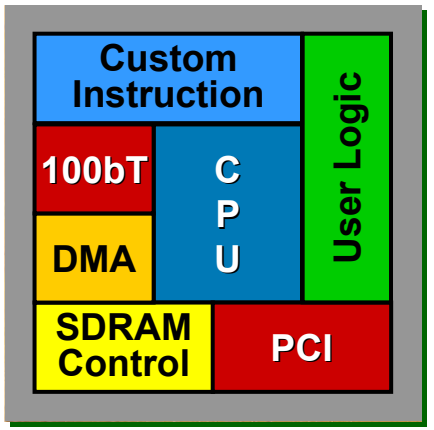
System Verification

- Automated Testbench Generation
  - Complete System Simulation Model
  - Testbench
- Immediate Simulation of Hardware & Software



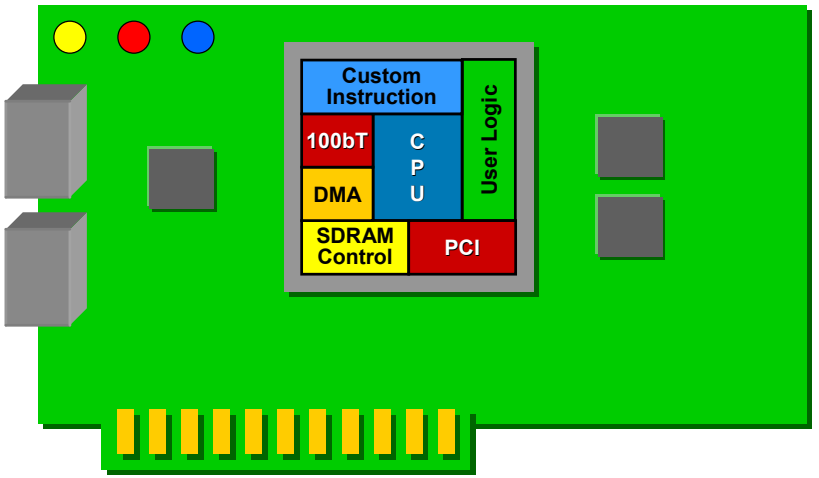
Rapid Prototype in PLD

Incremental Embedded System Design



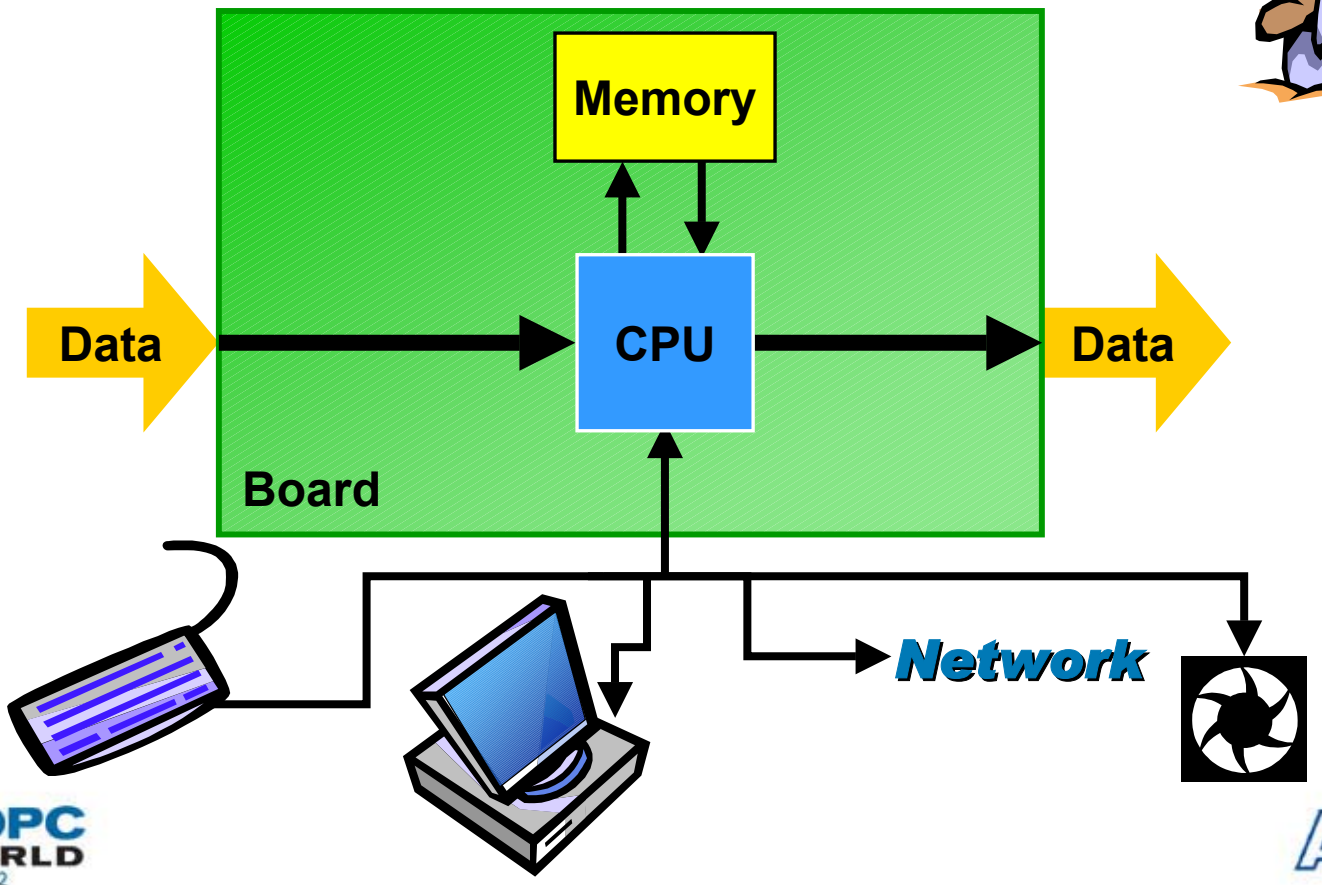
Rapid Prototype in PLD

- Incremental Embedded System Design
- Rapid Prototype in PLD
  - At Full Speed, In Real Hardware
  - Real World Stimulus



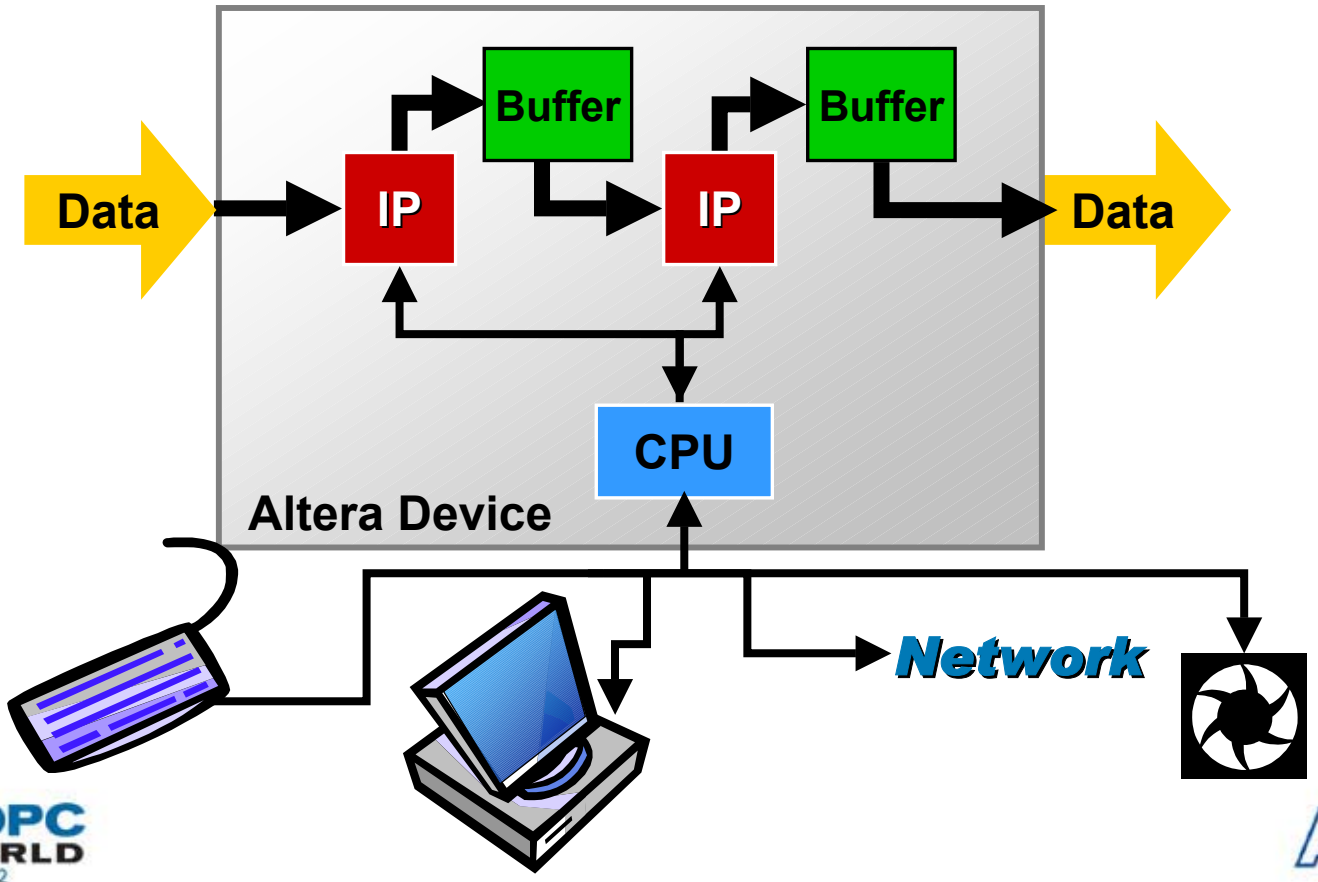
Board-Level Strategy

- **Processor Performs**
  - Data Processing / Data Flow (Heavy Lifting)
  - Control (Housekeeping)



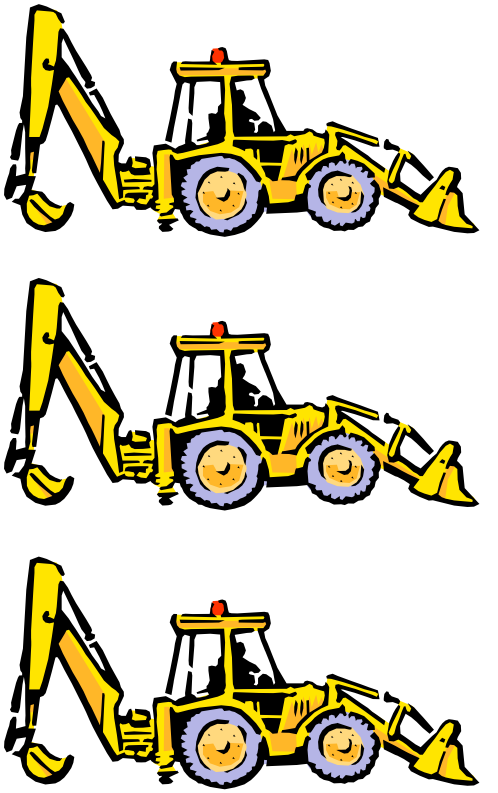
SOPC Strategy

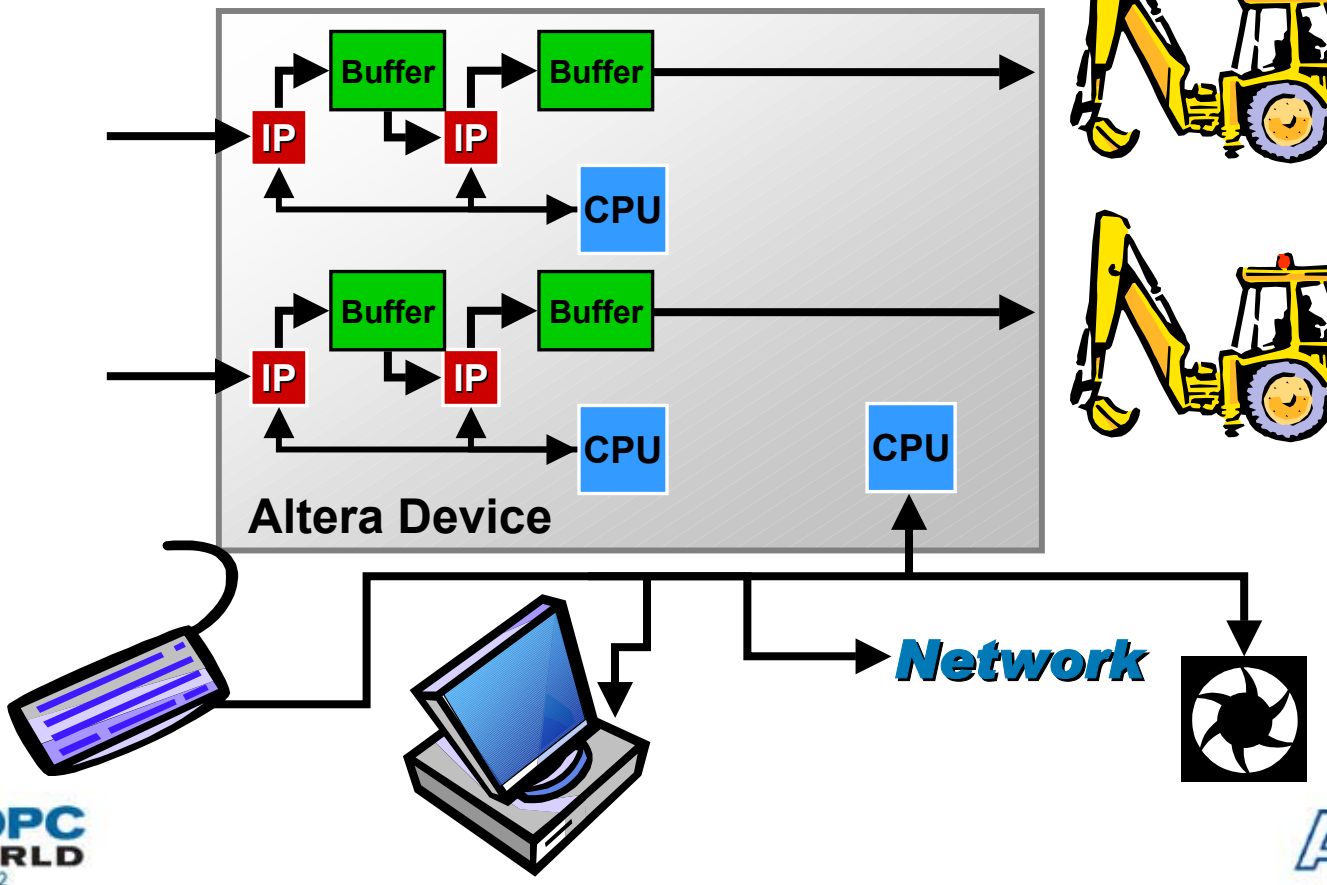
- **Performance-Optimized Systems**
  - IP Handles Data Flow (Heavy Lifting)
  - Processor Provides Control (Housekeeping)



SOPC Strategy

- **Performance-Optimized Systems**
  - Extensible Design



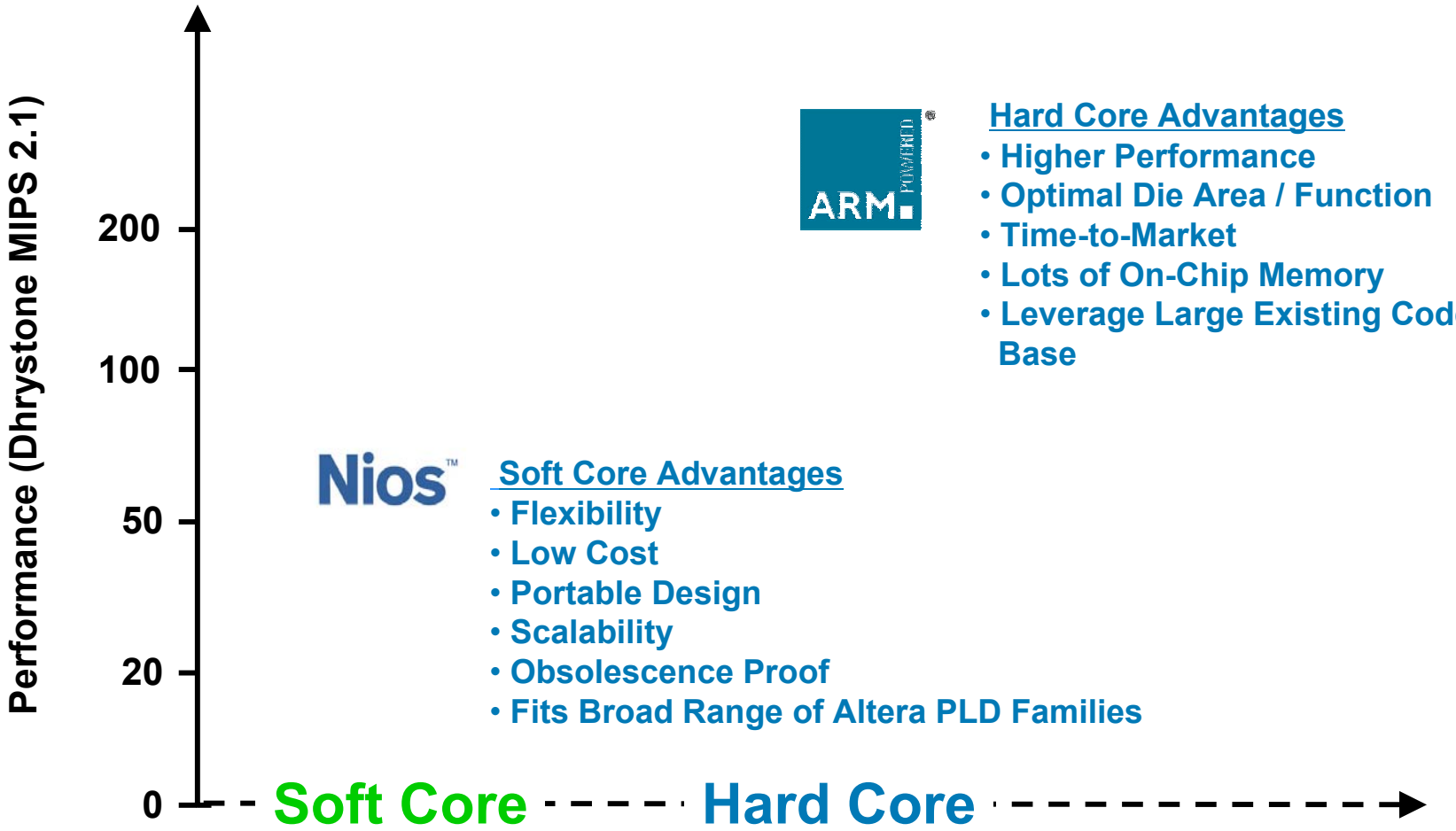


SOPC Builder Ready Components

ARM922T™ Processor	DMA	USB 1.1	SDRAM
Nios™ Embedded Processor	PCI	USB 2.0	SSRAM
ARM®-to-Nios Bridge (AMBA AHB-to-Avalon)	GPIO	SPI	SRAM
Interface to User Logic	Timer	CAN 2.0	FLASH
10/100 Ethernet	Watchdog	16550S UART	On-Chip ROM On-Chip RAM

The List Keeps Growing . . .

Excalibur Embedded Processor Cores



ARM. POWERED

Hard Core Advantages

- Higher Performance
- Optimal Die Area / Function
- Time-to-Market
- Lots of On-Chip Memory
- Leverage Large Existing Code Base

Nios™

Soft Core Advantages

- Flexibility
- Low Cost
- Portable Design
- Scalability
- Obsolescence Proof
- Fits Broad Range of Altera PLD Families

Nios Embedded Processor

- Configurable Soft Core Embedded Processor
- Optimized for Altera® Programmable Logic Device (PLD) Architecture
- 32-Bit RISC Architecture
- License & Royalty Free
- Over 3,300 Kits Sold

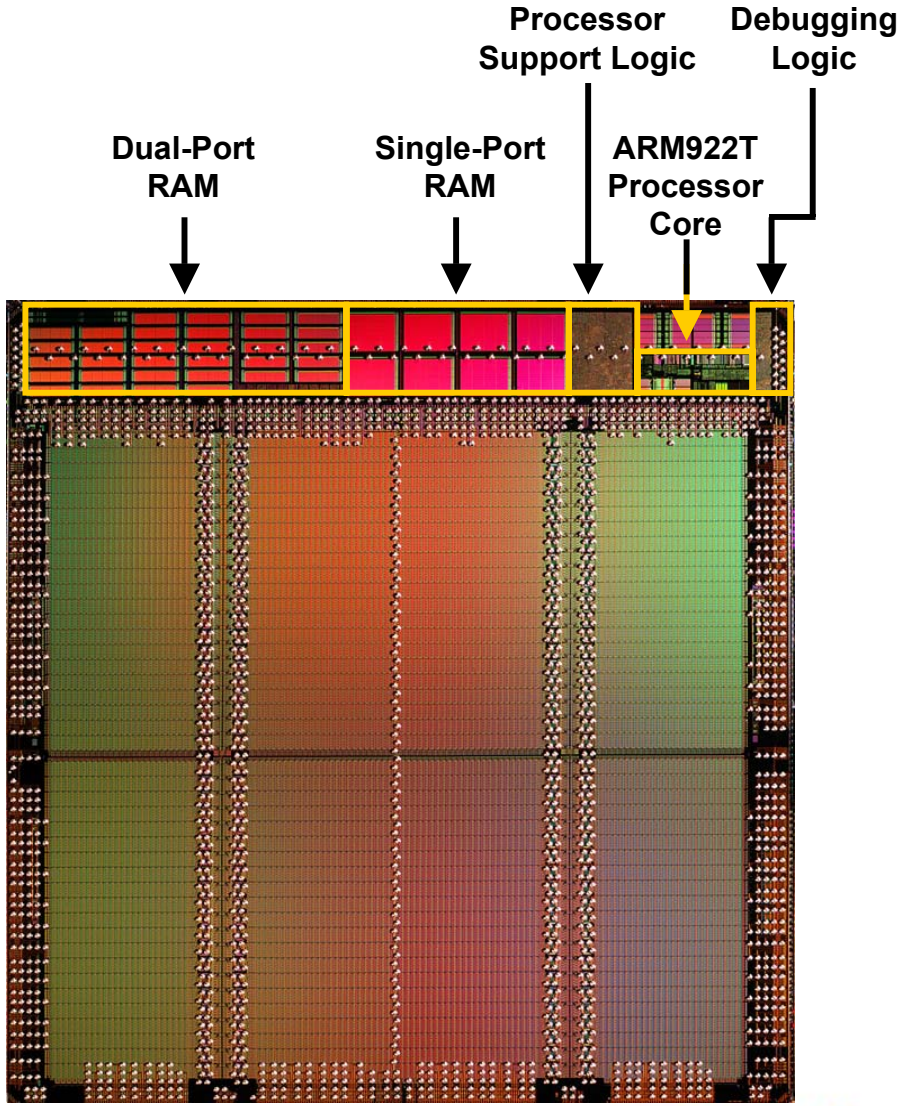
Nios Processor Supports All Device Families

Device Family	Features
Stratix™	Highest Speed (0.13-µm, All-Layer Copper) DSP Blocks Very High Speed I/O Very High Density
Mercury™	Very High-Speed I/O with Clock-Data Recovery (CDR) Medium Density
ARM®-Based Excalibur	High Speed Multi-Processor Systems (ARM + Nios) Medium-to-High Density
APEX™ II	High-Speed Differential I/O Very High Density
APEX 20KE APEX 20KC	High-Speed Differential I/O Low-to-High Density
FLEX® 10K	Low Cost Low-to-Medium Density
ACEX® 1K	Low Cost Low Density

ARM-Based Excalibur Device

- ARM922T Stripe
  - Hard Logic
- Programmable Logic
  - 100K Gates to 1M Gates
- Three Devices in Family

All Available Today



ARM POWERED

SOPC WORLD 2002

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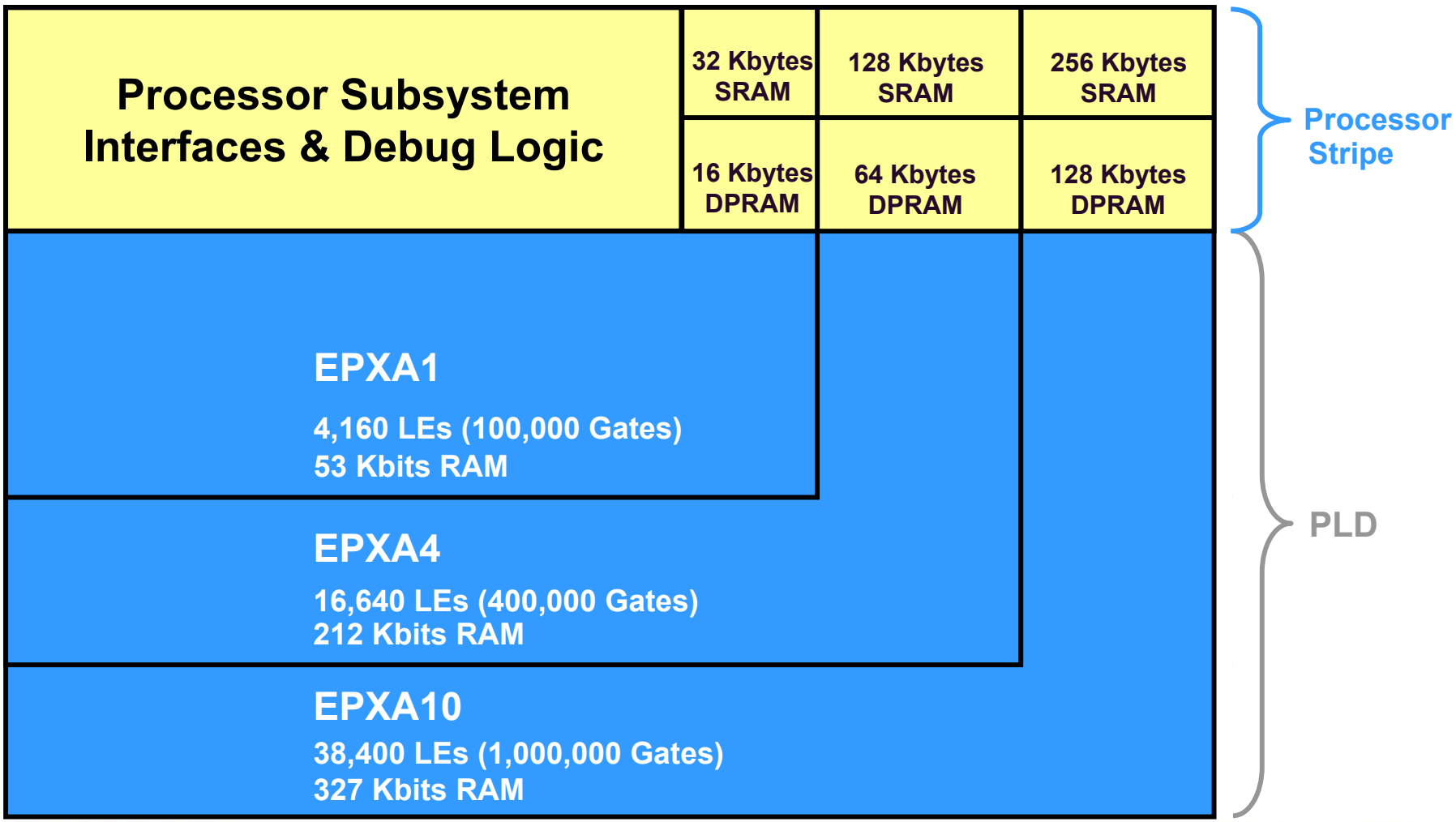
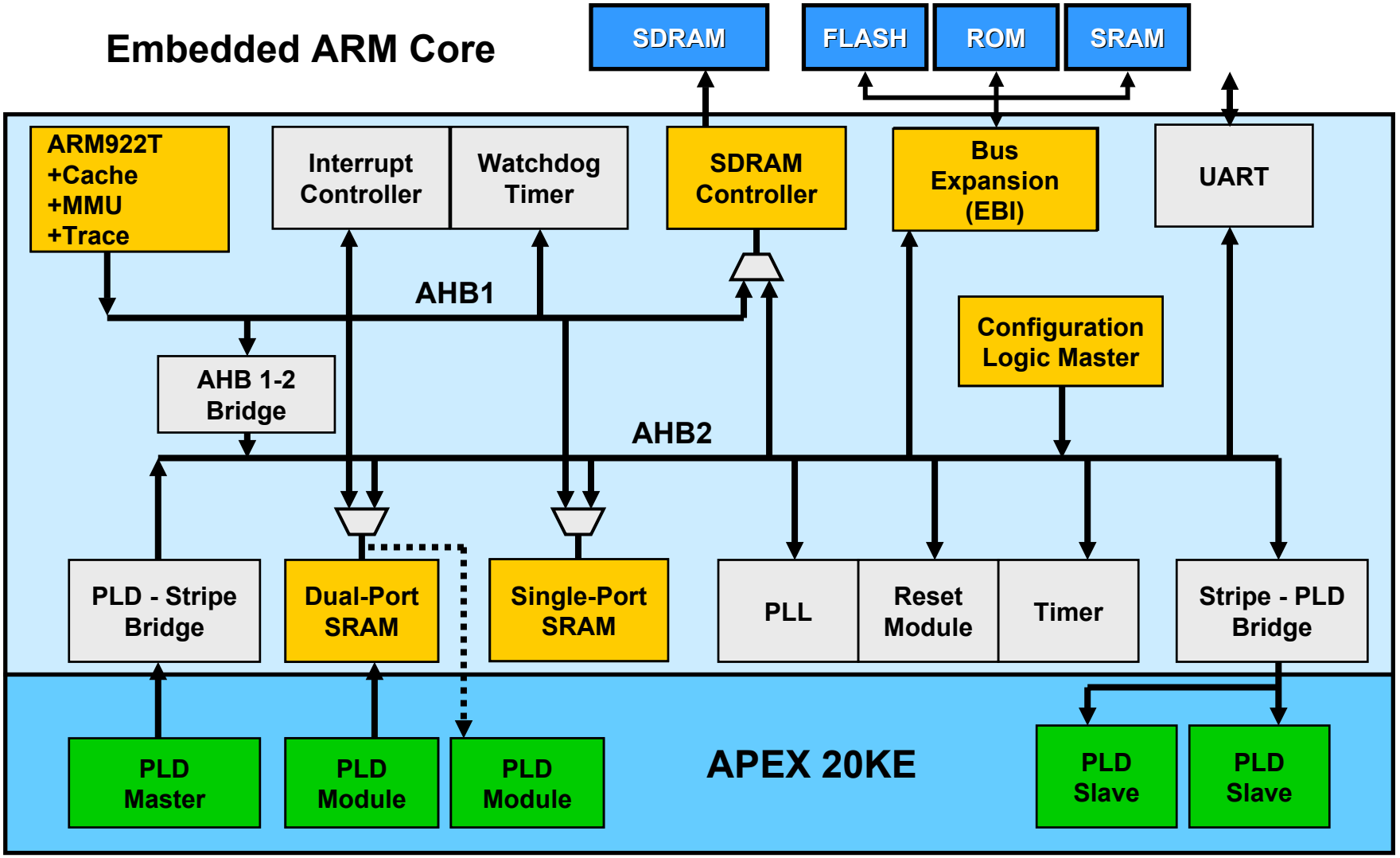
The Altera Excalibur Approach

Industry's First Embedded Processor PLD Solutions

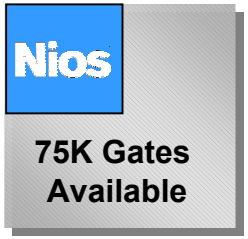


Excalibur Processor Subsystem



Excalibur Flexibility & Scalability

Low-Cost Embedded Processor

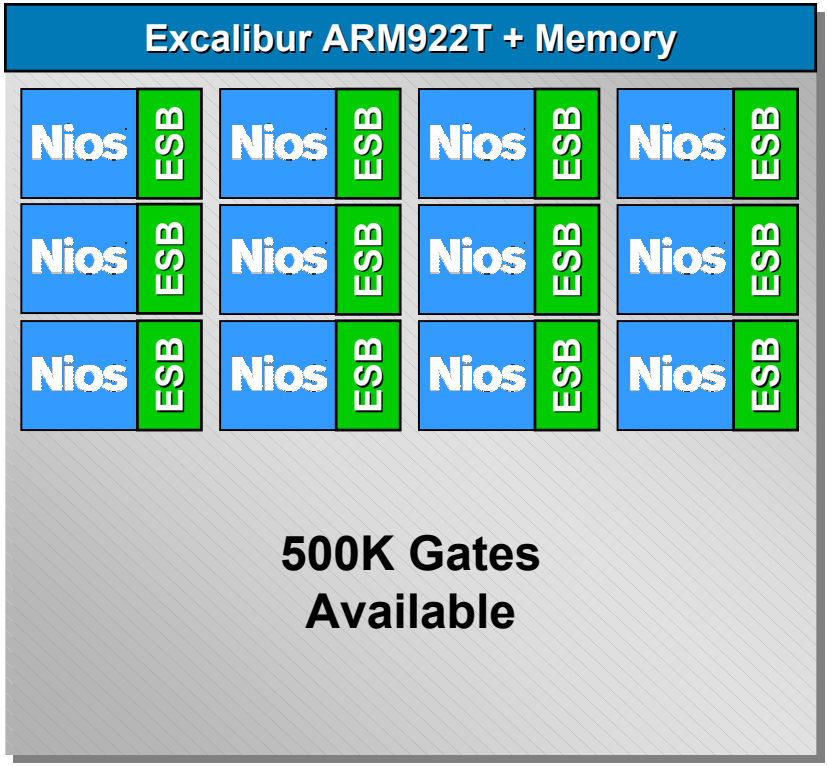


ACEX™ EP1K100 Device

High-Performance Custom DSP

APEX EP20K200E Device

Network Processor System

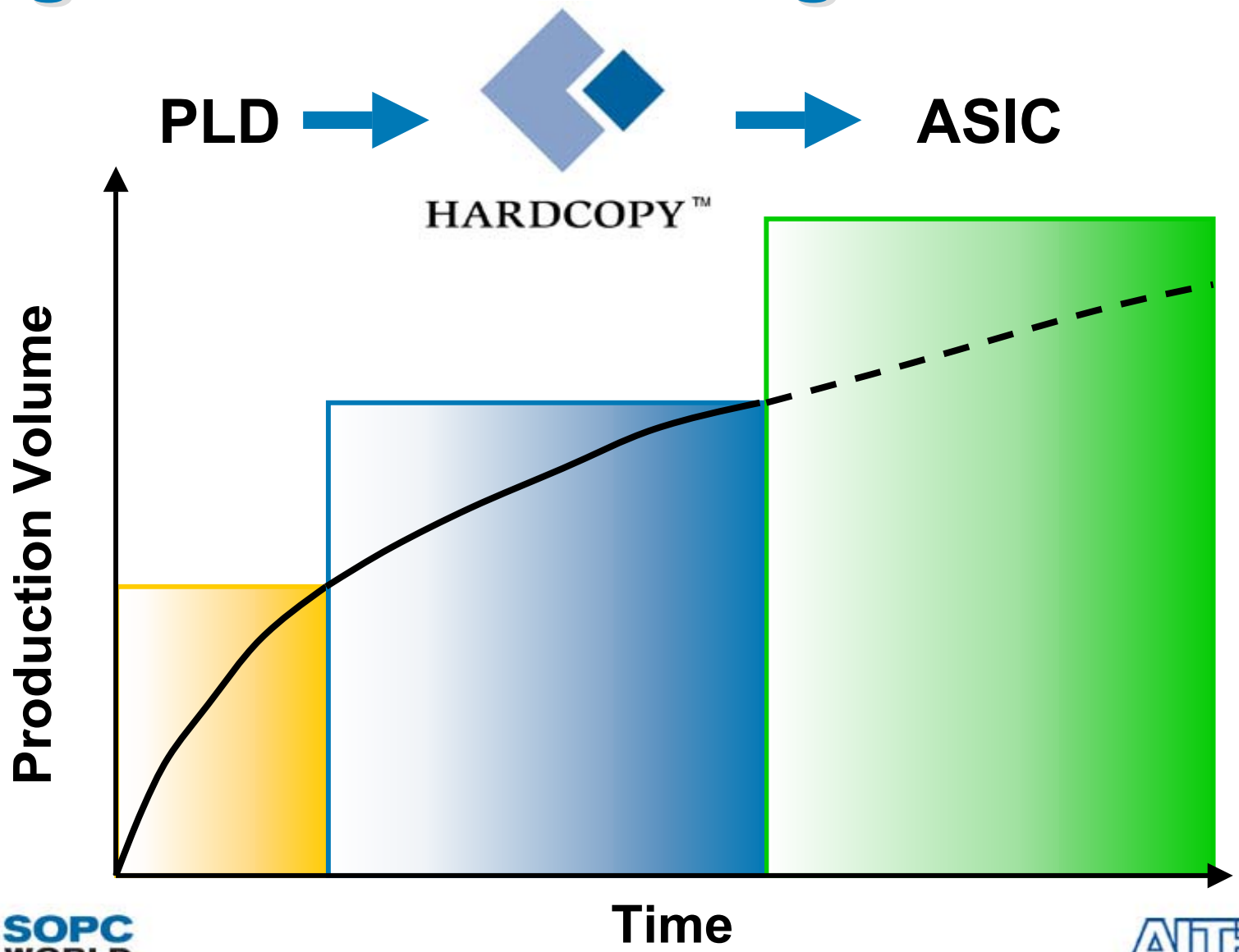


Excalibur EPXA10 Device

ESB = Memory

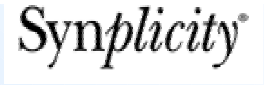
ALTERA

Migration Path for High Volume



Combines Altera Strengths

- High-Density, High-Performance Devices
  - Stratix
  - APEX II
  - Mercury
  - ARM-Based Excalibur

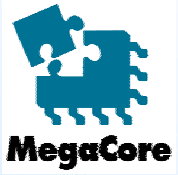


- Hardware Development Tools
  - Quartus® II
  - LeonardoSpectrum™
  - ModelSim®
  - Development Boards

SOPC Builder

- Software Development Tools
  - Compiler
  - Debugger
  - RTOS

- Robust IP Offerings
  - Processor
  - DSP
  - Communication
- Bus Interface



SOPC Builder Benefits

- Custom-Fit SOC Solution
- Huge Reduction in Time-to-Market
- Low-Risk, Low-Cost Development
- Complete Solution
- Powerful & Flexible Processor Solutions
- Makes SOC Available to Everyone

SOPC Builder Accelerates Design from Concept to System in Minutes

SOPC Builder Design Flow