20 YEARS *of*

ALTERA®

INNOVATION

# SOPC WORLD 2003

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# Stratix HardCopy Design Flow With Quartus-II Ver. 3.0

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# Agenda

- HardCopy Stratix Overview
- Quartus II 3.0 Features For HardCopy
  - Compilation And Supported Devices
  - Design Assistant
  - HardCopy Optimization Wizard
  - HardCopy Timing Constraints
  - HardCopy Files Wizard
  - HardCopy Power Estimation
- Designing For HardCopy
  - Clock
  - Reset
  - Timing Closure
  - Non-synchronous Design Structure

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# HardCopy Stratix Overview

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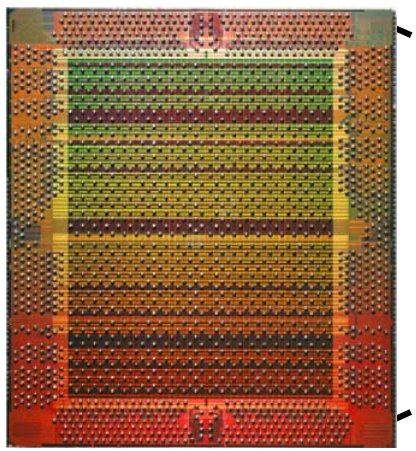
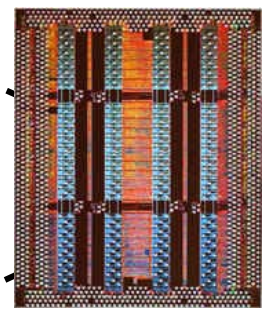
# Stratix HardCopy Value Proposition

- Industry's Only Complete Solution from Prototype to Production
  - Benefits of Designing with FPGAs
  - Seamless Migration from Proven FPGA Design to Custom Design
  - Unified & Complete Design Methodology with Single Design Tool
- Single Source for Devices, Tools & Intellectual Property (IP)



FPGA Die



HardCopy Die

***Seamless Migration***
***Simplified Technology***
***~70% Die Size Reduction***
***~1/5th ASIC Development Time***

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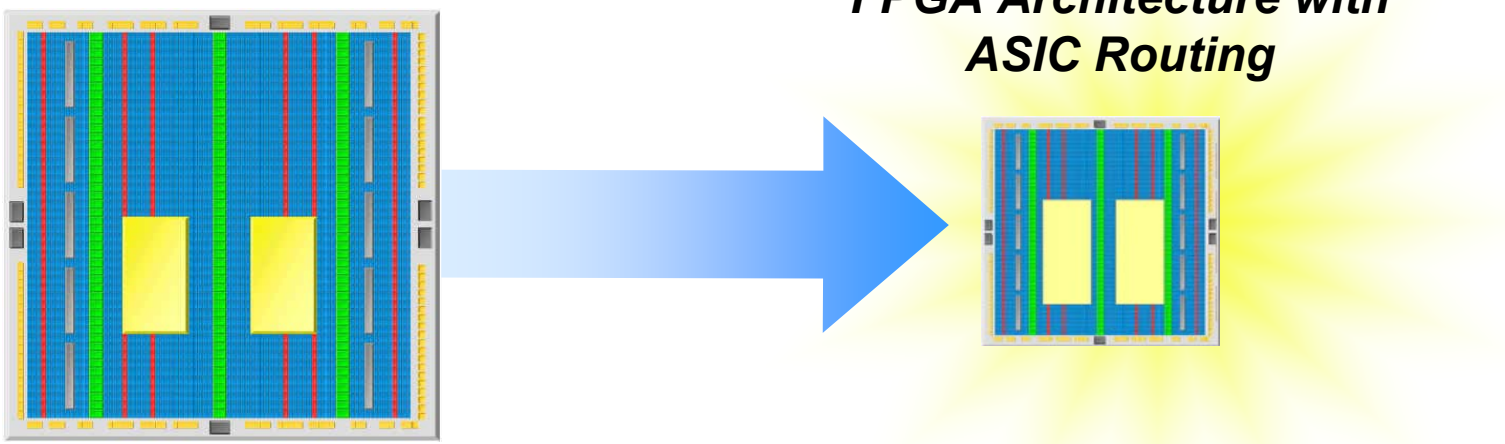
# FPGA to HardCopy Device

- Remove Configuration Circuitry
- Remove Programmable Routing
- Remove Programmability for Logic & Memory
- Add Embedded Testability
- Customize with Two Metal Layers




**Stratix™ EP1S25**

**HardCopy HC1S25**

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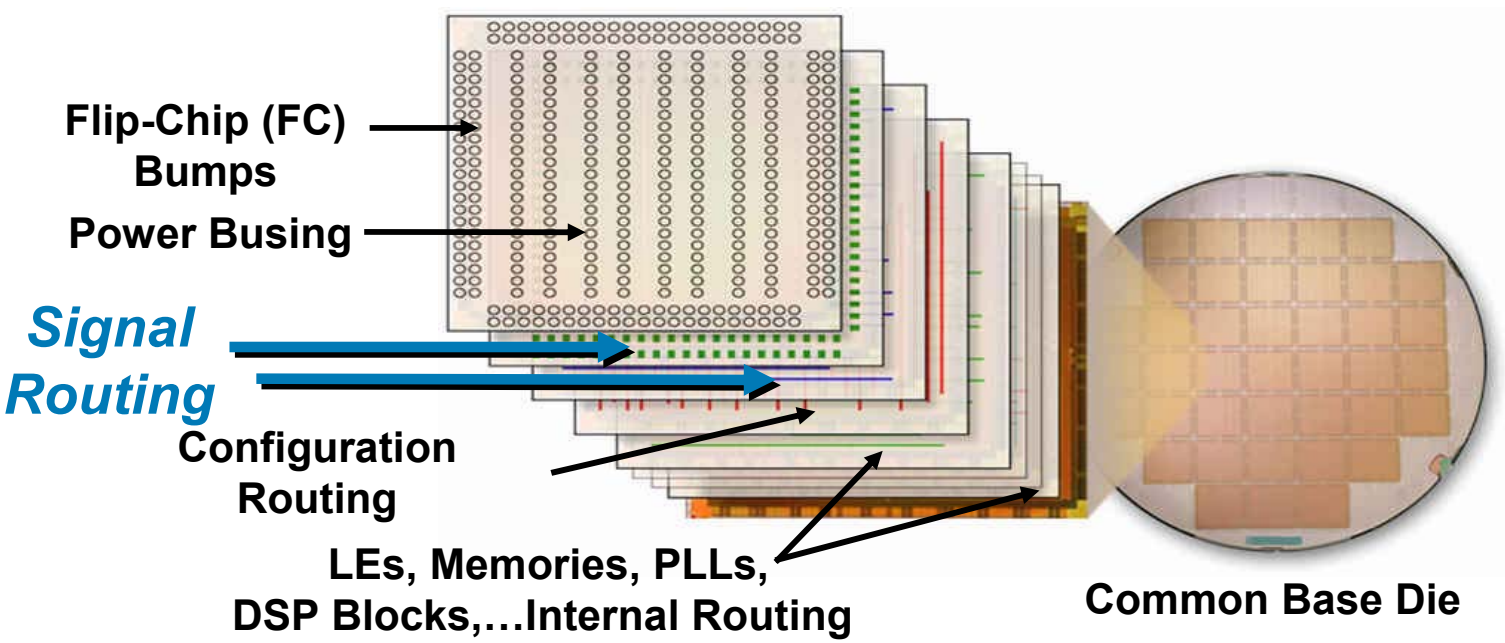
# HardCopy Silicon Technology

- Same Process Technology as FPGA
- Common Base Die
- Eight Metal Layers in HardCopy Stratix Devices
  - Two for Customer Design

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# Verification

- Timing Verification
  - Industry-Standard Tools
    - Synopsys PrimeTime Tool
- Structural Verification
  - Boundary Scan, BIST
  - Automatic Test Pattern Generation (ATPG)
    - No Need for Functional Vectors from Customer
    - Ensures High-Fault Coverage, ~99%
- Altera Delivers Tested Devices

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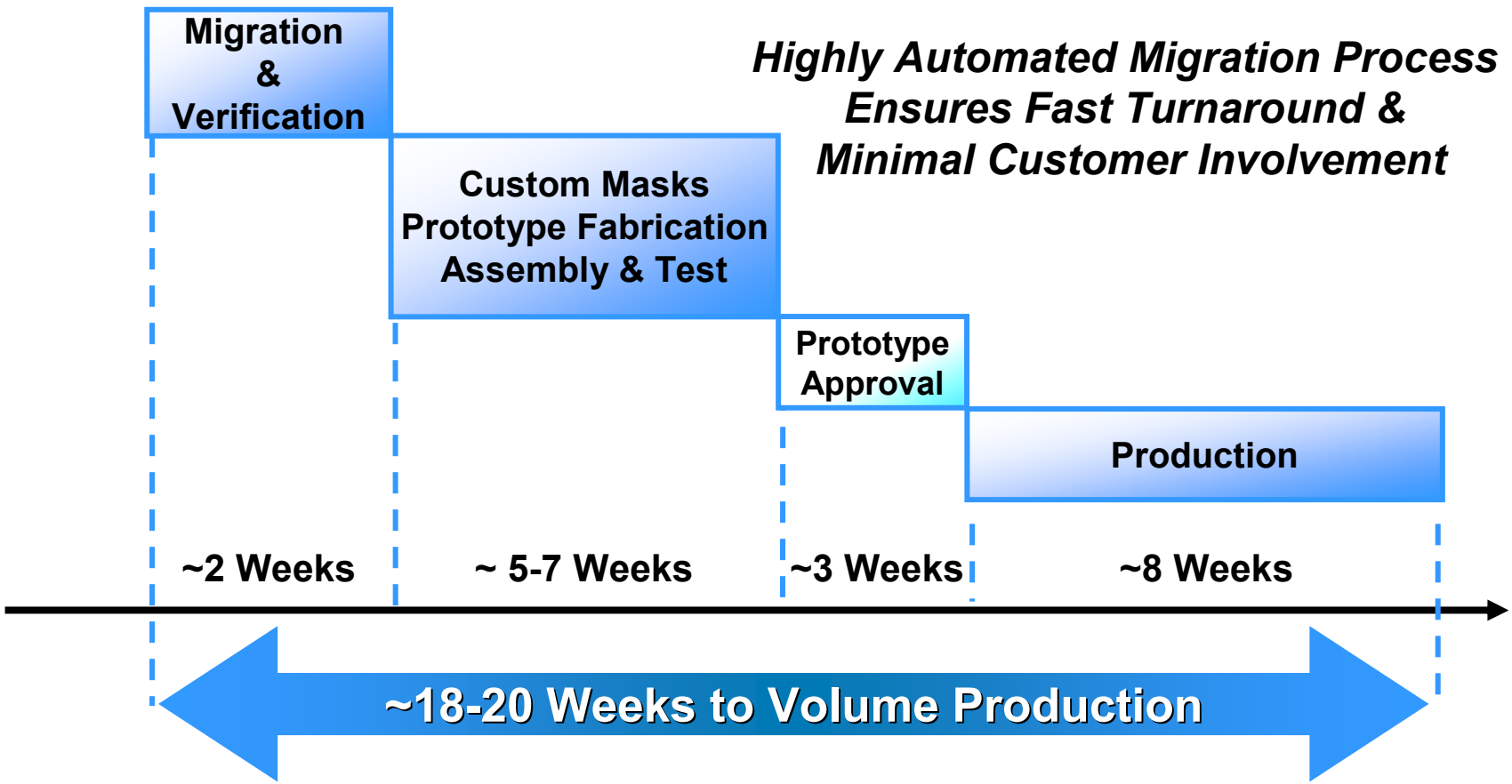
# Implementation Timeline

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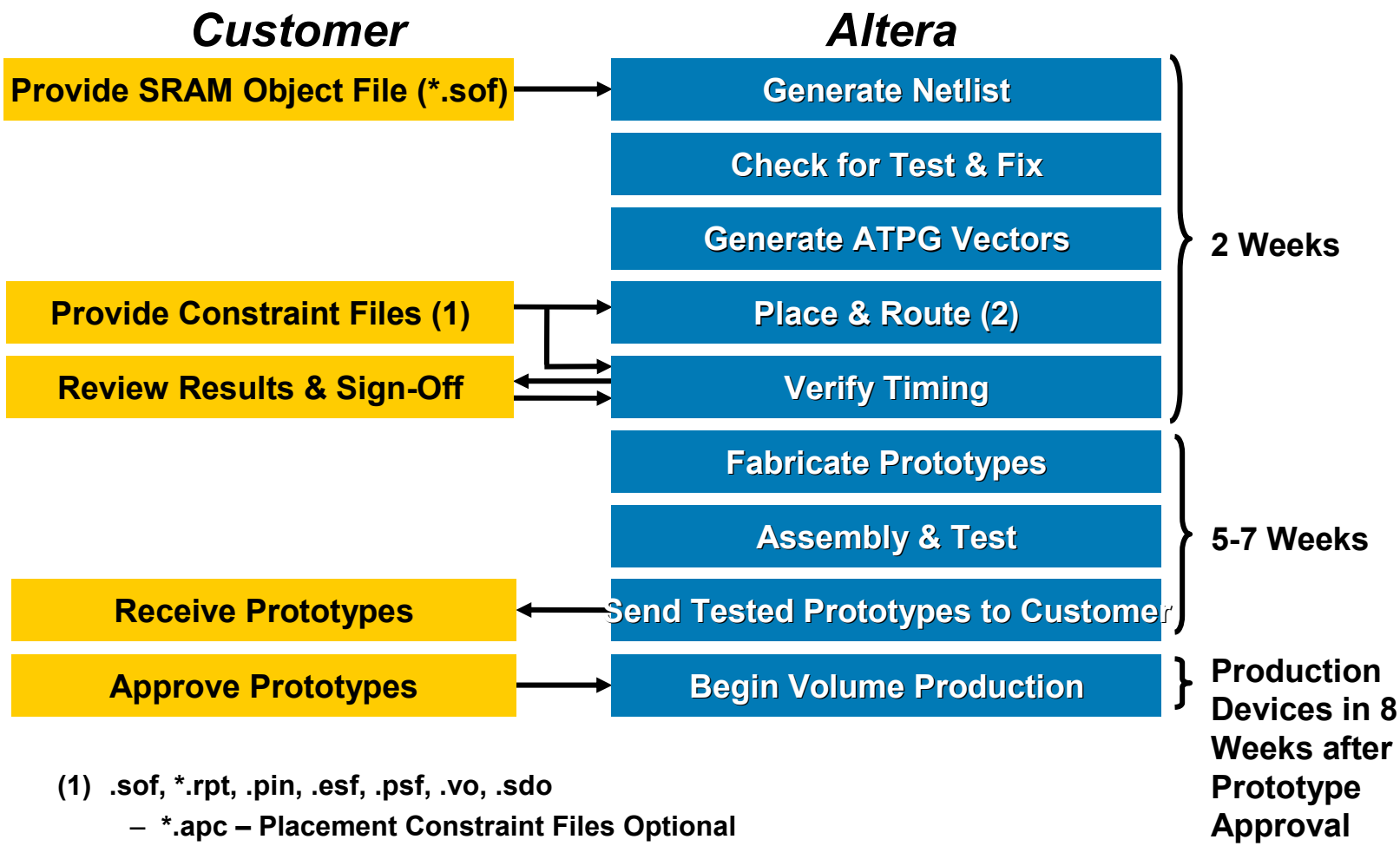
# Migration Flow




(1) .sof, *.rpt, .pin, .esf, .psf, .vo, .sdo
  – *.apc – Placement Constraint Files Optional
(2) Altera Will Use *.apc if Provided & Only Route Design

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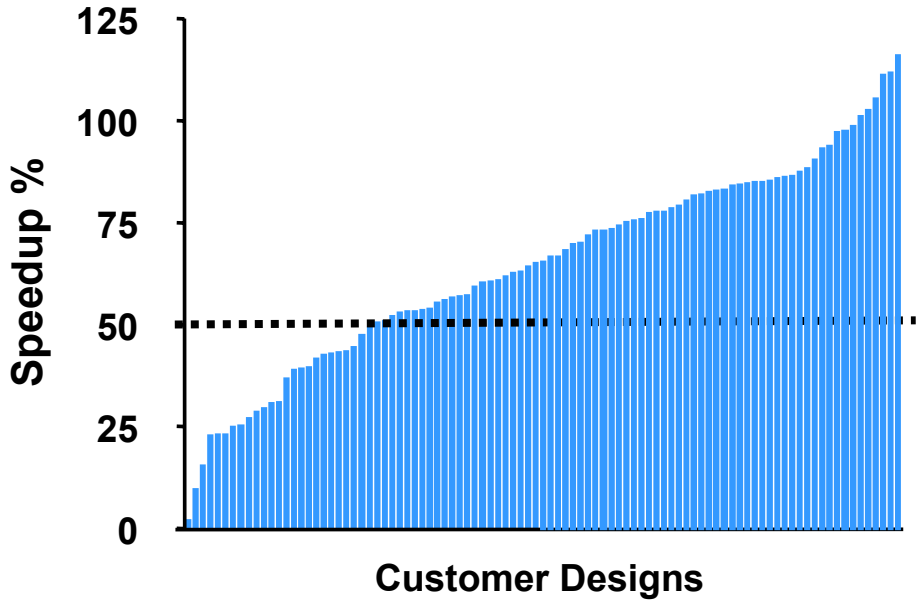
# HardCopy Device Performance

- Smaller Die
- Routing Benefits
- Reduced Internal Delays
- I/O Speed Unchanged
- $f_{MAX}$ Change Is Design-Dependent
- Performance Estimation through Quartus® II Software




***On the Average, 50% Performance-Improvement over FPGA***

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# Power Benefits

- ~40% Lower Power Consumption than FPGA
  - I/O Power Remains Unchanged
  - Power Estimation Tool Supported by Quartus II Design Software
    - Also Available on Altera Web Site

# HardCopy Vs. ASIC Devices

| Category | HardCopy | ASIC |
|---|---|---|
| Design Time | 2-3 Weeks | Months |
| Design Effort | Minimal | Significant |
| Investment in Tools | None | Significant |
| Staff Needed | None | Significant |
| Package Design Effort | None | Yes |
| Board Re-Design | No | Yes |
| Fabrication & Assembly Cycle Time | 7 Weeks | 12 Weeks |
| Non-Recurring Engineering (NRE) Cost | Low | High |
| Price per Part | Low | Lowest |
| Time to Volume | Weeks | Months |

***HardCopy Process Leverages***
***the Benefits of FPGA Design & Engineering***

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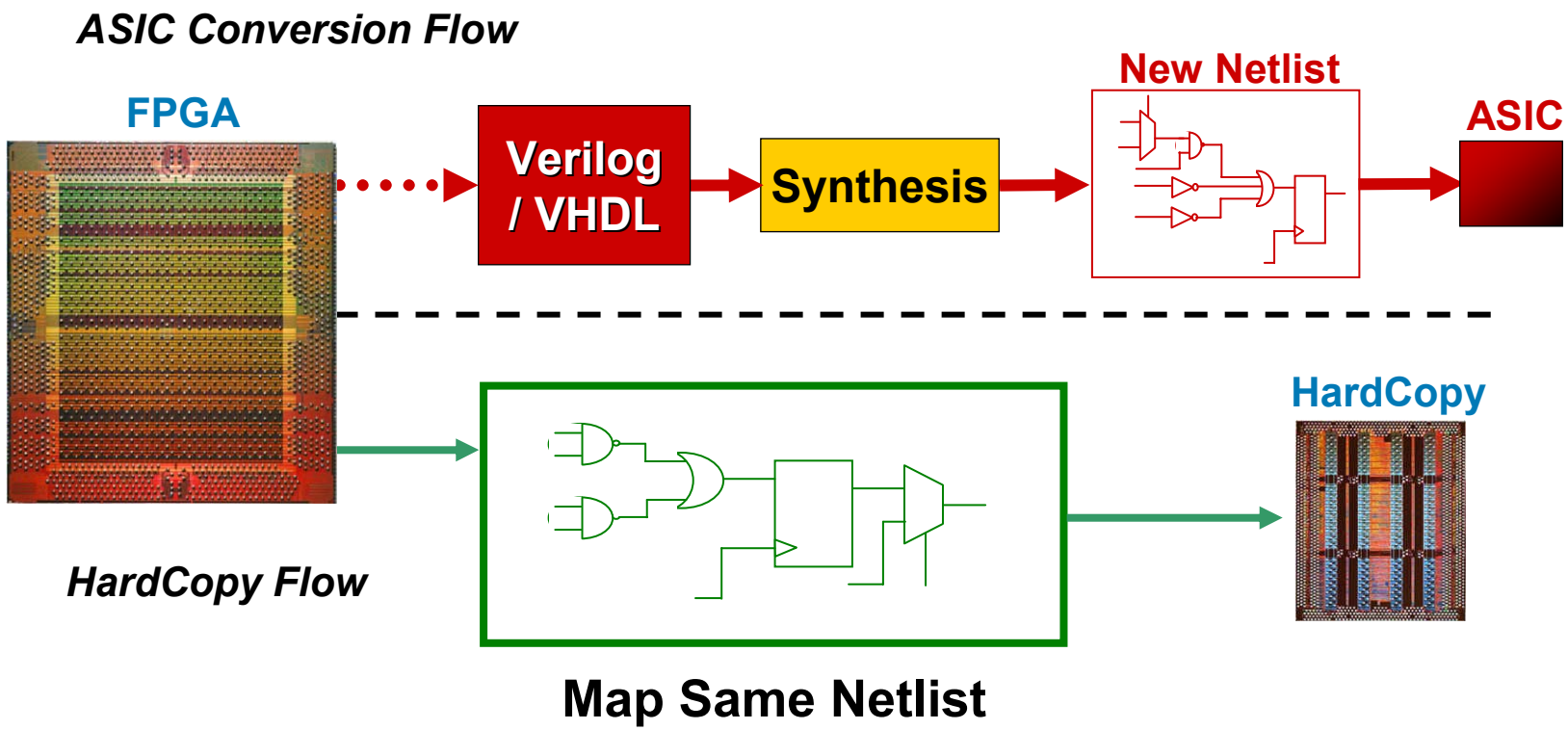
# HardCopy Vs. ASIC Conversion Flow

## *ASIC Conversion Generates New Netlist*
## *Design Needs Validation & Adjustment*

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# HardCopy Migration Is Not ASIC Conversion

| Altera FPGA | HardCopy | ASIC |
|---|---|---|
| Logic Elements | Same as FPGA | Re-Synthesis to Gates |
| Memory Blocks | Same as FPGA | Compiled/ Cell Based |
| I/O Pins | Same as FPGA | Different I/O Library |
| Phase-Locked Loops (PLLs) | Same as FPGA | Different Design |
| Intellectual Property | Same as FPGA | Re-Qualification & License |
| Packaging | Same as FPGA | Custom |
| Process Geometry | Same as FPGA | Same/Different/Hybrid |
| Foundry | Same as FPGA | Same/Different |
| Interconnect Routing | Similar SOG* of Standard Cell ASIC Routing | |

* SOG – Sea of Gates

***ASIC Conversion Requires Starting Over***

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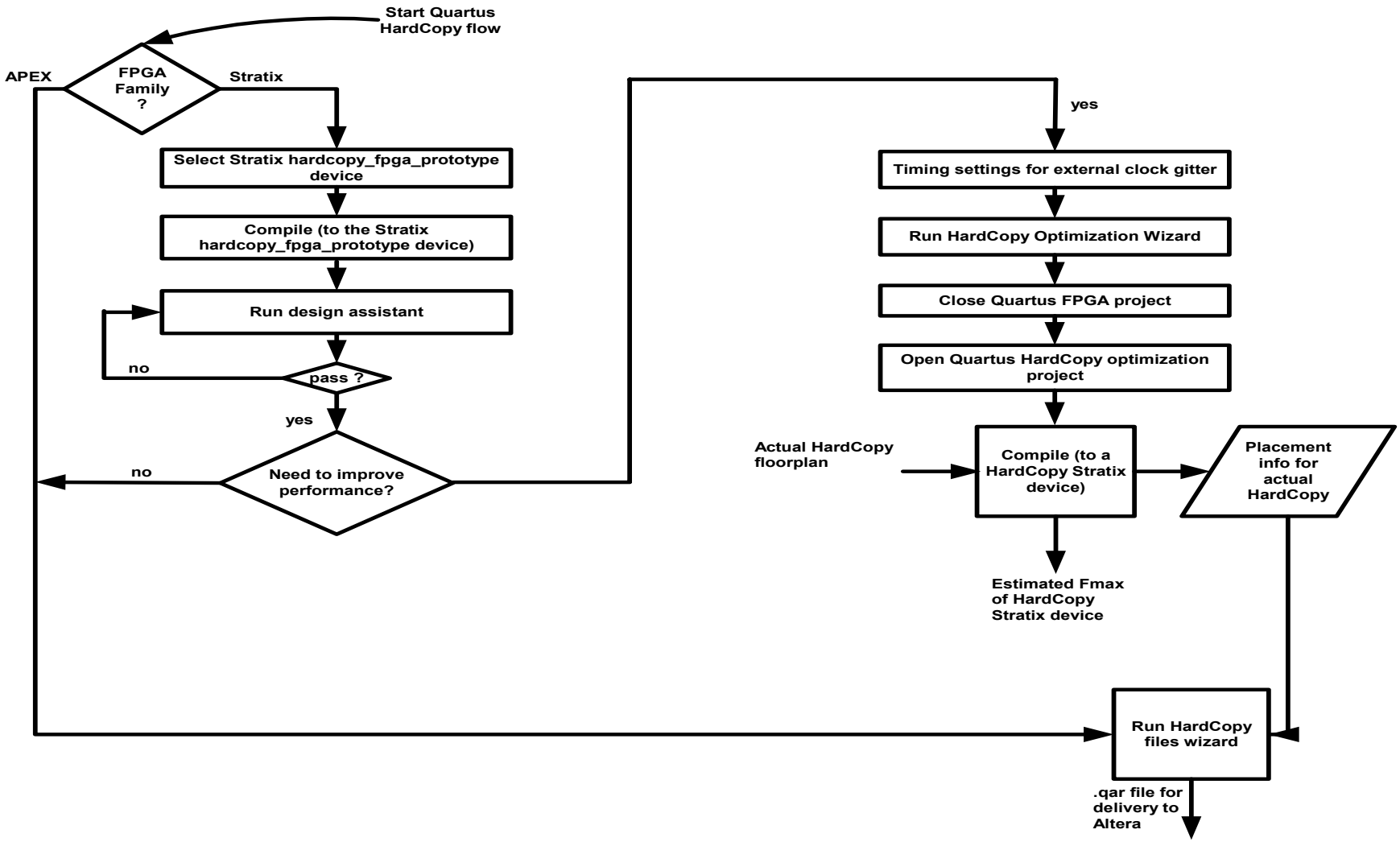
# Quartus II 3.0 Features For HardCopy

# HardCopy Process Flow

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# HARDCOPY_FPGA_PROTOTYPE Devices

- Part Of The Stratix Family
- Is A **Virtual** FPGA Device To Guide Quartus II
  - Has Reduced Feature Set From Its Equivalent FPGA
    - Less MRAMs As An Example
  - Has An Identical Timing Model As The FPGA
  - Has The Identical Floorplan Of The FPGA
- Is Not The Actual Hardcopy Device
  - Does Not Match The Floorplan Of The Hardcopy Device
  - Matches The Pin-out Of The Equivalent Hardcopy Device
- Always Has Equivalent Real FPGA
  - This Is NOT A New Hardware Die

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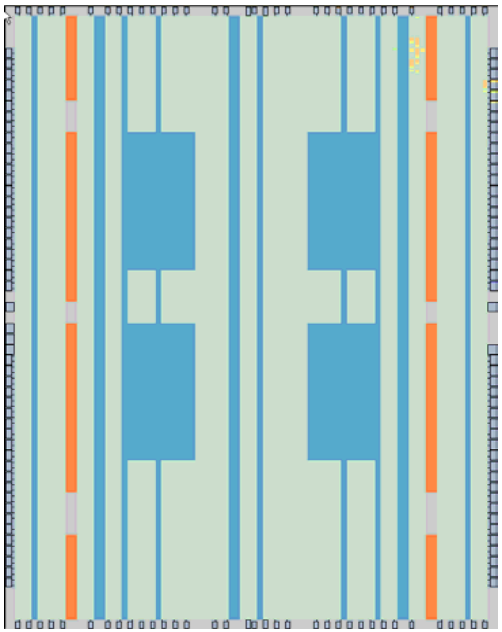
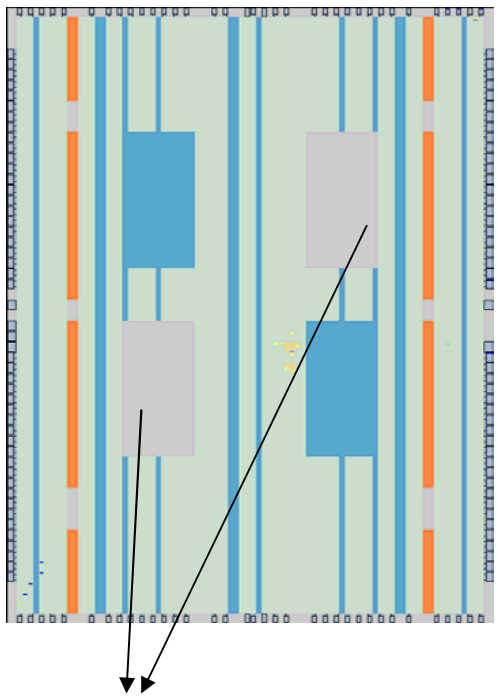
# HARDCOPY_FPGA_PROTOTYPE vs. FPGA vs. HardCopy devices

EP1S30F780C5

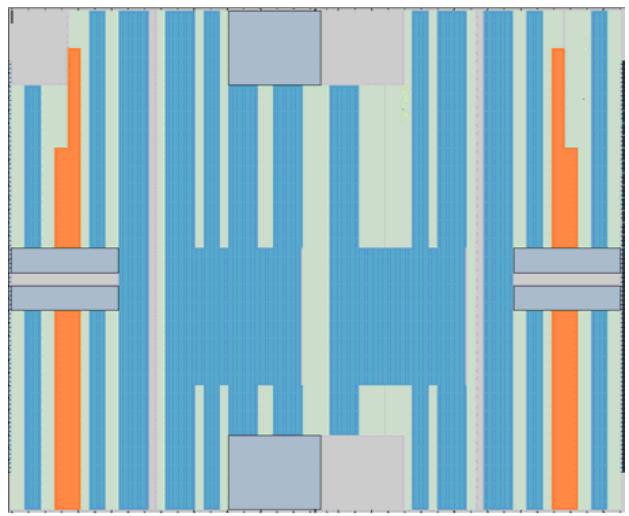


EP1S30F780C5_**HARDCOPY_FPGA_PROTOTYPE**



Blanked out MRAM blocks

HC1S30F780



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# Device Mapping

| Physical FPGA | FPGA Prototype Device for HardCopy | HardCopy Device |
|---|---|---|
| EP1S25F672C6 | EP1S25F672C6_HARDCOPY_FPGA_PROTOTYPE | HC1S25F672 |
| EP1S25F672C7 | EP1S25F672C7_HARDCOPY_FPGA_PROTOTYPE | |
| EP1S30F780C5 | EP1S30F780C5_HARDCOPY_FPGA_PROTOTYPE | HC1S30F780 |
| EP1S30F780C6 | EP1S30F780C6_HARDCOPY_FPGA_PROTOTYPE | |
| EP1S30F780C7 | EP1S30F780C7_HARDCOPY_FPGA_PROTOTYPE | |
| EP1S40F780C5 | EP1S40F780C5_HARDCOPY_FPGA_PROTOTYPE | HC1S40F780 |
| EP1S40F780C6 | EP1S40F780C6_HARDCOPY_FPGA_PROTOTYPE | |
| EP1S40F780C7 | EP1S40F780C7_HARDCOPY_FPGA_PROTOTYPE | |
| EP1S60F1020C6 | EP1S60F1020C6_HARDCOPY_FPGA_PROTOTYPE | HC1S60F1020 |
| EP1S60F1020C7 | EP1S60F1020C7_HARDCOPY_FPGA_PROTOTYPE | |
| EP1S80F1020C6 | EP1S80F1020C6_HARDCOPY_FPGA_PROTOTYPE | HC1S80F1020 |
| EP1S80F1020C7 | EP1S80F1020C7_HARDCOPY_FPGA_PROTOTYPE | |

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# Stratix Supported Devices

*Table 1: Hardcopy Stratix Devices Vs. Equivalent Stratix Devices*

| Device | Resources Compared to Equivalent FPGA | | | | | | |
|---|---|---|---|---|---|---|---|
| | LEs | M512 Blocks | M4K Blocks | M-RAM Blocks | DSP Blocks | PLLS | Max. User I/Os |
| **HC1S25F672** | 25,660 | 224 | 138 | 2 | 10 | 6 | 473 |
| **EP1S25F672** | 25,660 | 224 | 138 | 2 | 10 | 6 | 473 |
| **HC1S30F780** | 32,470 | 295 | 171 | 2 | 12 | 10 | 597 |
| **EP1S30F780** | 32,470 | 295 | 171 | 4 | 12 | 10 | 597 |
| **HC1S40F780** | 41,250 | 384 | 183 | 2 | 14 | 12 | 615 |
| **EP1S40F780** | 41,250 | 384 | 183 | 4 | 14 | 12 | 615 |
| **HC1S60F1020** | 57,120 | 574 | 292 | 6 | 18 | 12 | 773 |
| **EP1S60F1020** | 57,120 | 574 | 292 | 6 | 18 | 12 | 773 |
| **HC1S80F1020** | 79,040 | 767 | 364 | 6 | 22 | 12 | 773 |
| **EP1S80F1020** | 79,040 | 767 | 364 | 9 | 22 | 12 | 773 |

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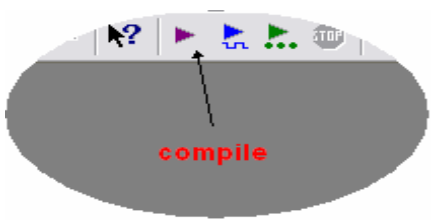
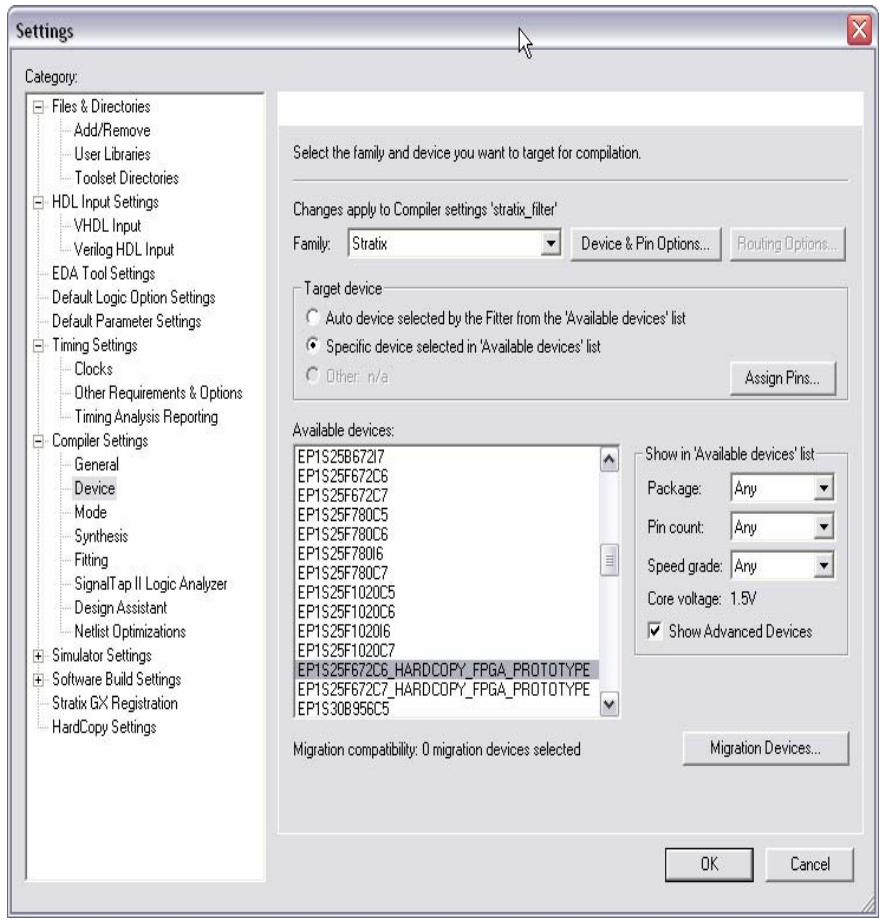
# Compilation

- In An Open Project, Select The Target HardCopy Device Thru The Compiler Setting Option. Make Sure To Select a HARDCOPY_FPGA_PROTOTYPE device
- Assignments -> Device Menu Option Will Bring You To The Settings Window
- Compile Your Design

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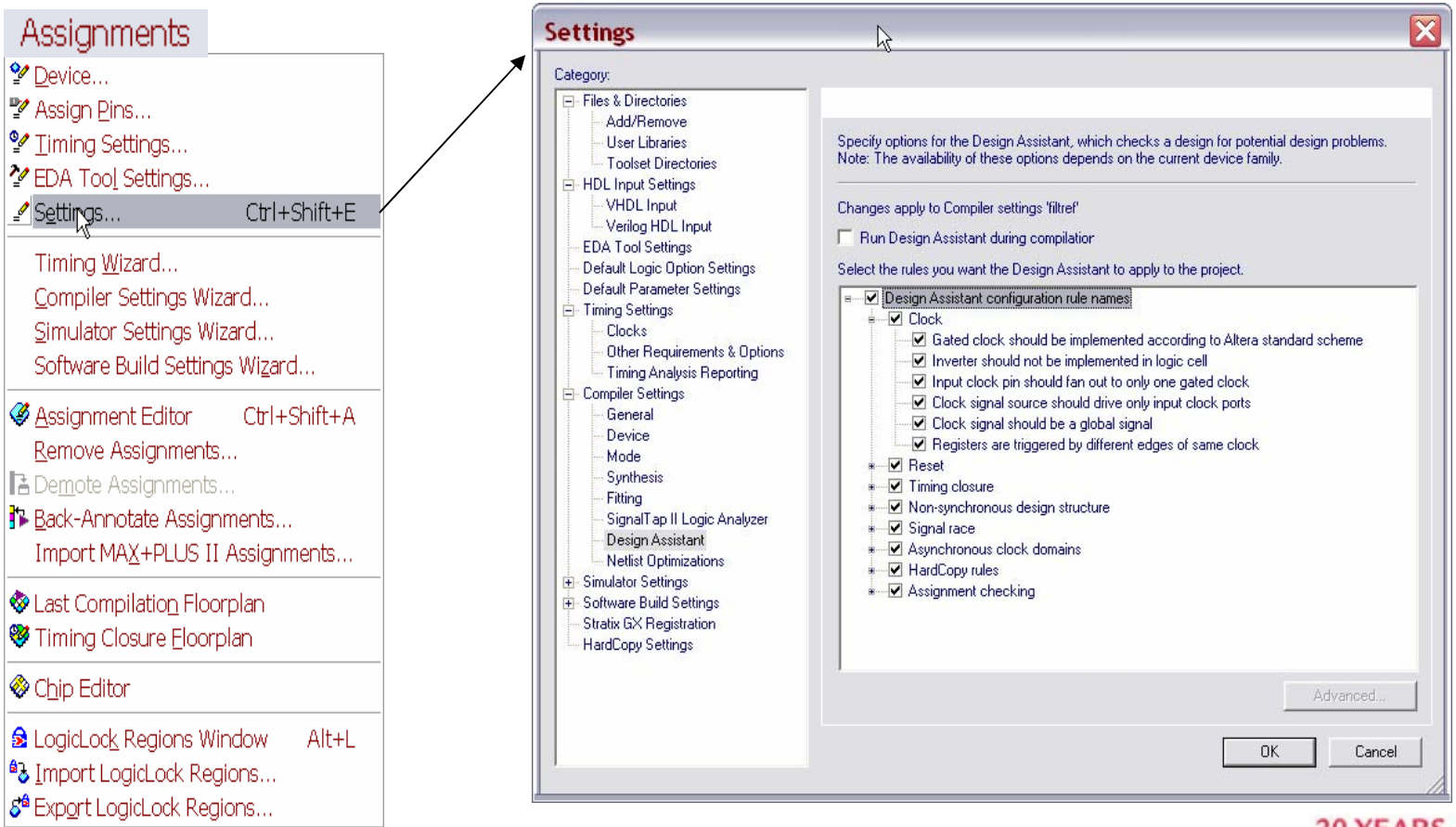
# Design Assistant

- Design Assistant Checks Your Design Against Design Rules That Are Selected Thru The Assignment Menu.  Turn It On During Compilation.

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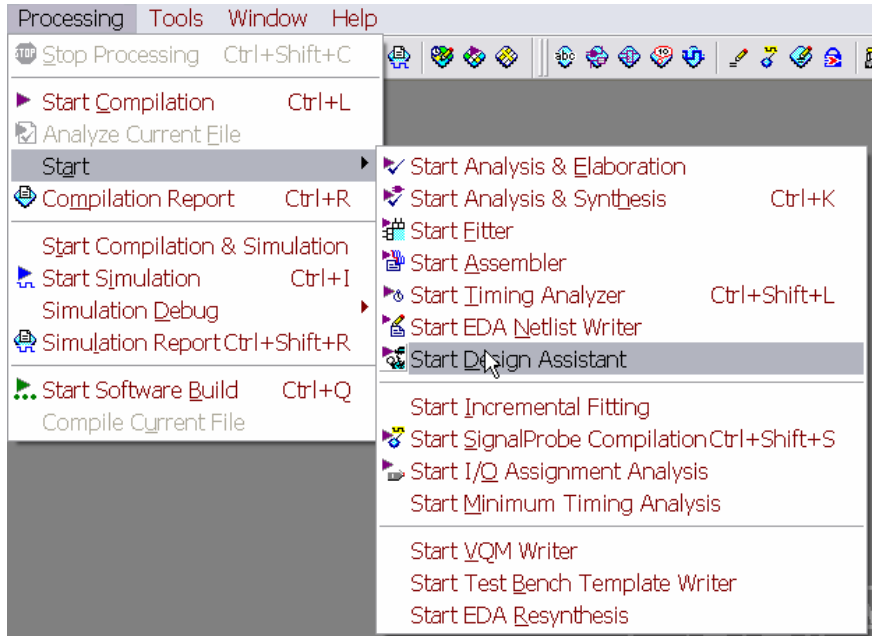
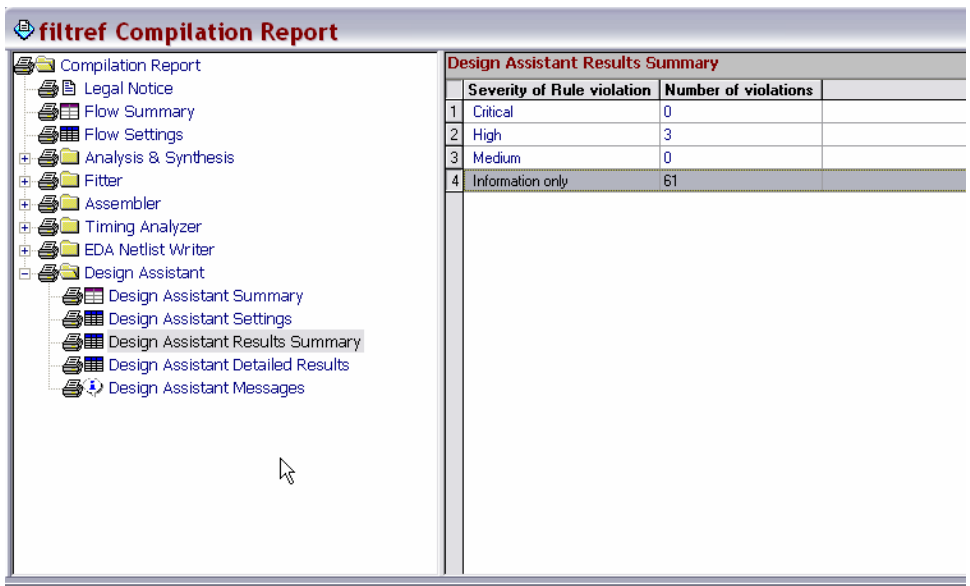
# Design Assistant (Continue)

- Rules Are In Place To Guarantee Smooth Migration From FPGA To HardCopy Device
- Checks The Viability Of The Design And Assesses Its Risk
- Need To Make Sure All Violations Are Reviewed  Informational Messages Are Acceptable

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# HardCopy Optimization Wizard

- HardCopy Will Always Perform As Good As FPGA. You May Not Need To Run Optimization Wizard Unless You Don't Meet Your Performance In FPGA
- The Optimization Wizard Is Used To Generate HardCopy Files That Will Approximate The Real Delays In The HardCopy Device
- The optimization wizard creates a new project directory, a .VSM file, and back-annotates the pin information from the original project.

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# HardCopy Optimization Wizard (continue)

- All Pin Assignments Are Preserved.
- All Pin Properties Are Preserved
  - I/O Standard, Drive Strength, …
- Global Assignments Are Maintained
- All Core Location Assignments Are Removed.
- All Logic Lock Regions Are Removed.
- All Timing Assignments Are Migrated
  - Including Multi-cycle, Point To Point Cuts, …

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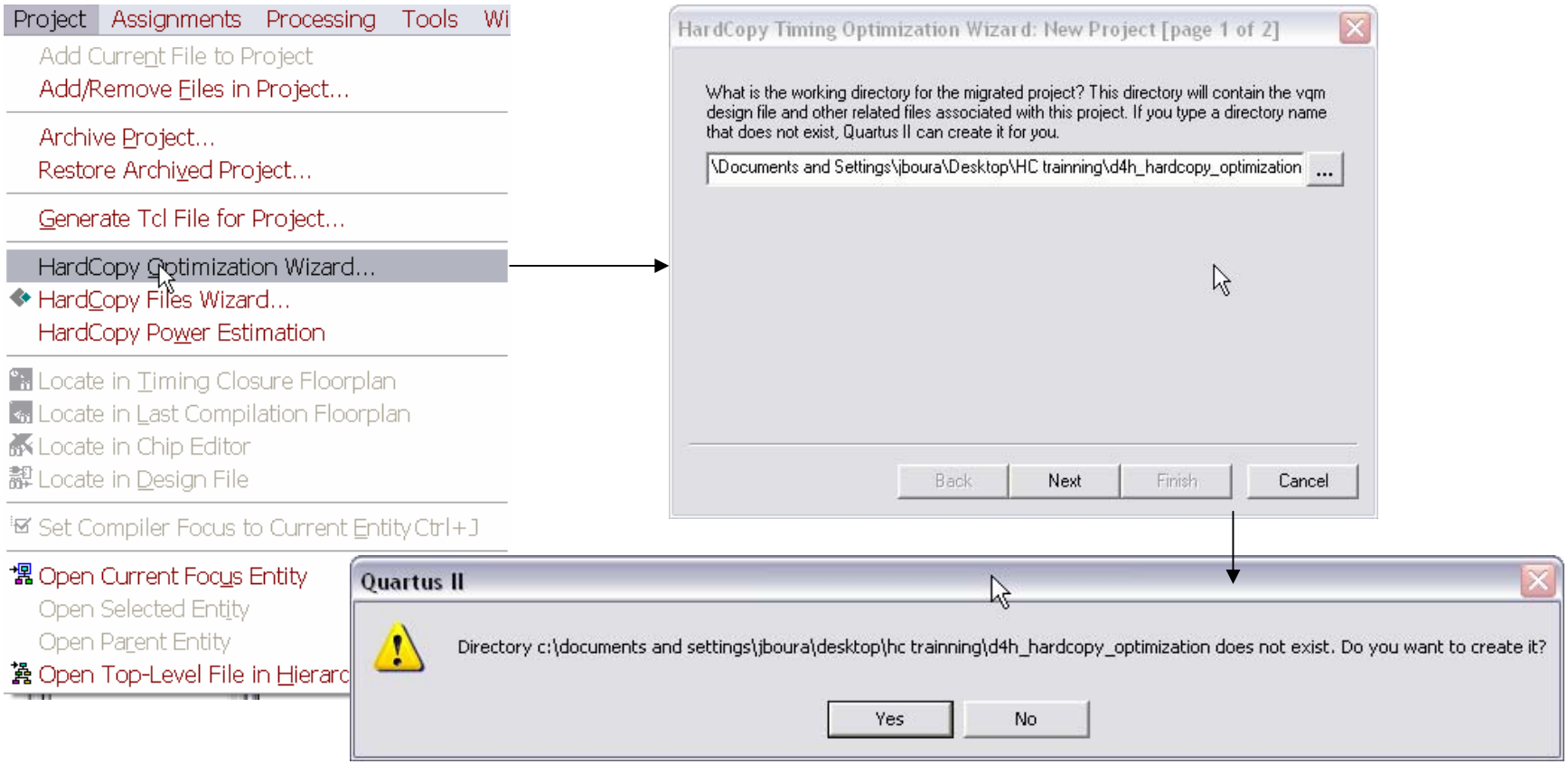
# HardCopy Optimization Wizard (Menu)

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# New Project

- We now have a new Quartus II Project in a new directory
  - Example: <my design>_hardcopy_optimization
  - Assigned to the equivalent Hardcopy member in the “Stratix Hardcopy” family.
- Old Quartus II project for FPGA_PROTOTYPE compile maintained
- Compiling the new project gives you the hardcopy timing estimation.
- Can change timing assignments
  - To optimize Hardcopy designs differently
  - To monitor timing differently

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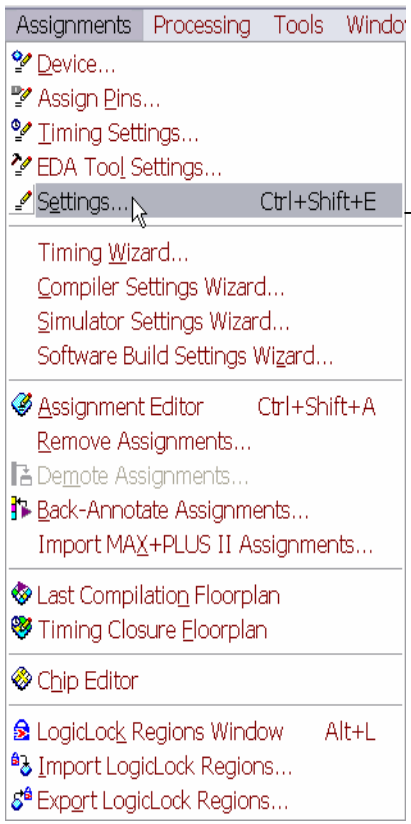
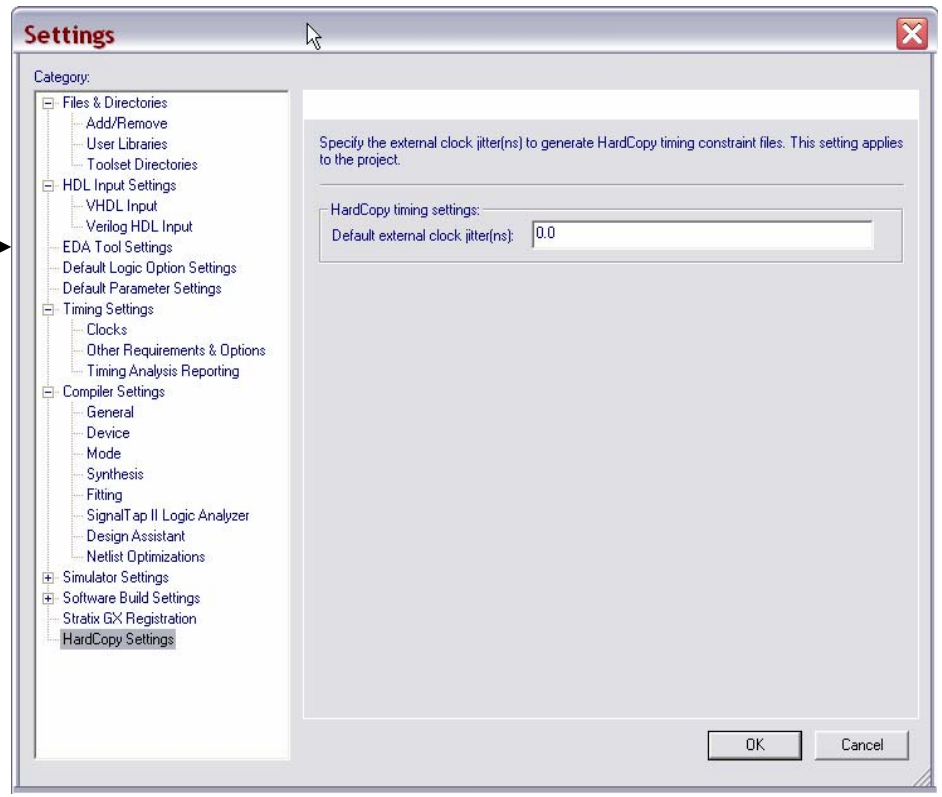
# HardCopy Timing Constraints

- In The New HardCopy Project Directory, Open The Project, Specify HardCopy Timing Constraint, Compile The Design, And Look Up The Timing Analyzer Results For The New FMAX.




Compile

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# HardCopy Files Wizard (formerly passport)

- The Files Wizard Could Be Run With Or Without An Optimization Run
- Runs Design Assistant With All Rules Enabled Regardless Of What The User Turned On/Off
- The Files Wizard Goes Thru An Interactive List Of Questions To Gather Design Specifications
- The Files Wizard Generates A .Qar File That Gets Sent To Altera For Conversion

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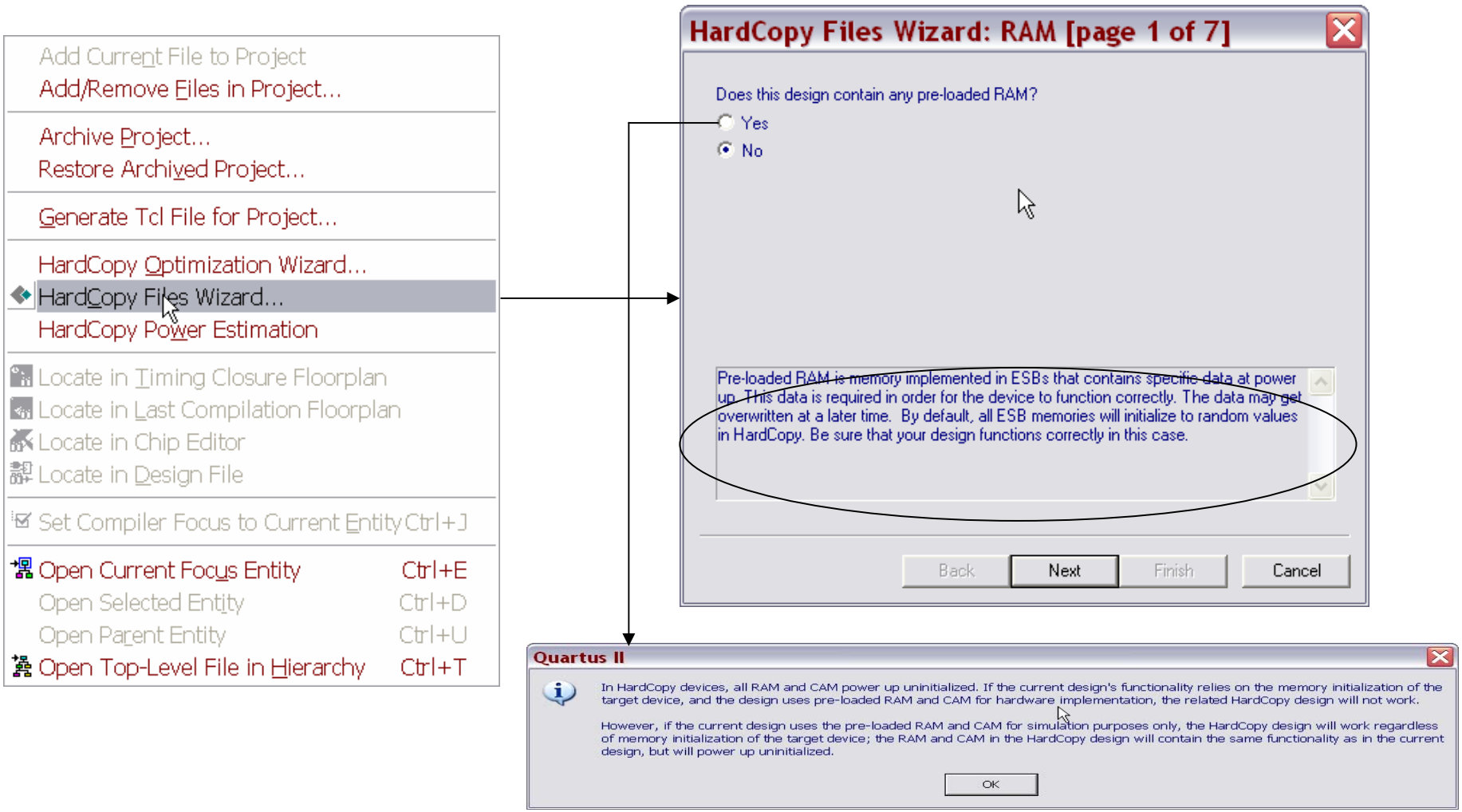
# HardCopy Files Wizard (Continue)

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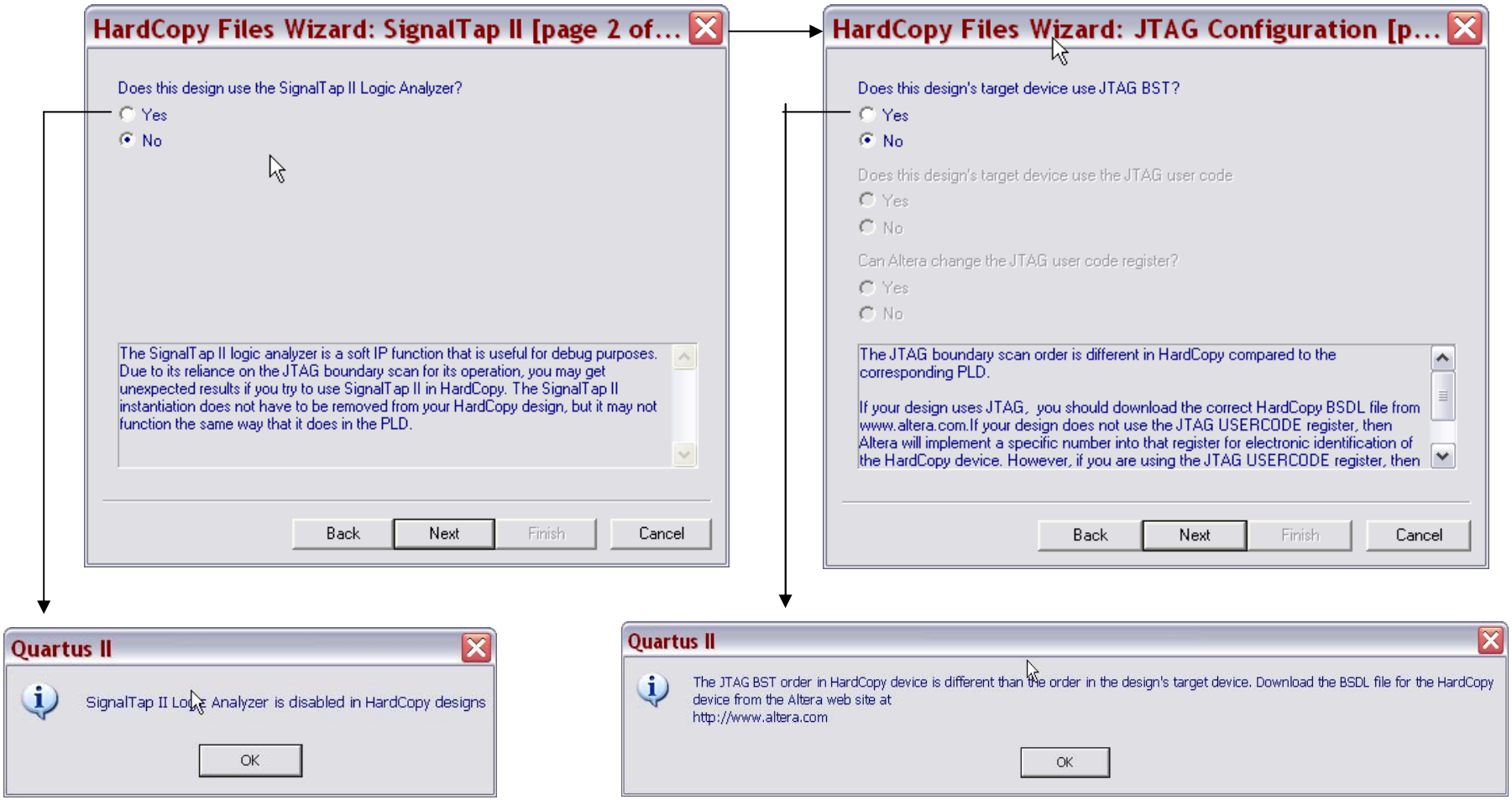
# HardCopy Files Wizard (Continue)




Signal Tap Is Fully Supported In HardCopy Stratix, But Not In HardCopy APEX

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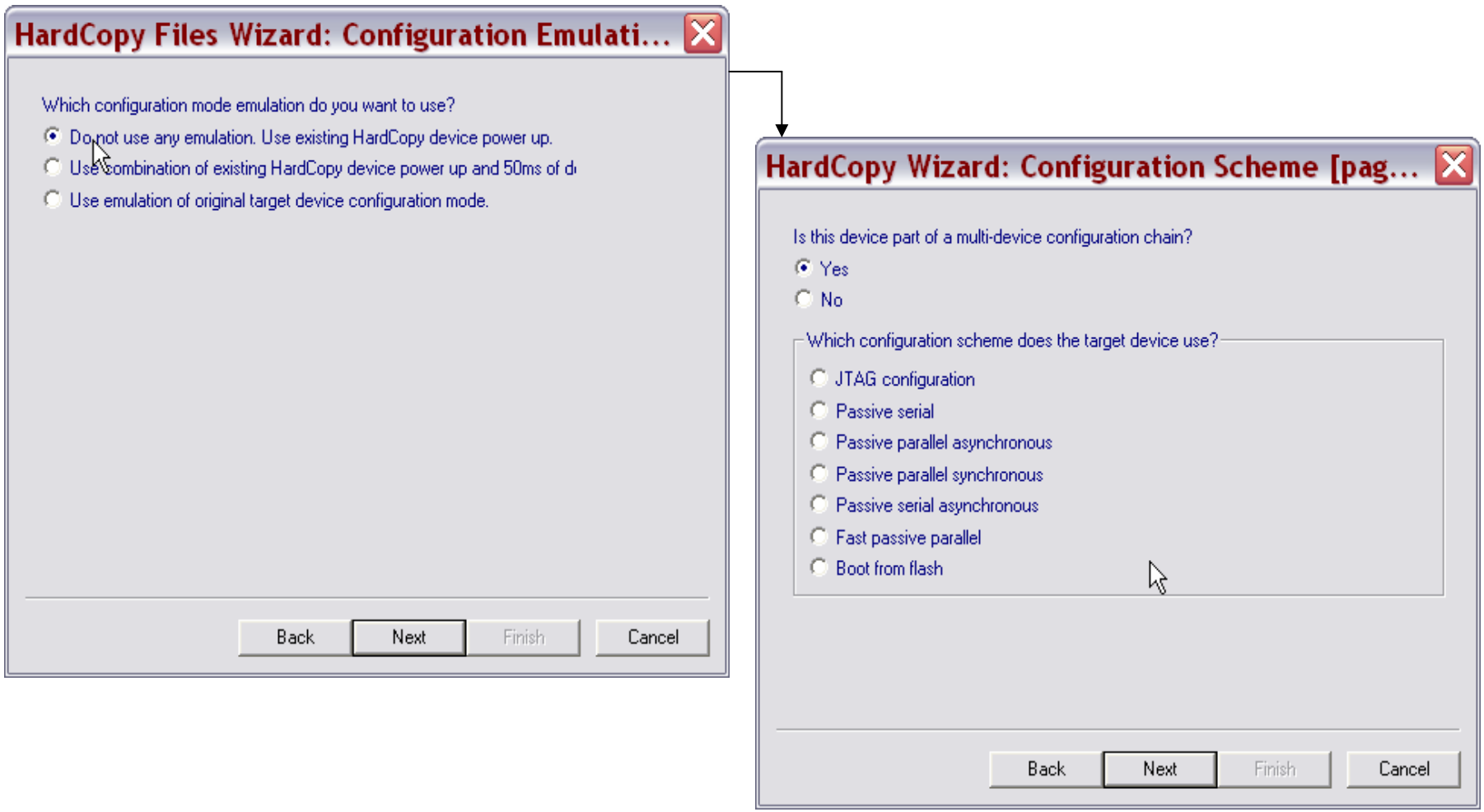
# HardCopy Files Wizard (Continue)

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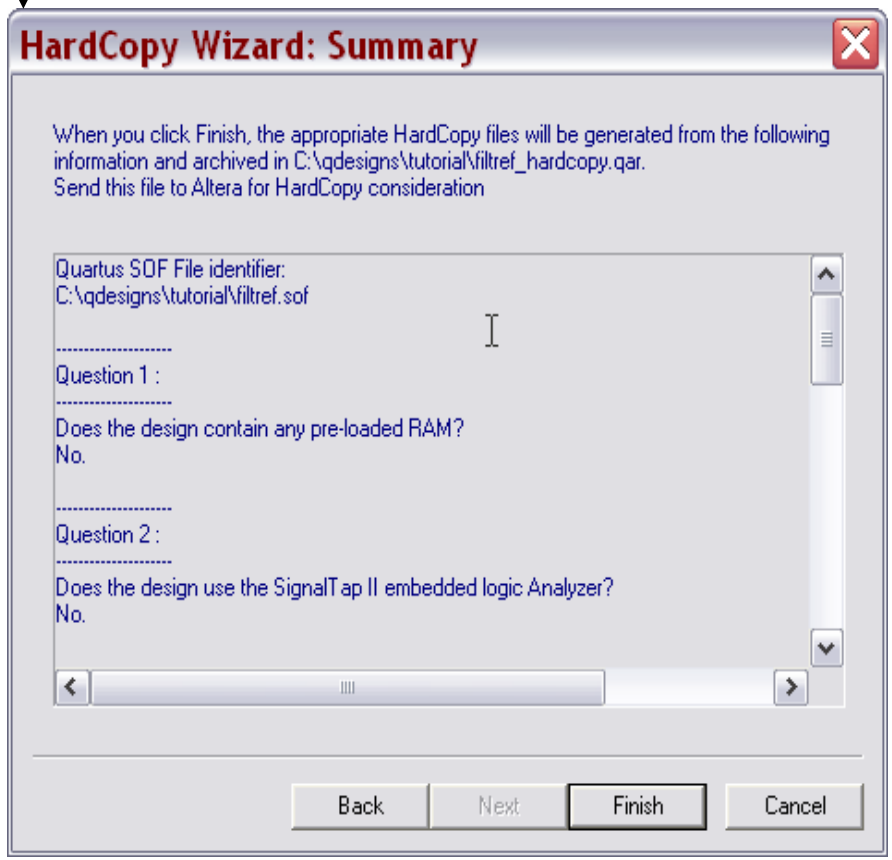
# HardCopy Files Wizard (Continue)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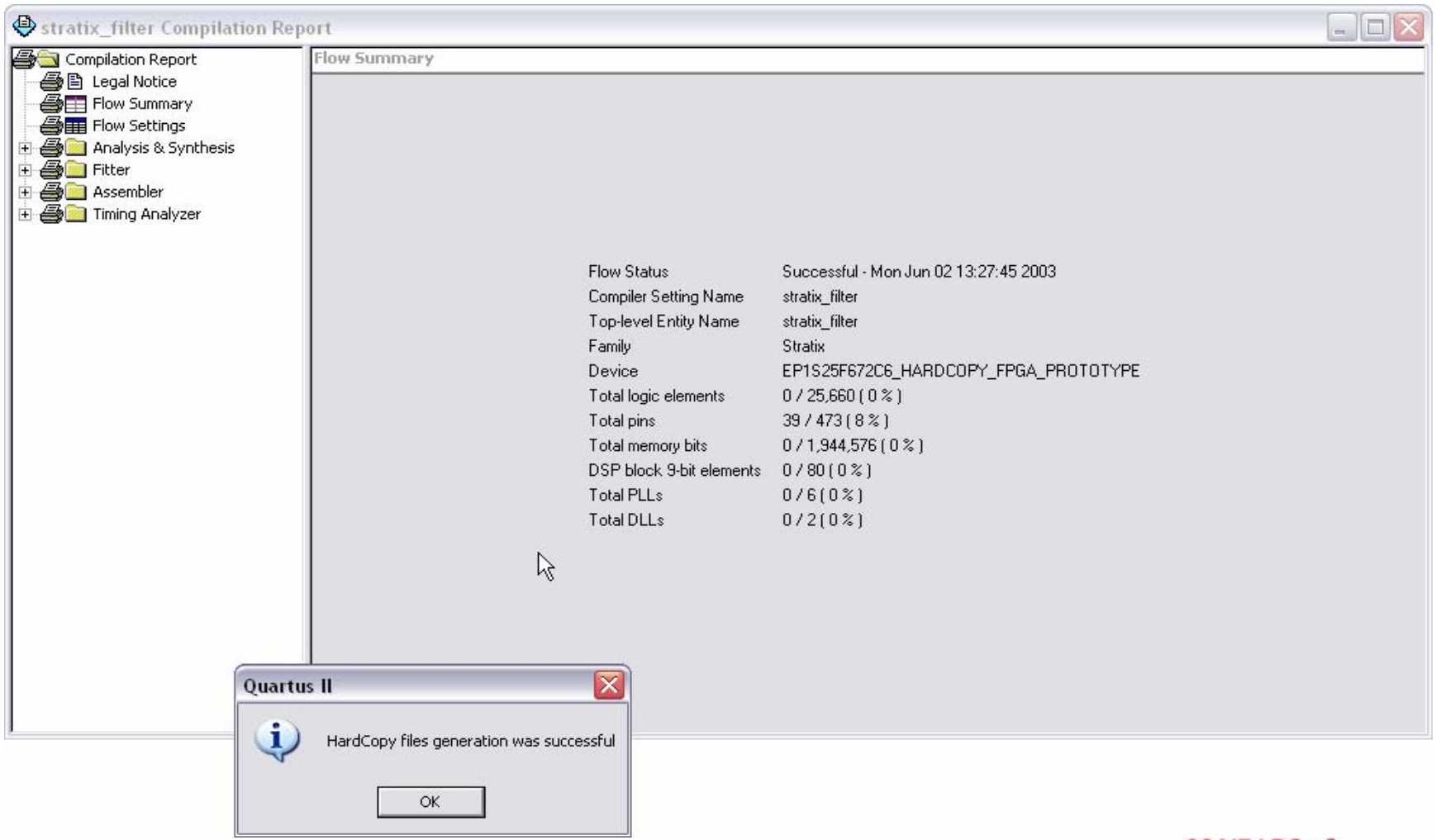
# HardCopy Files Wizard (Continue)

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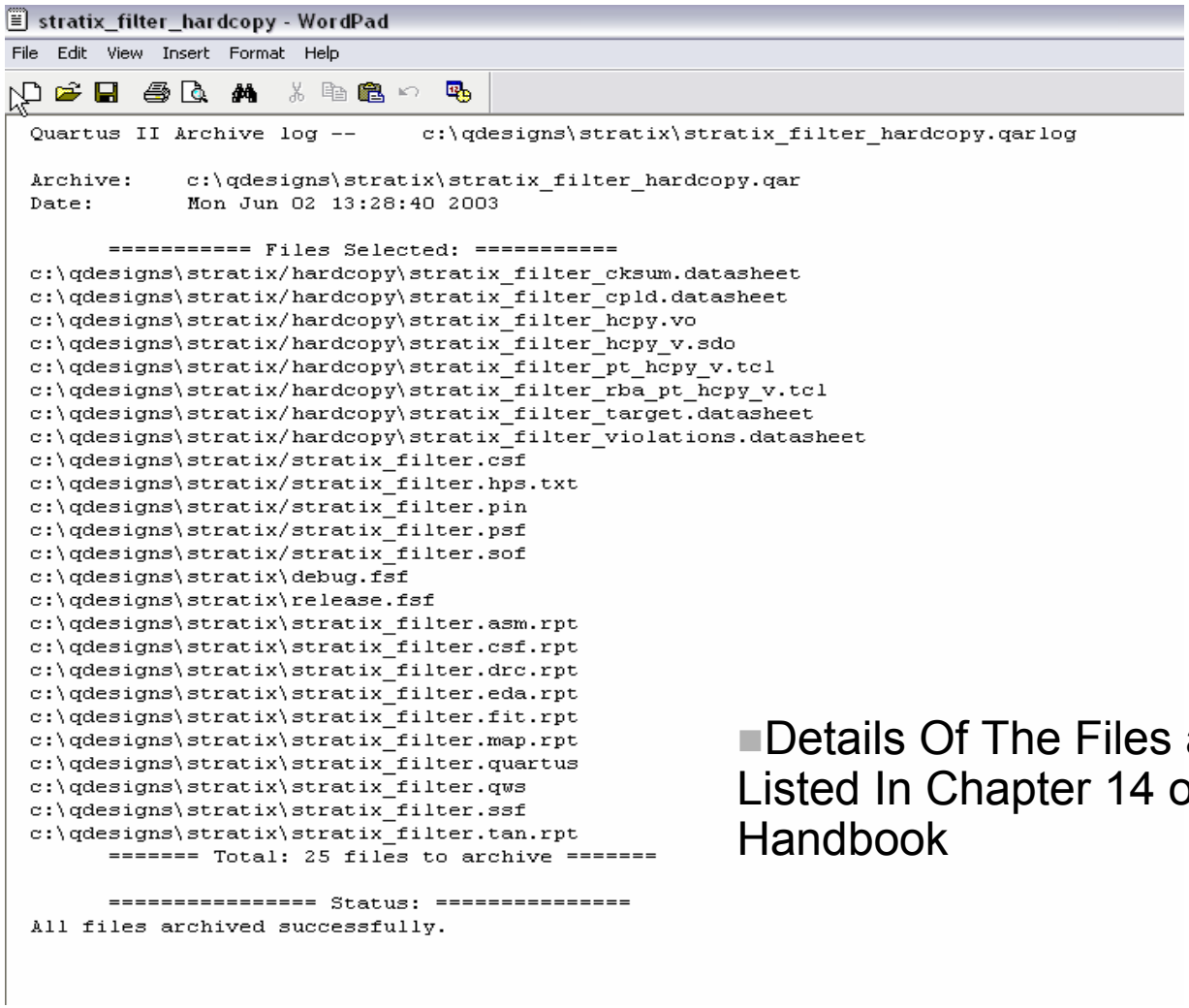
# HardCopy Generated Files Summary


stratix_filter_hardcopy - WordPad

File Edit View Insert Format Help

```
Quartus II Archive log --     c:\qdesigns\stratix\stratix_filter_hardcopy.qarlog

Archive:    c:\qdesigns\stratix\stratix_filter_hardcopy.qar
Date:       Mon Jun 02 13:28:40 2003

      =========== Files Selected: ===========
c:\qdesigns\stratix/hardcopy\stratix_filter_cksum.datasheet
c:\qdesigns\stratix/hardcopy\stratix_filter_cpld.datasheet
c:\qdesigns\stratix/hardcopy\stratix_filter_hcpy.vo
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c:\qdesigns\stratix\stratix_filter.map.rpt
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c:\qdesigns\stratix\stratix_filter.qws
c:\qdesigns\stratix\stratix_filter.ssf
c:\qdesigns\stratix\stratix_filter.tan.rpt
      ======= Total: 25 files to archive =======

      ================ Status: ===============
All files archived successfully.
```

- Details Of The Files archived in the .qar file are Listed In Chapter 14 of the HardCopy Device Handbook

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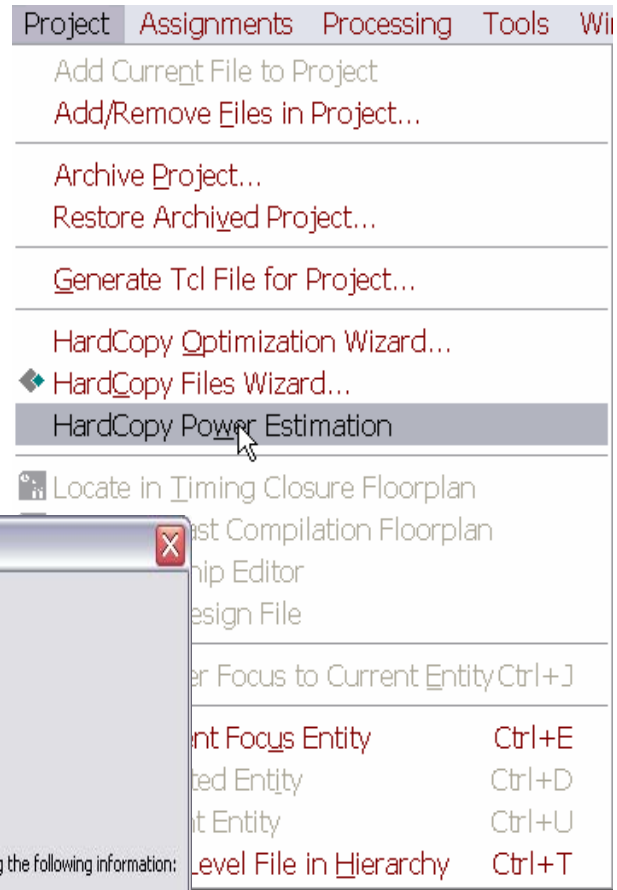
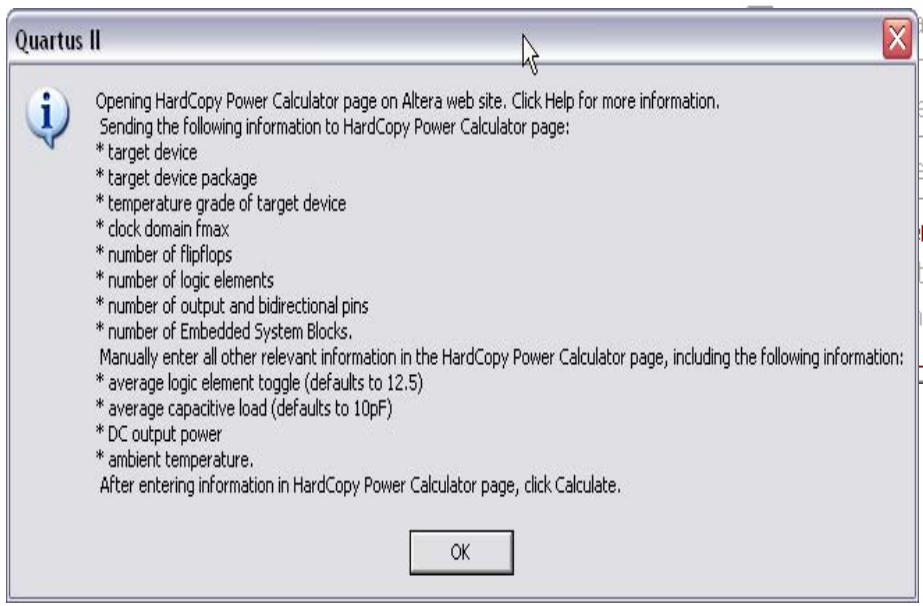
# HardCopy Power Estimation

- In The HardCopy Project Directory, Invoke The Power Calculator As Shown Thru The Menu.
- Upon Running The Power Estimation Command, Quartus II Automatically Sends Information And Configures The HardCopy Power Calculator On Altera's Web Site
- Some Information Will Have To Be Entered Manually. Most information can be changed manually.

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# HardCopy Power Estimation (continue)


*Table 1. Device*

| Device | Package | Temperature Grade | $V_{CCINT}$ (V) | Total $P_{INT}$ (mW) | Total $P_{IO}$ (mW) | Total $P_{TOTAL}$ (mW) |
|---|---|---|---|---|---|---|
| HC1S25 | 672 FineLine BGA | C-commercial | 1.5 | 140.81 | 2.41 | 143.23 |

| $I_{CC}$ Standby (mA) | |
|---|---|
| Typical | 90.00 |

[Go to Top] Calculate

**Clock Tree**

*Table 2. Global Clock Network*

| Global Clock Network | $f_{MAX}$ (MHz) | Number of Flip-Flops | $I_{CCINT}$ (mA) | $P_{INT}$ (mW) |
|---|---|---|---|---|
| 1 | 100.00 | 50.00 | 3.64 | 5.46 |
| 2 | 10.00 | 8.00 | 0.18 | 0.27 |
| 3 | 0.00 | 0.00 | 0.00 | 0.00 |
| 4 | 0.00 | 0.00 | 0.00 | 0.00 |
| 5 | 0.00 | 0.00 | 0.00 | 0.00 |
| 6 | 0.00 | 0.00 | 0.00 | 0.00 |
| 7 | 0.00 | 0.00 | 0.00 | 0.00 |
| 8 | 0.00 | 0.00 | 0.00 | 0.00 |
| 9 | 0.00 | 0.00 | 0.00 | 0.00 |
| 10 | 0.00 | 0.00 | 0.00 | 0.00 |
| 11 | 0.00 | 0.00 | 0.00 | 0.00 |
| 12 | 0.00 | 0.00 | 0.00 | 0.00 |
| 13 | 0.00 | 0.00 | 0.00 | 0.00 |
| 14 | 0.00 | 0.00 | 0.00 | 0.00 |
| 15 | 0.00 | 0.00 | 0.00 | 0.00 |
| 16 | 0.00 | 0.00 | 0.00 | 0.00 |
| | | Subtotal | 3.82 | 5.73 |

[Go to Top] Calculate

**HardCopy Stratix Power Calculator - Summary**

Calculate << Go back to Step 4

- Clock Tree
  - Global Clock Network
  - Regional Clock Network
  - Fast Regional Clock Network
- Logic Element (LE)
- Digital Signal Processing (DSP) Blocks
- Phase-Locked loops (PLL)
  - Enhanced Phase-Locked Loops
  - Fast Phase-Locked Loops
- RAM blocks
  - M512 Blocks
  - M4K Blocks
  - M-RAM Blocks
- High-Speed Differential Interface (HSDI)
  - Receiver
  - Transmitter
- General I/O Power Consumption
- Terminator Technology
- Total Power
- Thermal Analysis
  - Without Heat Sink
  - With Heat Sink

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# Designing For HardCopy (Back-Up Slides )

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# Designing For HardCopy

- Guidelines To Permit A Successful FPGA To HardCopy Device Conversion
- Good General Design Practice Guidelines
- Design Assistant Examines The Conformance Of Your Design Against These Design Rules
- Take Corrective Design Actions Based On Feedback From Design Assistant
- Case study

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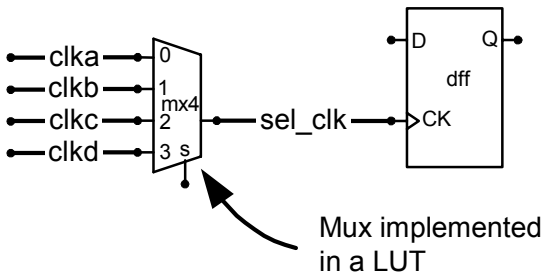
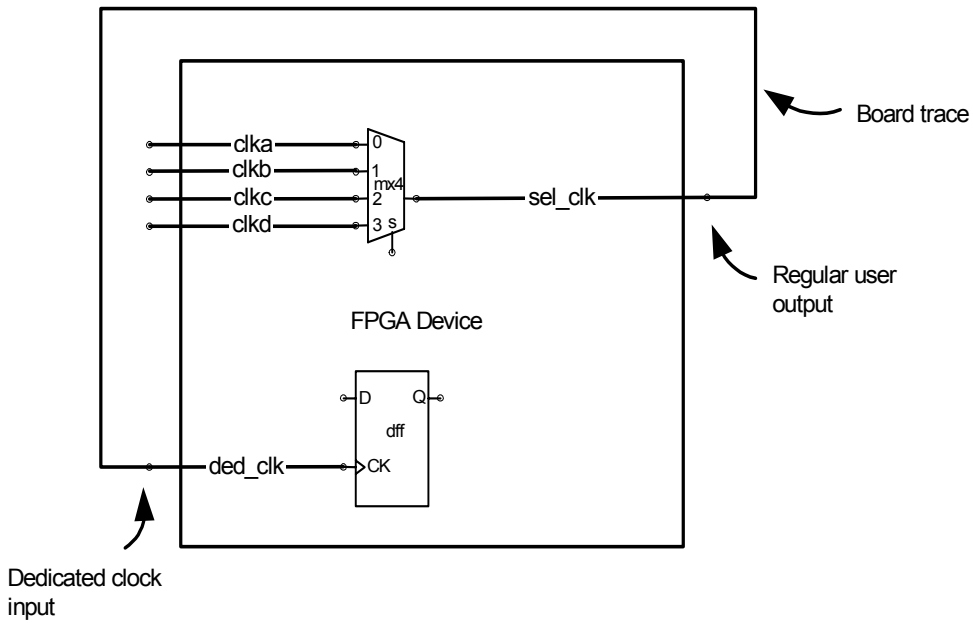
# HardCopy Recommendation 1

## Clocks

- All Clock Signals In A Design Should Be Global Signals  Clock Signals That Are Mapped To Regular Logic Can Affect The Performance Of The Design (i.e. Might Not Work)




## Can DO

- More Difficult STA

## Better To Do

- Easier STA
- Two Extra Pins

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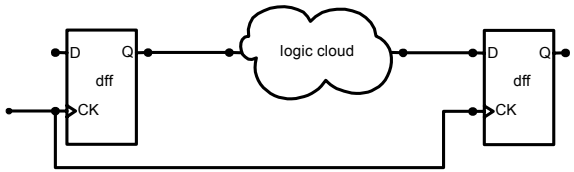
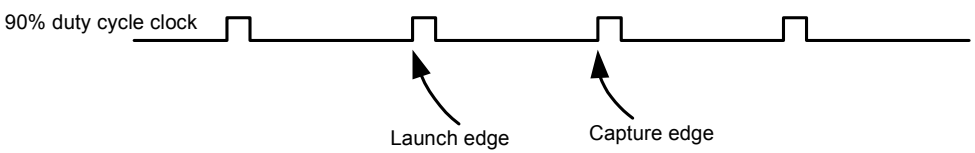
# HardCopy Recommendation 1

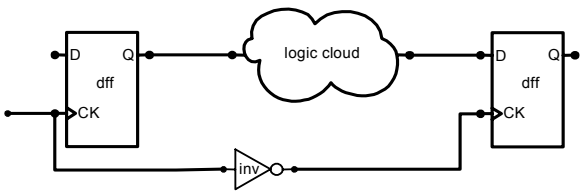
## Clocks

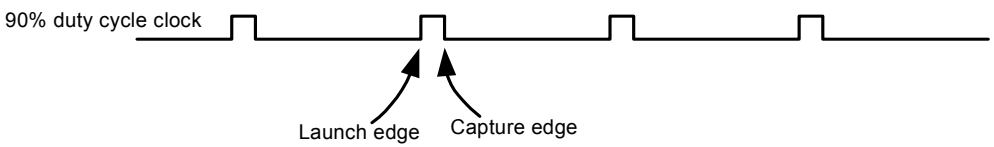
**Do**

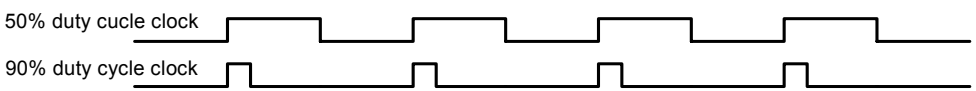



**Dont**




- Any Time A Circuit Needs To Use Both Edges Of The Clock, The Duty Cycle Has To Be Accurately Described For Proper Static Timing Analysis
- Try To Use Same Edge Clocking To Avoid Warnings By The Design Assistant

**Duty Cycle Will Determine Success In Meeting Timing Not Frequency (Probably Not The Intention)**

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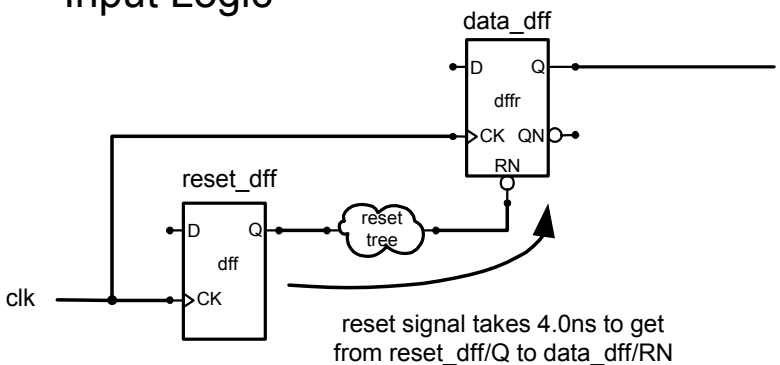
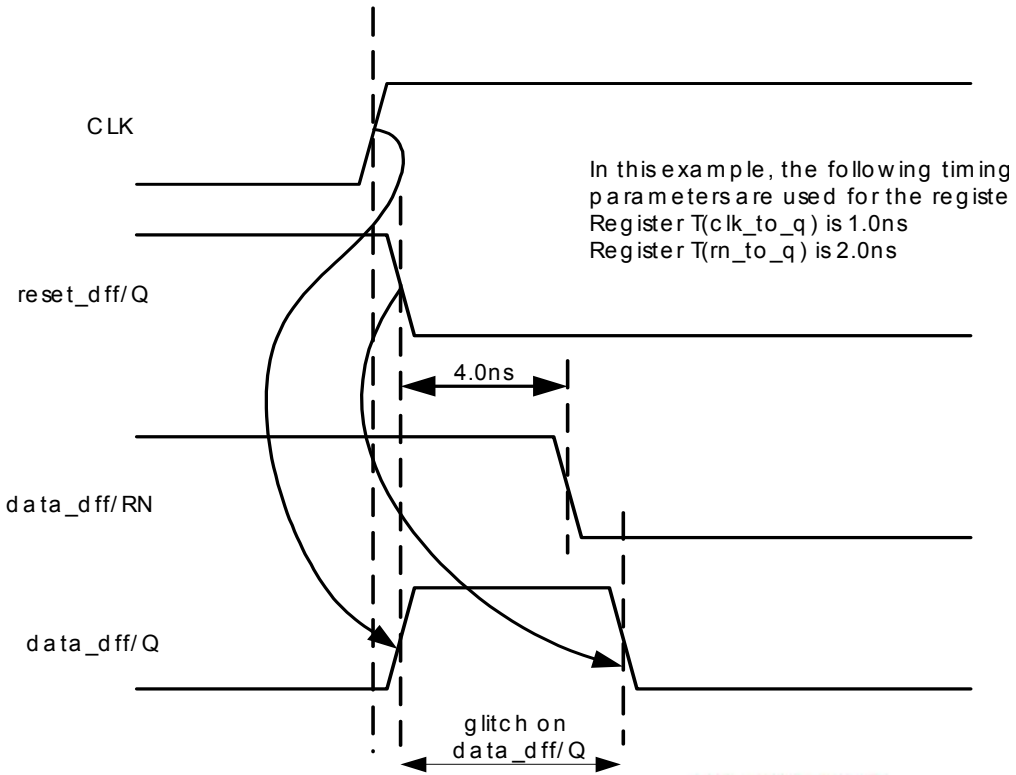
# HardCopy Recommendation 2

## Reset

- Reset Trees Have Inherent Delays In Them That Might Cause A Glitch On The Output Of Registers If This Presents A Problem In Your Design, Make Reset Part Of Your Input Logic




### Glitch Free Reset

```
Always @ (Posedge Clk)
Begin
   If (!Rst)
      Q <= 1'b0 ;
   Else
      Q <= D;
End
```

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# HardCopy Recommendation 3 Timing Closure

- Minimize Excessive Number Of Loads On Nets. This Will Improve Your Chances Of Meeting Your Design Goals
- If The Two Registers Are Triggered By Clock Edges At The Same Time, A Hold Time Violation May Occur. This Is Only A Design Assistant Info Message

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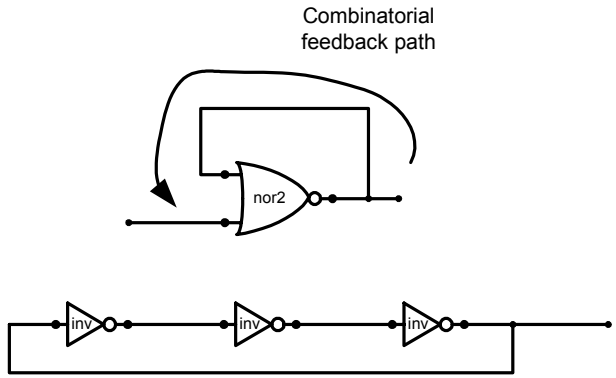
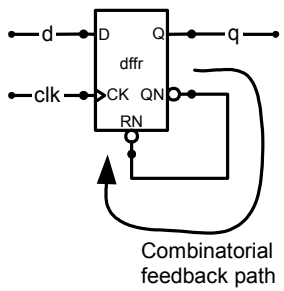
# HardCopy Recommendation 4

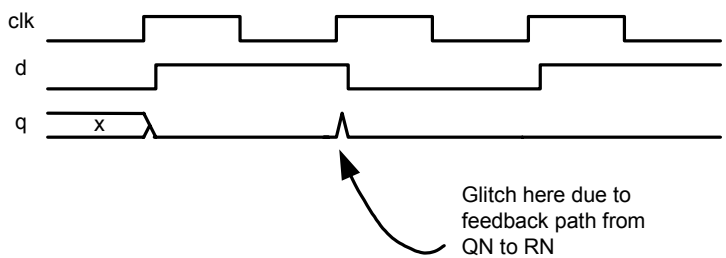
## Non-synchronous Design Structure

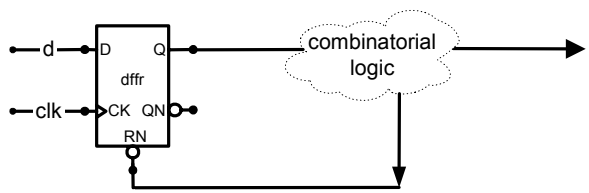
- A Design Should Not Contain Any Combinatorial Loops These Combinatorial Loops Can Cause Significant Stability And Reliability Problems In A Design




- A Design Should Not Contain Any Combinatorial Loops Where The Output Of A Register Directly Drives One Of Its Own Control Signals

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