20 YEARS *of*

ALTERA®

INNOVATION

SOPC WORLD 2003

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ALTERA MEMORY FEATURE

MEMORY BLOCK

- *M512, M4K, MEGARAM*
- *SINGLE, DUAL PORT RAM*
- *FIFO*

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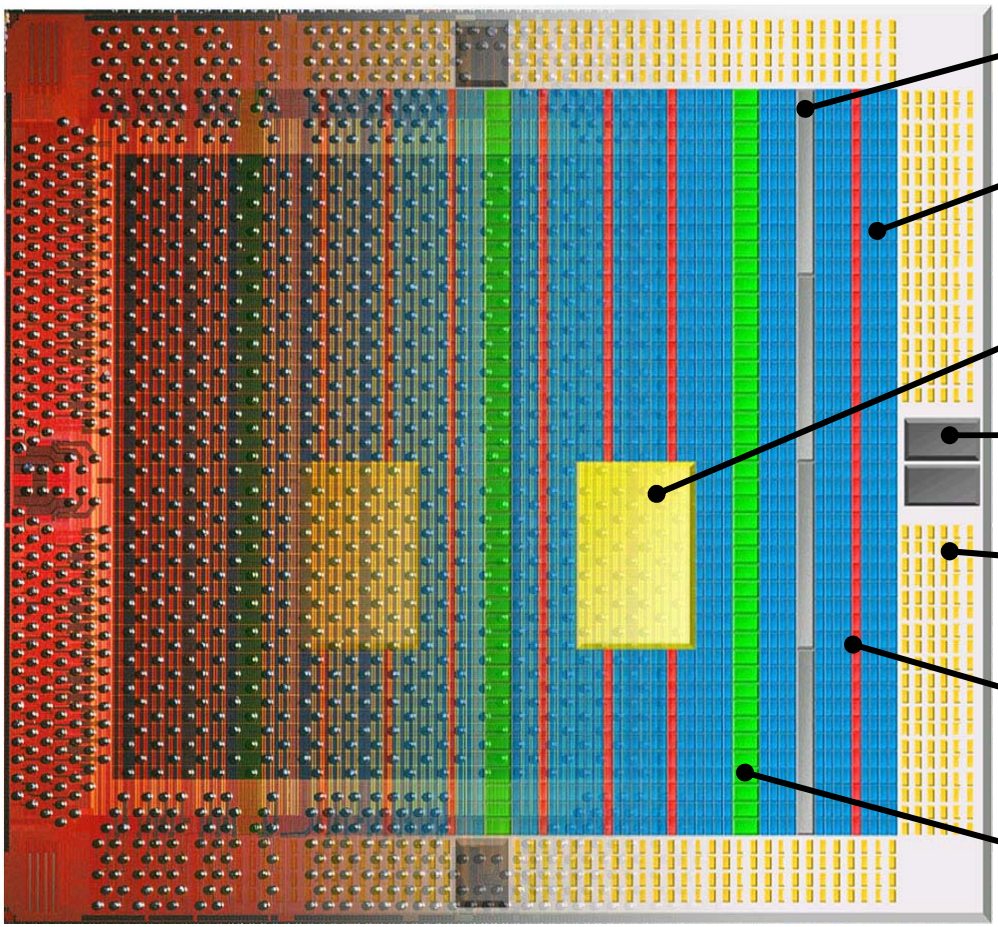
Stratix Architecture Overview



DSP Blocks

Logic Array Blocks (LABs)

M-RAM Blocks

Phase-Locked Loops (PLLs)

I/O Elements (IOEs)

M512 RAM Blocks

M4K RAM Blocks

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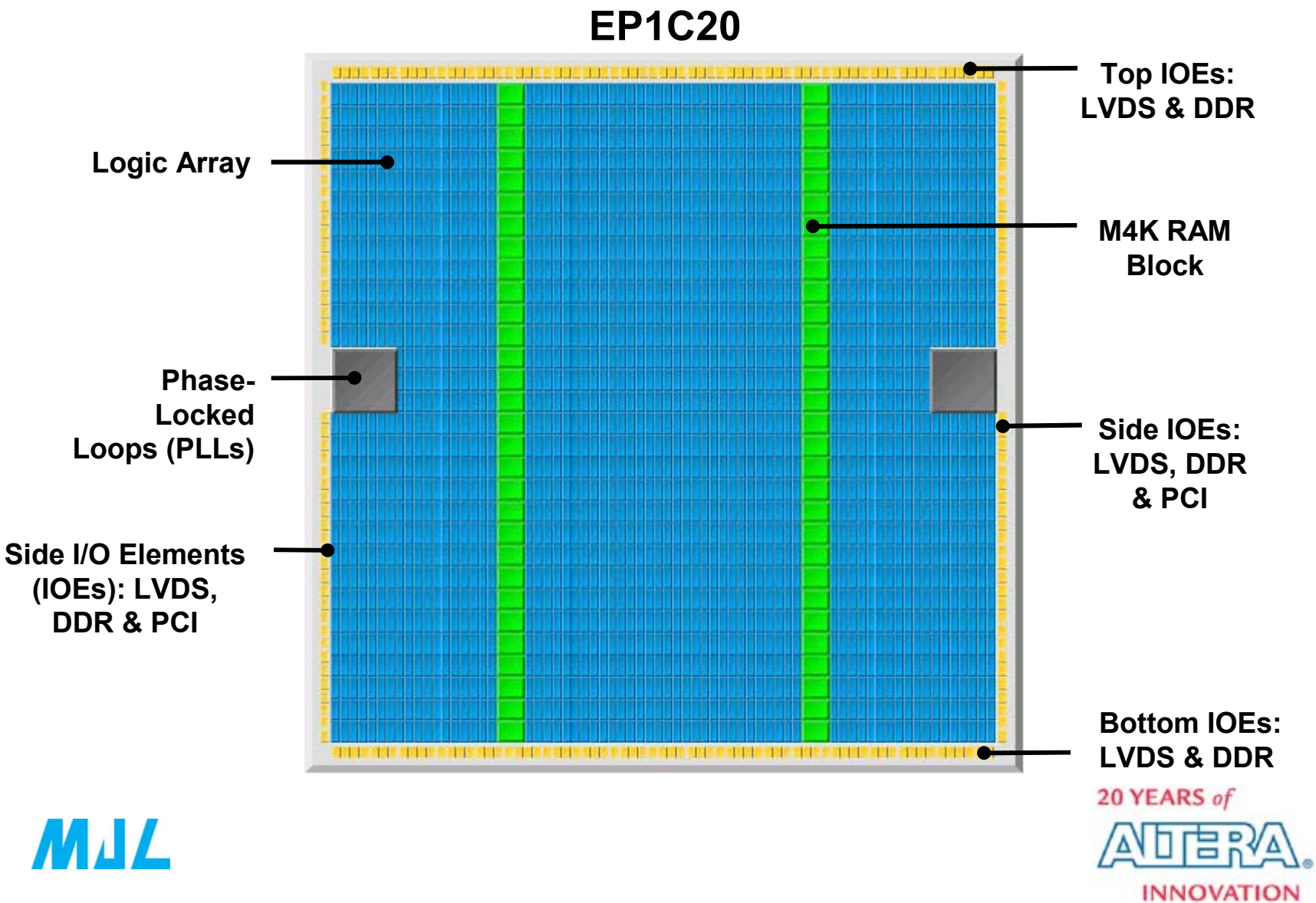
EP1C20 Device Floorplan



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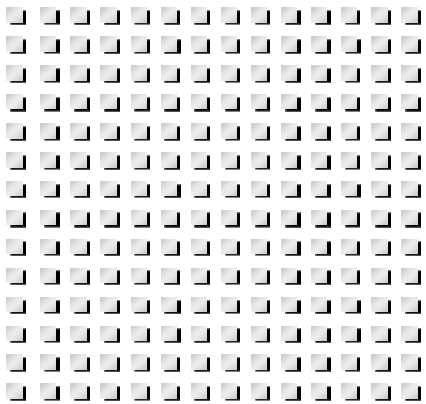
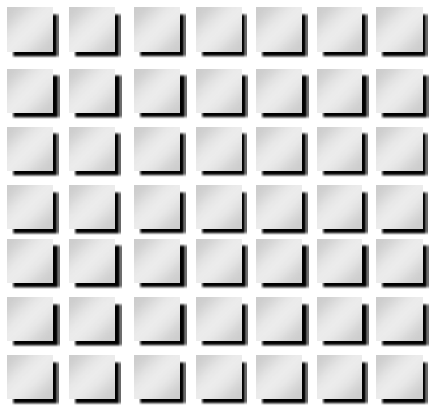
TriMatrix Memory

More Data Bits for Larger Memory Buffering

M512 Blocks	M4K Blocks	M-RAM Block
		
■ 512 Bits per Block	■ 4 Kbits per Block	■ 512 Kbits per Block
■ 32 Ports per Kbit	■ 8 Ports per Kbit	■ 0.25 Ports per Kbit
■ Up to 1,118 Blocks	■ Up to 520 Blocks	■ Up to 12 Blocks

More Data Ports for Greater Memory Bandwidth

Addresses Memory Bandwidth & Capacity Requirements

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Memory Block Summary

Memory Feature	M512 576 Bits	M4K 4,608 Bits	M-RAM 589,824 Bits
Performance	312 MHz	312 MHz	300 MHz
True Dual-Port Mode		●	●
Parity Bits	●	●	●
Shift Register Mode	●	●	
Mixed-Clock Mode	●	●	●
Byte Enable		●	●
Preload	●	●	
Read-Only Mode	●	●	
Initialization Support	●	●	
Power-up Conditions	Outputs Cleared	Outputs Cleared	Outputs Undefined
Register Clears	Input & Output	Input & Output	Output
Same Port Read during Write	New Data on Positive Edge	New Data on Positive Edge	New Data on Positive Edge
Mixed-Port Read during Write	Unknown or Old Data	Unknown or Old Data	Unknown

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M-RAM Profile

Type: M-RAM Block

Applications: Packet Buffers, Processor Memory, Cache

Size: 589,824 Bits (Includes Parity Bits)

Features

- 300-MHz Performance
- Fully Synchronous
- True Dual-Port Mode
- Simple Dual-Port Mode
- Mixed-Clock Mode
- Mixed-Width Mode
- Byte Enables

Mixed-Width Configurations

Read Port (A)	Write Port (B)				
	64Kx9	32Kx18	16Kx36	8Kx72	4Kx144
64Kx9	✓	✓	✓	✓	
32Kx18	✓	✓	✓	✓	
16Kx36	✓	✓	✓	✓	
8Kx72	✓	✓	✓	✓	
4Kx144					●

✓ Supported in Simple & True Dual-Port Mode

● Supported Only in Simple Dual-Port Mode

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M4K Profile

Type: M4K Block

Applications: Header Storage, Channelized Functions, Packet Processing

Size: 4,608 Bits (Includes Parity Bits)

Features

- 312-MHz Performance
- Fully Synchronous
- True Dual-Port Mode
- Simple Dual-Port Mode
- Mixed-Clock Mode
- Mixed-Width Mode
- Shift Register Mode
- Read-Only Mode
- Byte Enables
- Initialization Support

Mixed-Width Configurations

Read Port (A)	Write Port (B)								
	4Kx1	2Kx2	1Kx4	512x8	256x16	128x32	512x9	256x18	128x36
4Kx1	✓	✓	✓	✓	✓	✓			
2Kx2	✓	✓	✓	✓	✓	✓			
1Kx4	✓	✓	✓	✓	✓	✓			
512x8	✓	✓	✓	✓	✓	✓			
256x16	✓	✓	✓	✓	✓	✓			
128x32	✓	✓	✓	✓	✓	✓			
512x9							✓	✓	●
256x18							✓	✓	●
128x36							●	●	●

✓ Supported in Simple & True Dual-Port Mode

● Supported Only in Simple Dual-Port Mode

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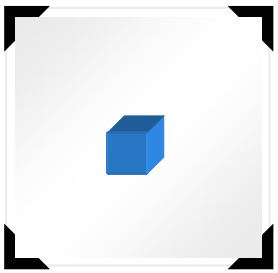
M512 Profile



Type: M512 Block

Applications: FIFOs, Filter Delay Elements, Rake Receiver Correlator

Size: 576 Bits (Includes Parity Bits)

Features

- 312-MHz Performance
- Fully Synchronous
- Simple Dual-Port Mode
- Mixed-Clock Mode
- Mixed-Width Mode
- Shift Register Mode
- Read-Only Mode
- Initialization Support

Mixed-Width Configurations

Read Port (A)	Write Port (B)						
	512x1	256x2	128x4	64x8	32x16	64x9	32x18
512x1	✓	✓	✓	✓	✓		
256x2	✓	✓	✓	✓	✓		
128x4	✓	✓	✓		✓		
64x8	✓	✓		✓			
32x16	✓	✓	✓		✓		
64x9						✓	
32x18							✓

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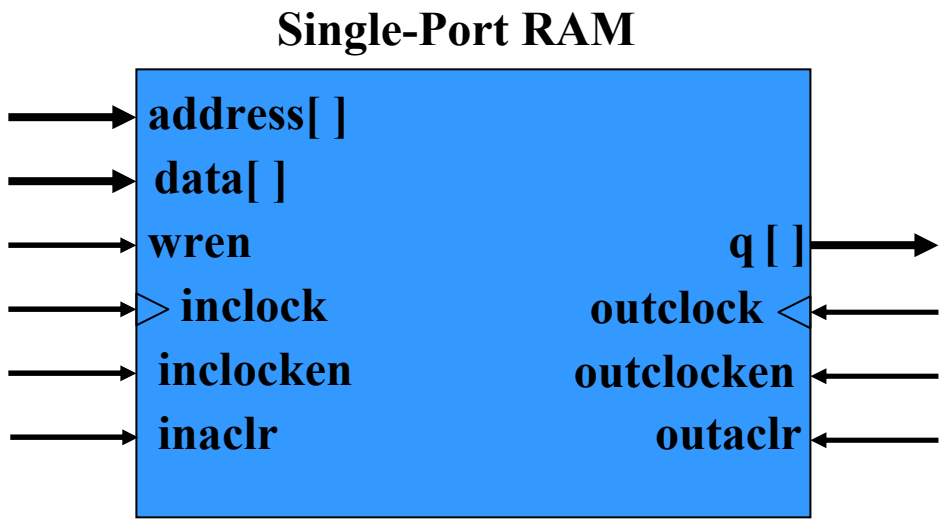
Single-Port RAM

- Single-Port RAM
  - Read & Write Address Are the Same Port
  - All Inputs Are Registered
- Clocking Options
  - Single Clock
  - Input/Output Clock Mode



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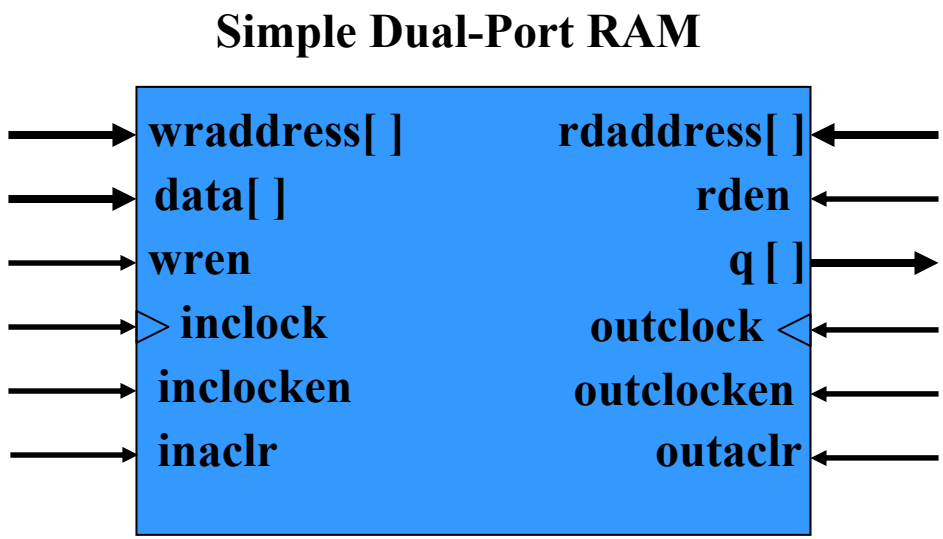
Simple Dual-Port RAM

- Simple Dual-Port RAM
  - Separate Read & Write Ports
  - All Inputs Are Registered
  - Mixed Width Capability
- Clocking Options
  - Single Clock
  - Input/Output Clock Mode
  - Read/Write Clock Mode



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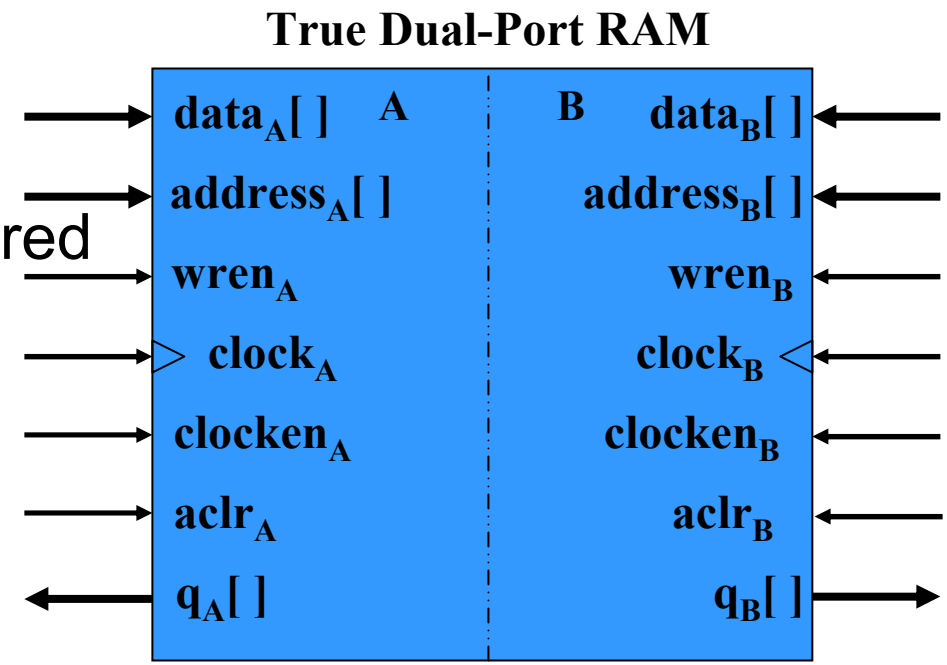
True Dual-Port RAM

- True Dual-Port RAM
  - Port A & Port B
  - All Inputs Must Be Registered
  - Mixed Width Capability
- Clocking Options
  - Single Clock
  - Input/Output Clock Mode
  - Independent Clock Mode



Shift Register Mode

- Fast Shift Register Implementation Reduces LE Resource Consumption
- Maximum Length Determined by Size of Block
  - Conditions
    - W x M x N Must Be Less than Total Number of Bits in Block
    - W x N Must Be Less than Maximum Data Width of Block
      - W: Input Data Width of Shift Register
      - M: Length of Taps
      - N: Number of Taps
- Larger Register Created by Cascading Multiple Memory Blocks Together

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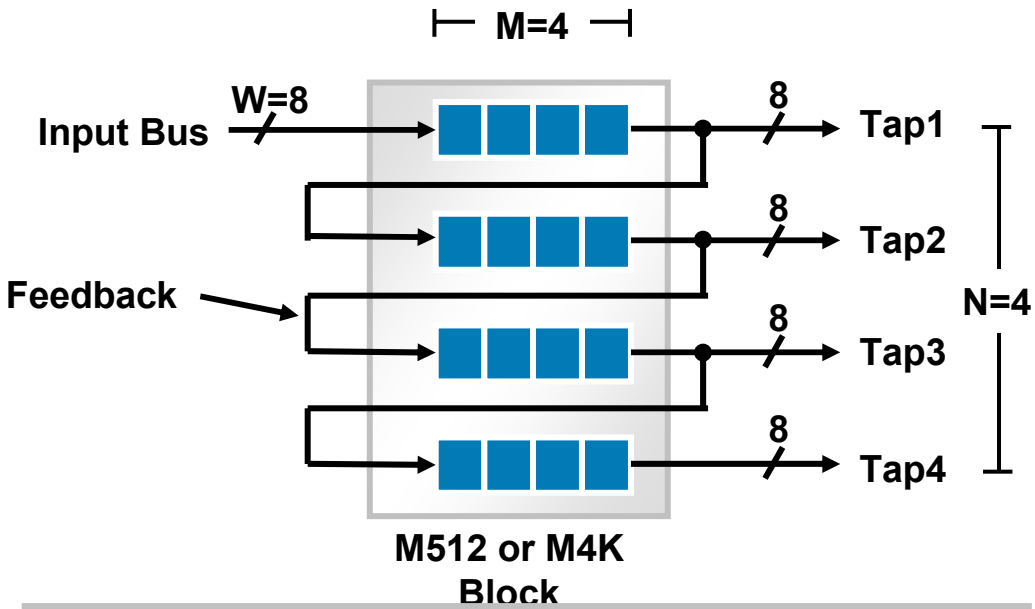
Shift Register Example

- 8-Bit Input Bus (W), Four Taps (N) & 4 Bits per Tap (M)



Memory Block	Maximum Shift Register Size (W x M x N)	Maximum Number of Outputs (W x N)
M4K Block	4,608	36
M512 Block	576	18

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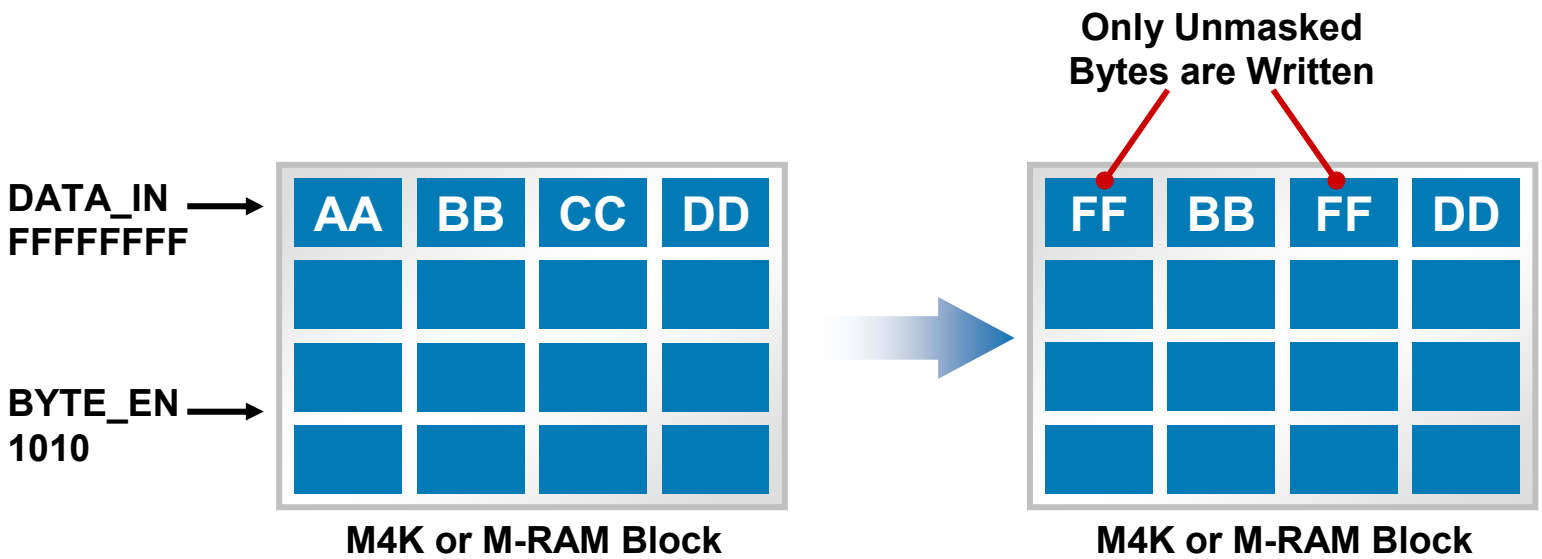
Byte Enables

- Allow Byte Masking During Write Operations
- Can Mask x8 or x9 Byte Sizes of Entire Word
- Used for Narrow Write & Wide Read Operations
- Byte Enable Signal Indicates Masked Bytes



Parity

- Supported by All Blocks
- Data Sizes Provide for 1 Extra Bit Per Byte
  - X9, X18 in M512
  - X9, X18, X36 in M4K
  - X9, X18, X36, X72, X144 in MegaRAM
- Bit Checked During Read or Generated During Write
- Useful For Control Bits Also

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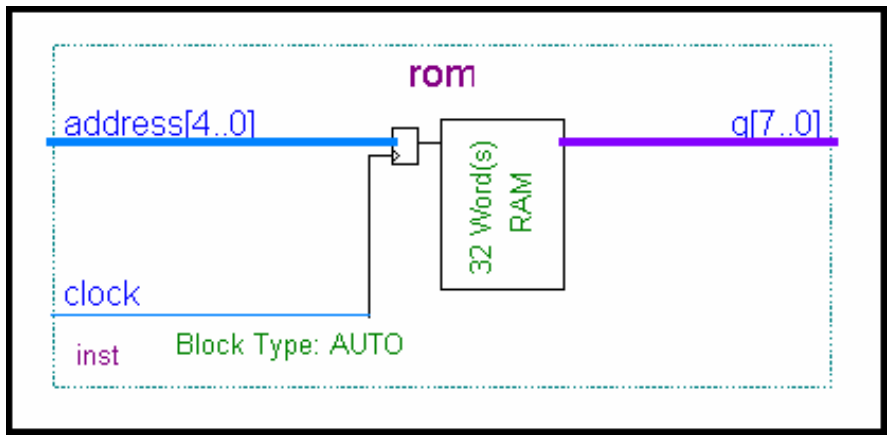
ROM

- Read Only Memory
  - All Inputs Are Registered
- Clocking Options
  - Single Clock
  - Input/Output Clock
- M512/M4K Block Only



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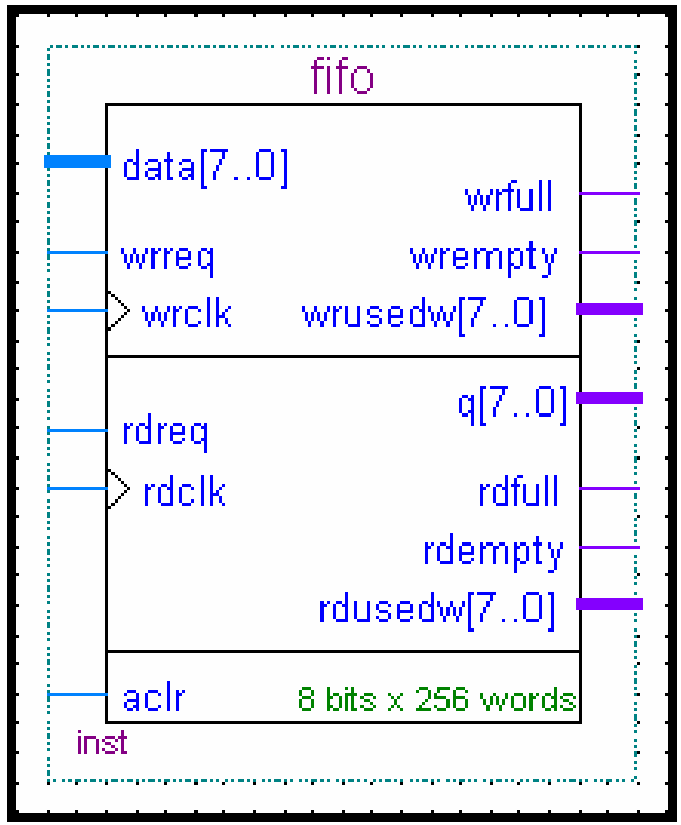
FIFO

- First in First Out Memory
  - Ideal for Rate Changing
  - All Inputs Are Registered
- Clocking Options
  - Single Clock
  - Read/Write Clock Mode



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MegaWizard

- Stratix RAMs Must Have All Inputs Registered
- New MegaFunction ALTSYNCRAM
  - Select for All Stratix RAM & ROM
- New MegaFunction ALTSHIFT_TAPS
  - Shift Register Mode
- Use LPM_FIFO+ for FIFOs

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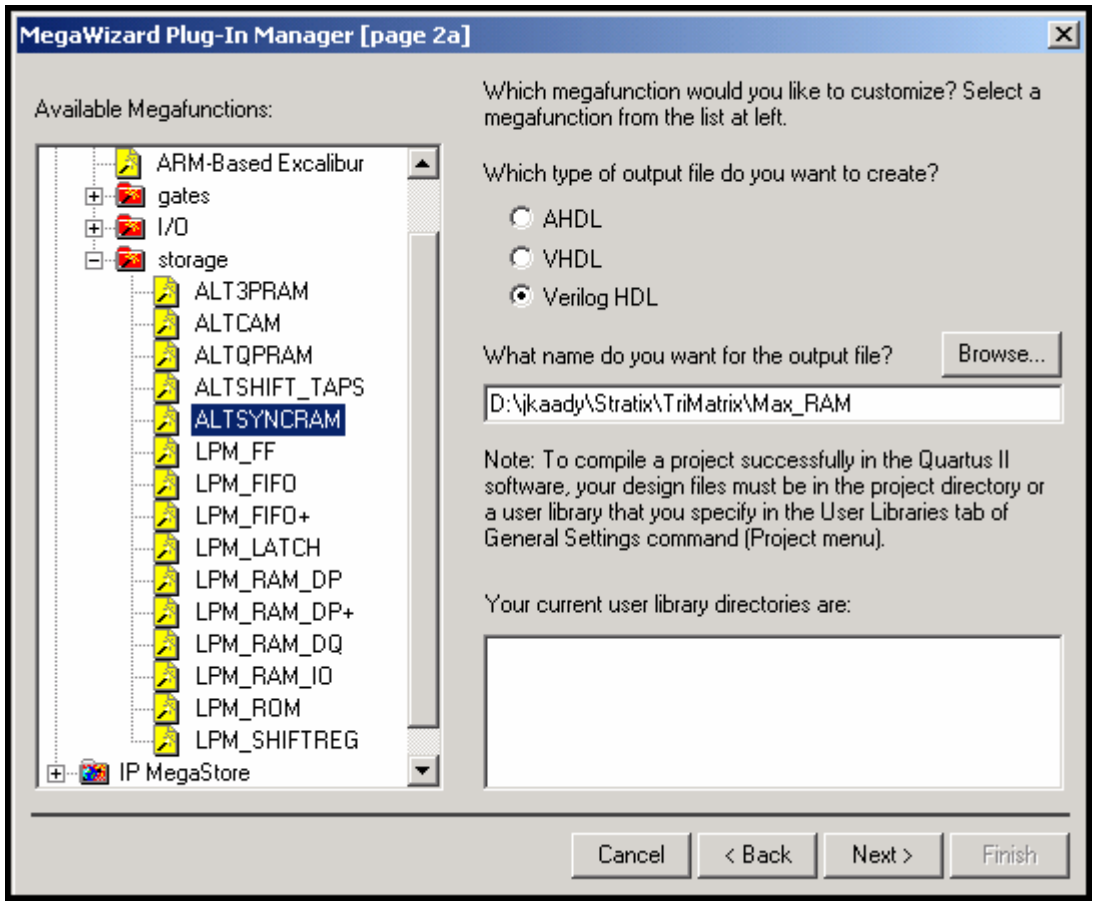
ALTSYNCRAM

- Located in the Storage Section



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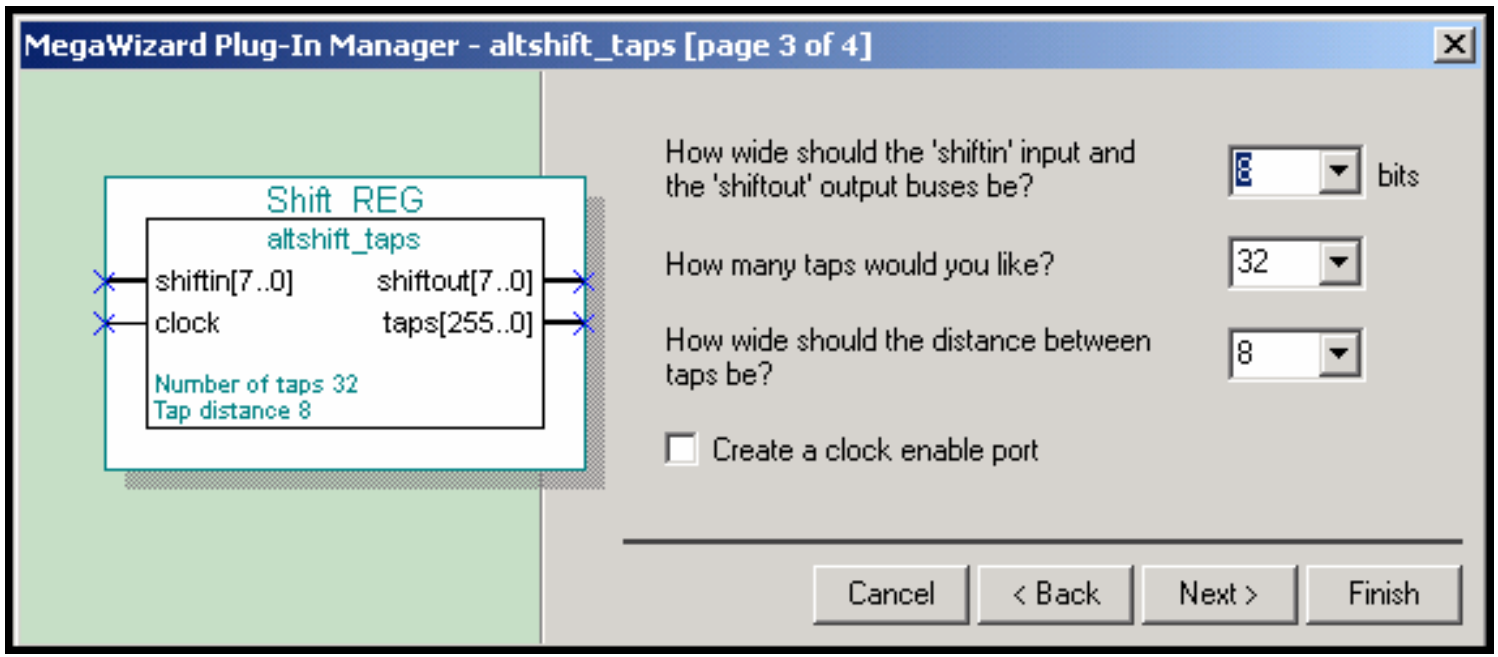
ALTSHIFT_TAPS

- Located in the Storage Section
  - Configure the RAM for Shift Register Mode



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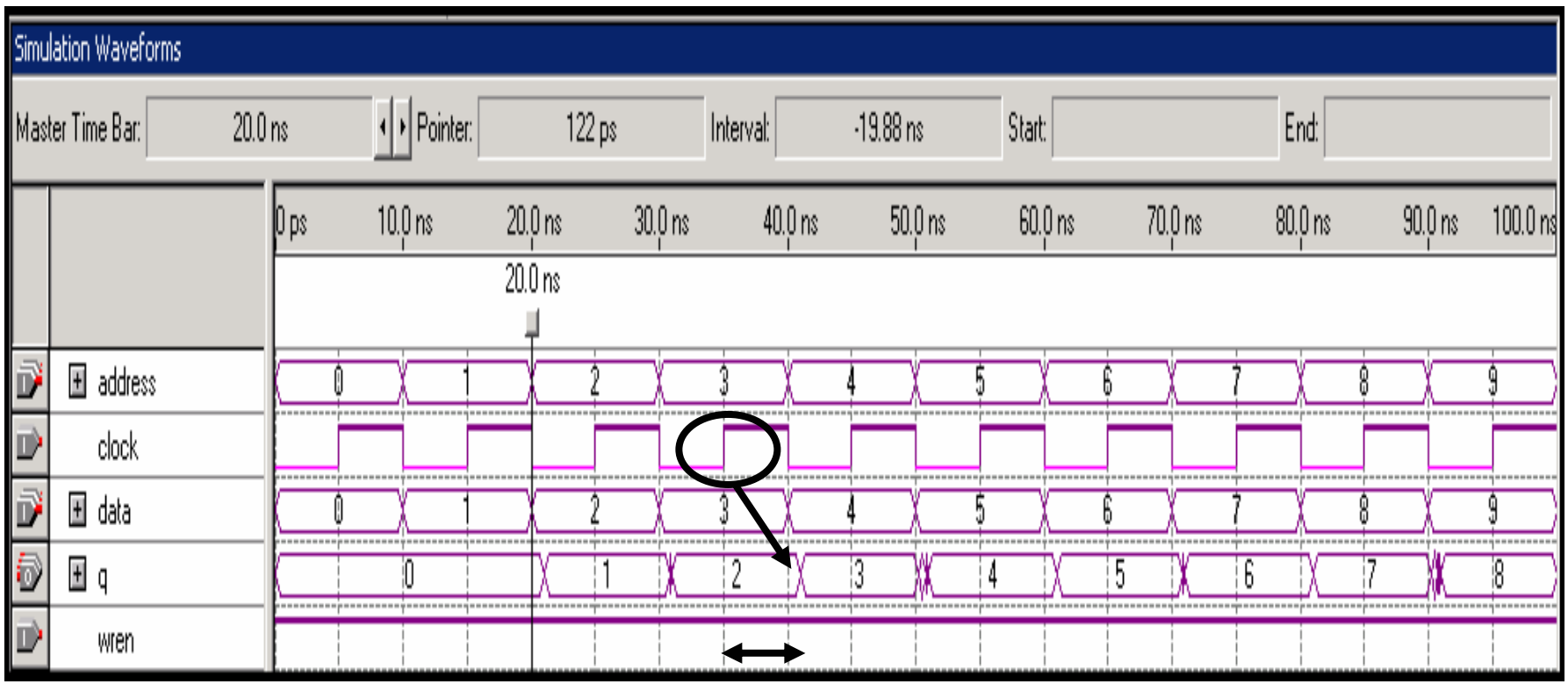
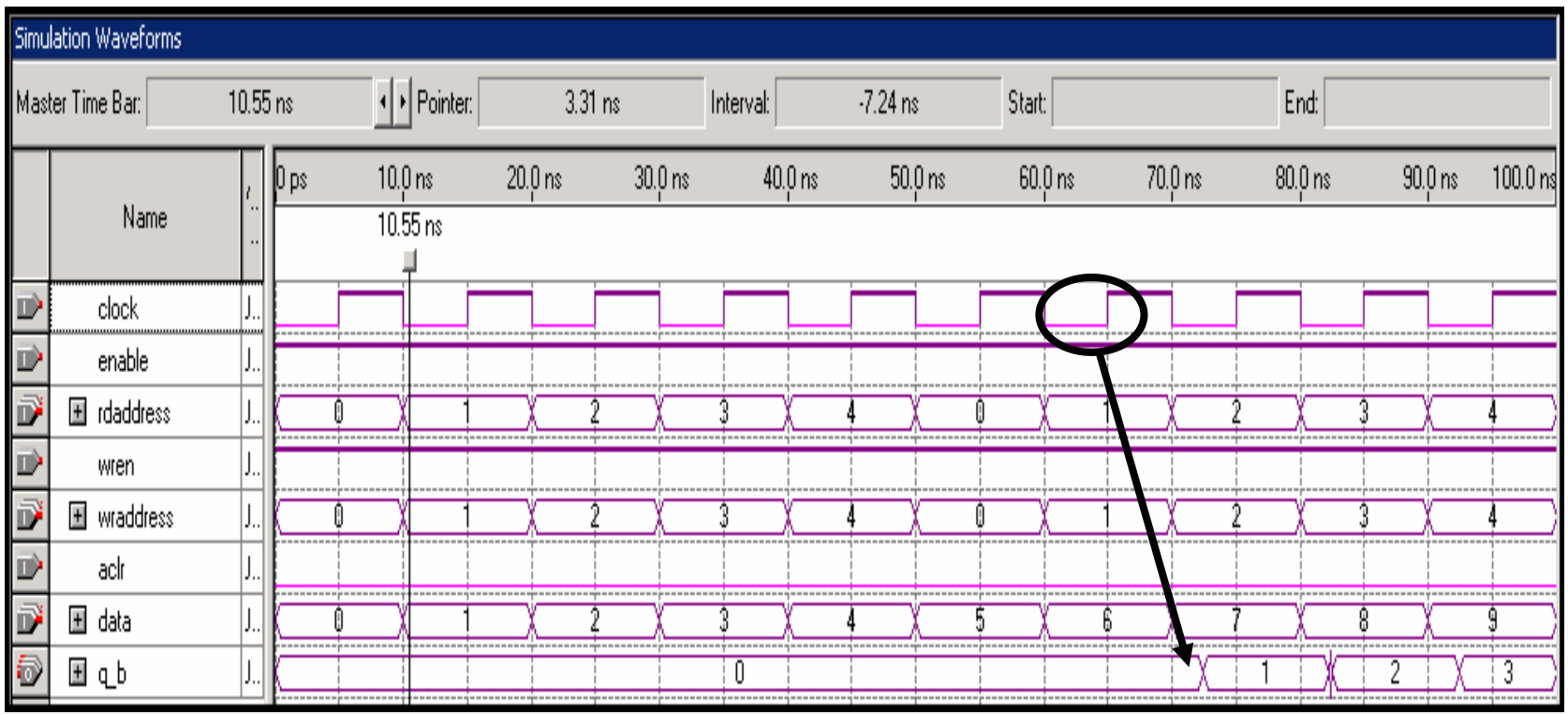
Read During Write

- Stratix Single-Port (Timing Simulation)
  - Unregistered Outputs



Read During Write

- Stratix Simple Dual-Port (Timing Simulation)
  - Unregistered Outputs



Stratix vs. Virtex-II

Stratix			Virtex-II		
Device	LEs	Kbits	Device	LEs	Kbits
			XC2V40	512	72
			XC2V80	1,024	144
			XC2V250	3,072	432
			XC2V500	6,144	576
EP1S10	10,570	899	XC2V1000	10,240	720
			XC2V1500	15,360	864
EP1S20	18,460	1,630	XC2V2000	21,504	1,008
EP1S25	25,660	1,899	XC2V3000	28,672	1,728
EP1S30	32,470	3,239			
EP1S40	41,250	3,344	XC2V4000	46,080	2,160
EP1S60	57,120	5,093			
			XC2V6000	67,584	2,592
EP1S80	79,040	7,253			
EP1S120	114,140	9,881	XC2V8000	93,184	3,026

Over 3X More Memory than Virtex-II

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Cyclone vs. Spartan-IIE

Spartan-IIE					Cyclone				
Device	Equivalent LEs	RAM Blocks	RAM Kbits	User I/O	Device	Equivalent LEs	RAM Blocks	RAM Kbits	User I/O
XC2S50E	1,536	8	32	182					
XC2S100E	2,400	10	40	202					
XC2S150E	3,456	12	48	263	EP1C3	2,910	13	58	104
XC2S200E	4,704	14	56	289	EP1C4	4,000	17	76	301
XC2S300E	6,144	16	64	329	EP1C6	5,980	20	90	185
XC2S400E	9,600	40	160	410					
XC2S600E	13,824	72	288	514	EP1C12	12,060	52	234	249
					EP1C20	20,060	64	288	301

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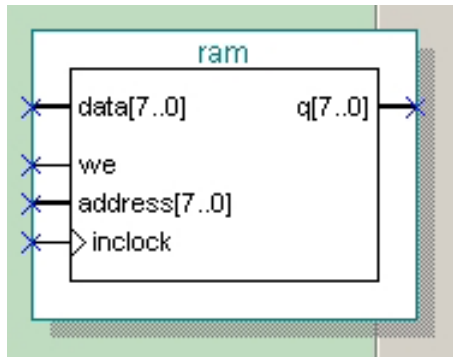
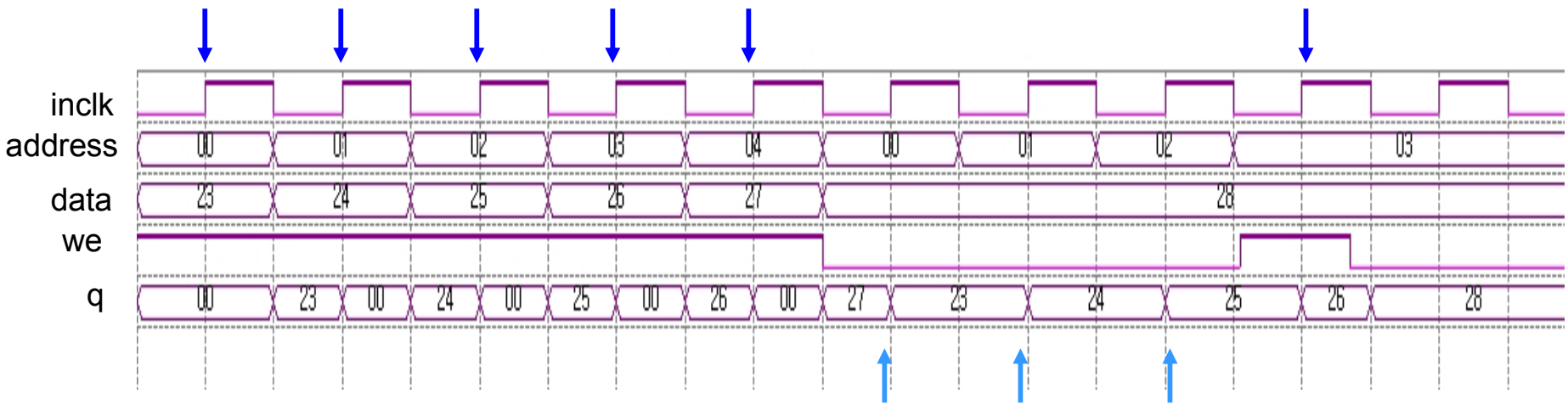
Sync. Single Port RAM (1)

- 256x8 size
- we = 1 : write / we = 0 : read
- Used Non – Registered Q output
- Inclock is 100MHz





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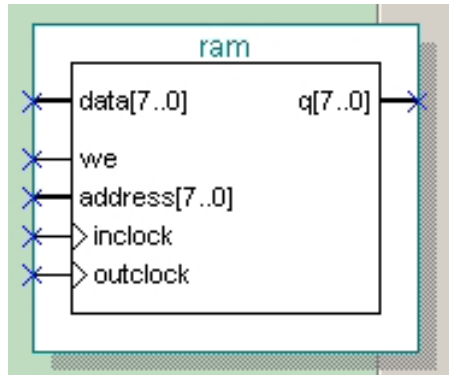
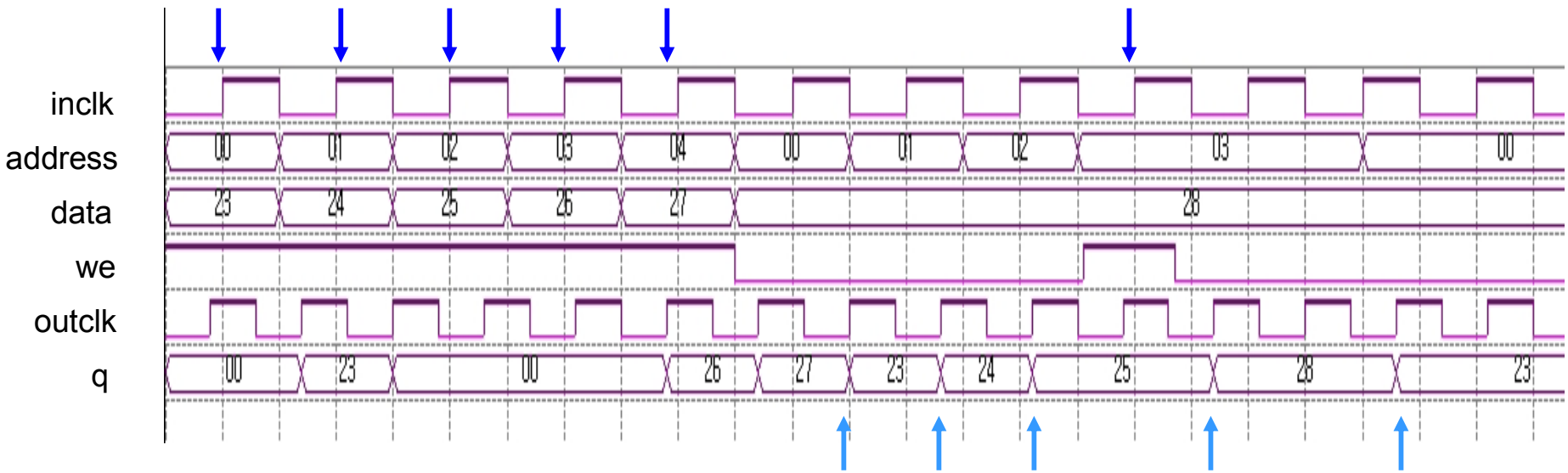
Sync. Single Port RAM (2)

- 256x8 size (1 ESB)
- Used Registerd Q output
- inclock is 100MHz and outclock is 125MHz





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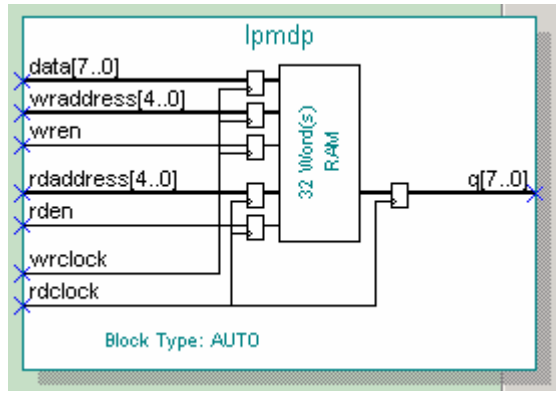
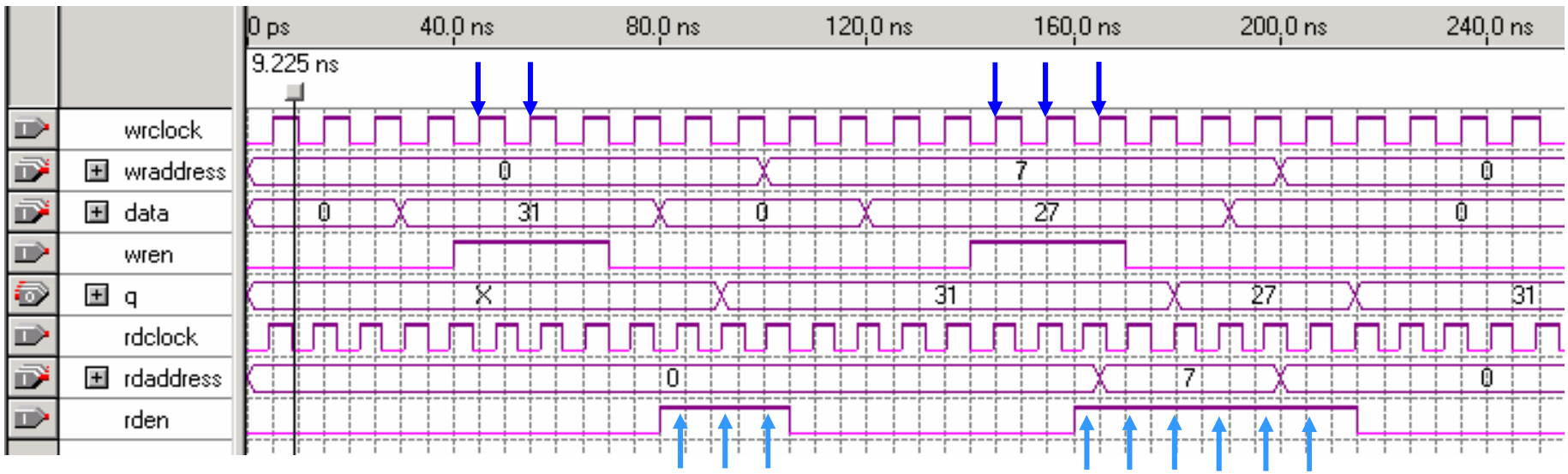
Sync. Separate Read/Write RAM

- 256x8 size
- Input read / write clock seperately
- Registered Q output
- wrclock 100MHz, rdclock 125MHz





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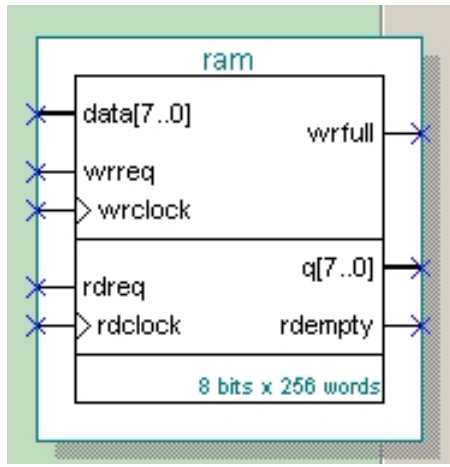
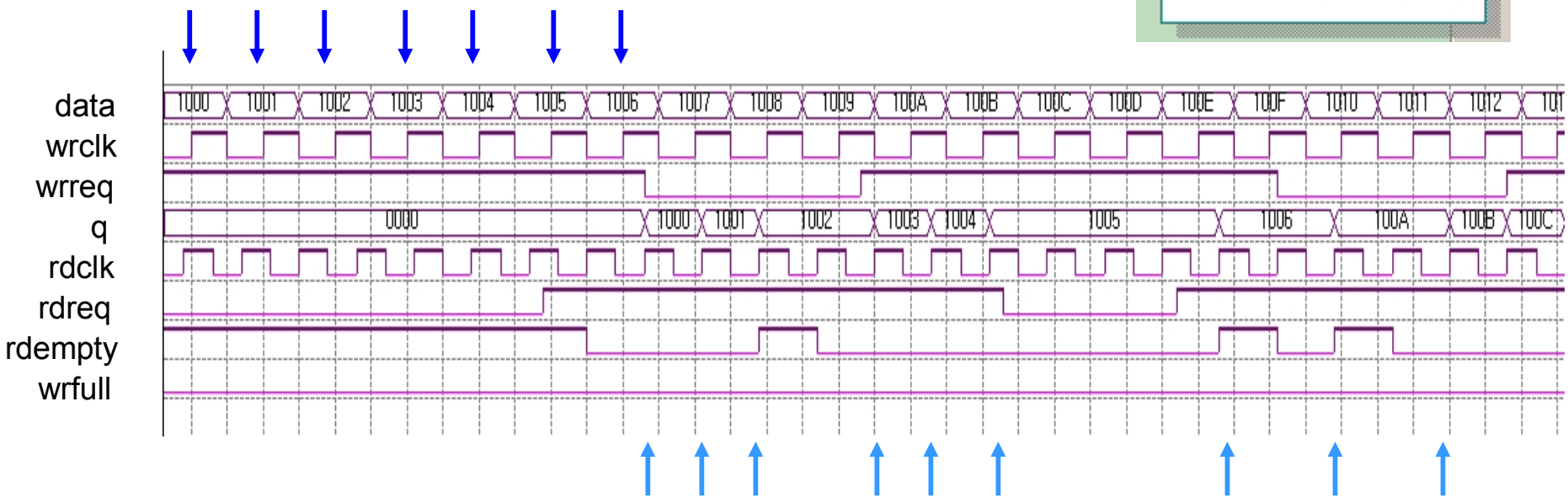
FIFO : LPM_FIFO

- 256x8 size (1 ESB)
- wrclk is 100MHz and rdclk is 125MHz





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