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MegaMACs to TeraMACs: Implementing Digital Signal Processing (DSP) in FPGAs

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Agenda

- DSP Applications & Signal Processing Requirements
- Altera FPGA & CPLD DSP Capabilities
- Development Tools & Intellectual Property (IP) Cores
- FPGA for Control & Dataflow Processing
- Utilizing Nios® II for DSP Applications
- Examples

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DSP Applications & Signal Processing Requirements

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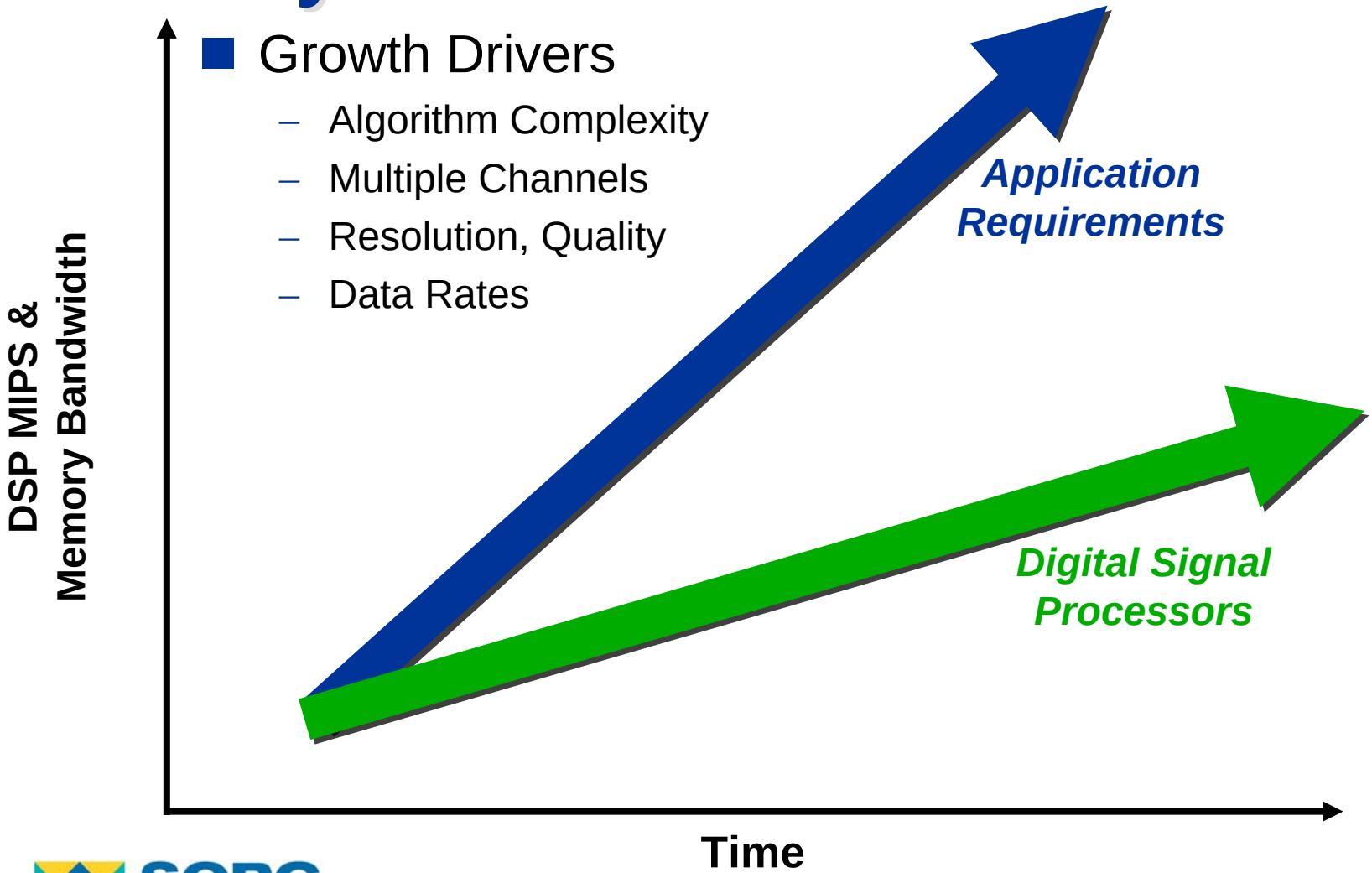
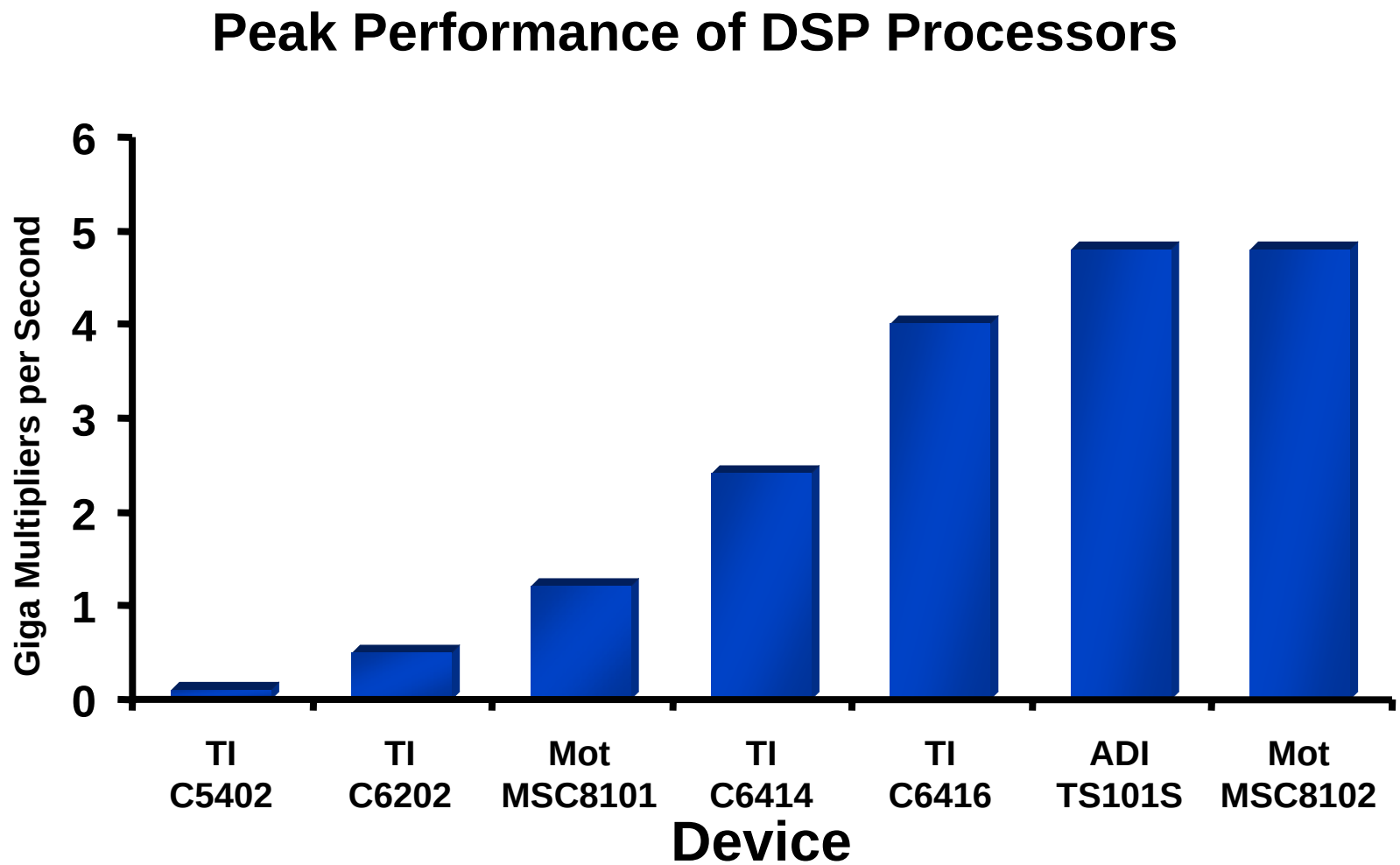
Growing Demand for MIPS & Memory Bandwidth



DSP Processors Multiplier Bandwidth



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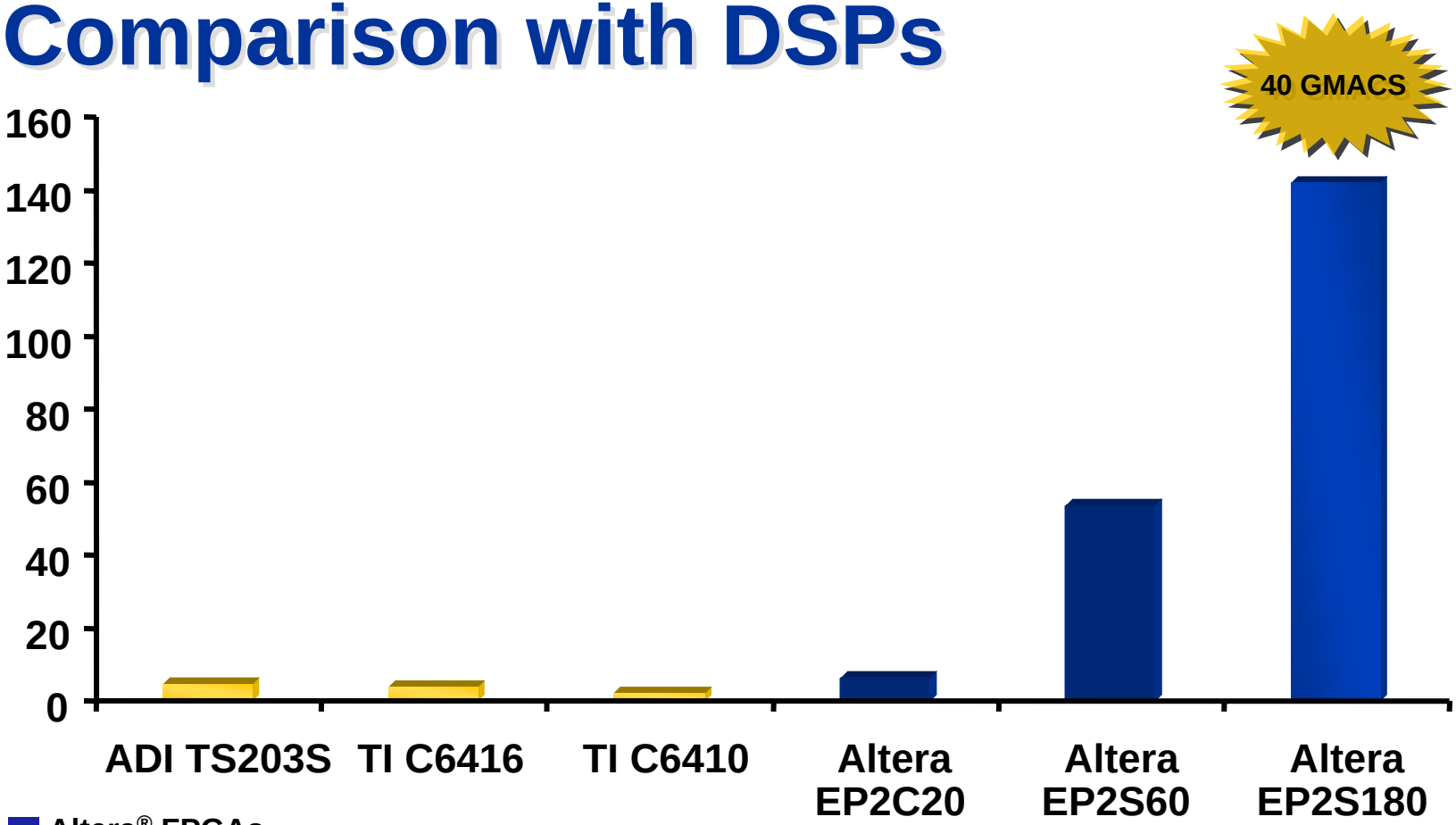
Embedded Multiplier Comparison with DSPs



Giga Multiplies/s = Clock Frequency * # of 16x16 Hardware Multiplies

Note: Additional Multiplier Bandwidth Available Using Memory & Logic Elements (LEs)
Stratix® II Bandwidth > 600 Giga Multiplies per Second

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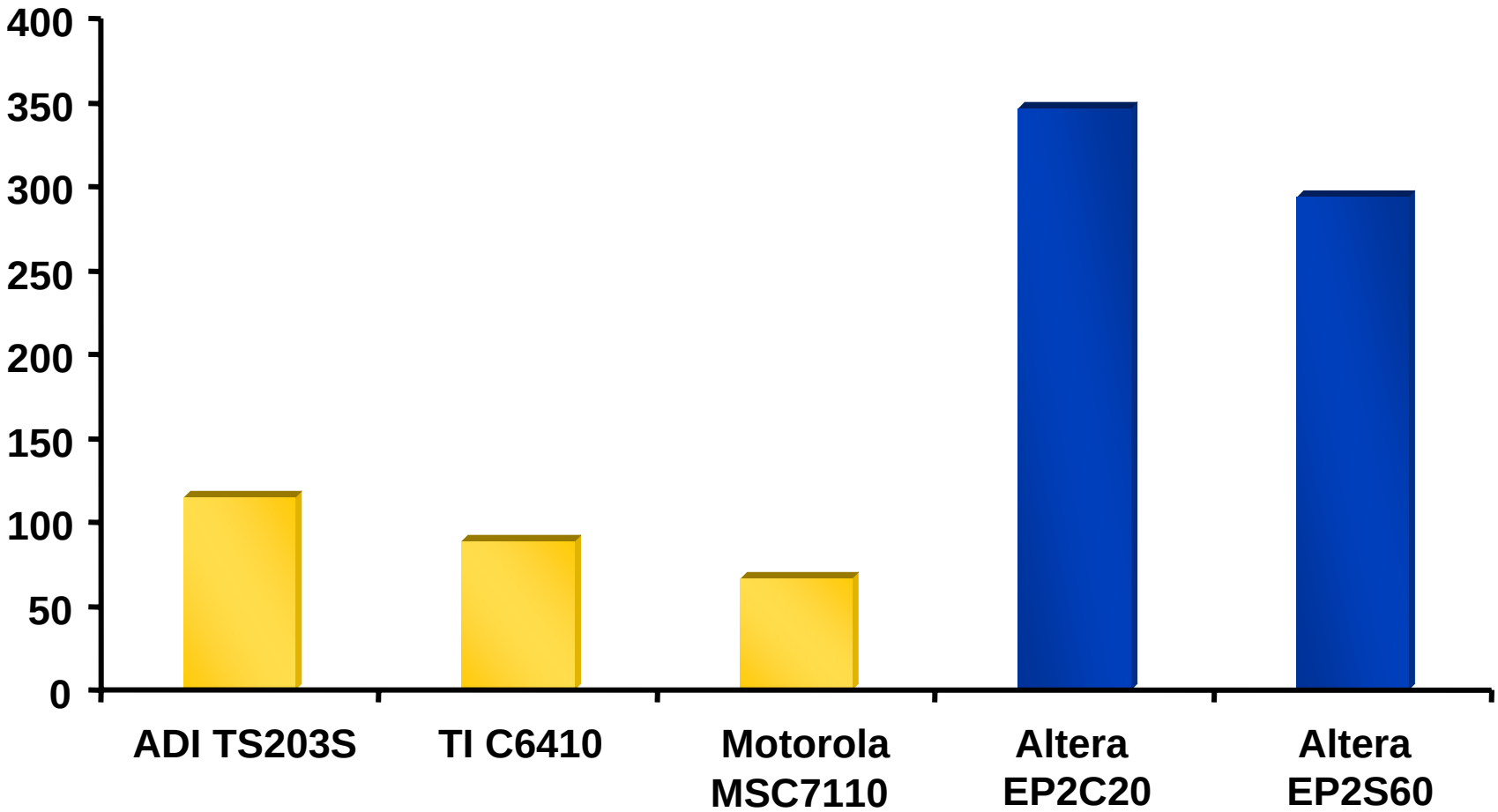
Embedded Mega Multiplies/$



Based on the following 10k List Prices: TS203S ($35), C6410 ($18), MSC7110 ($12), EP2C20 ($15), EP2S60 ($150)

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BDTI Benchmark

- Berkeley Design Technology, Inc. (www.BDTI.com)
  Leading Independent DSP Benchmarking Company
- Includes Results from New BDTI Benchmarks
  - New Telecom-Oriented, Single-Channel Receiver Benchmark
  - Report Released September 2002

"... Looking at [BDTI's new telecom benchmark] results, it appears that even a mid-range DSP-enhanced FPGA from Altera's Stratix line will be able to handle more than an order-of-magnitude more channels than the MSC8101 for a similar projected per-chip price..."

FPGA/DSP Blend Tackles Telecom Apps
In EE Times, Jul 1, 2002
Jennifer Eyre, Senior DSP Analyst, Berkeley Design Technology Inc.
http://www.eetimes.com/story/OEG20020628S0097

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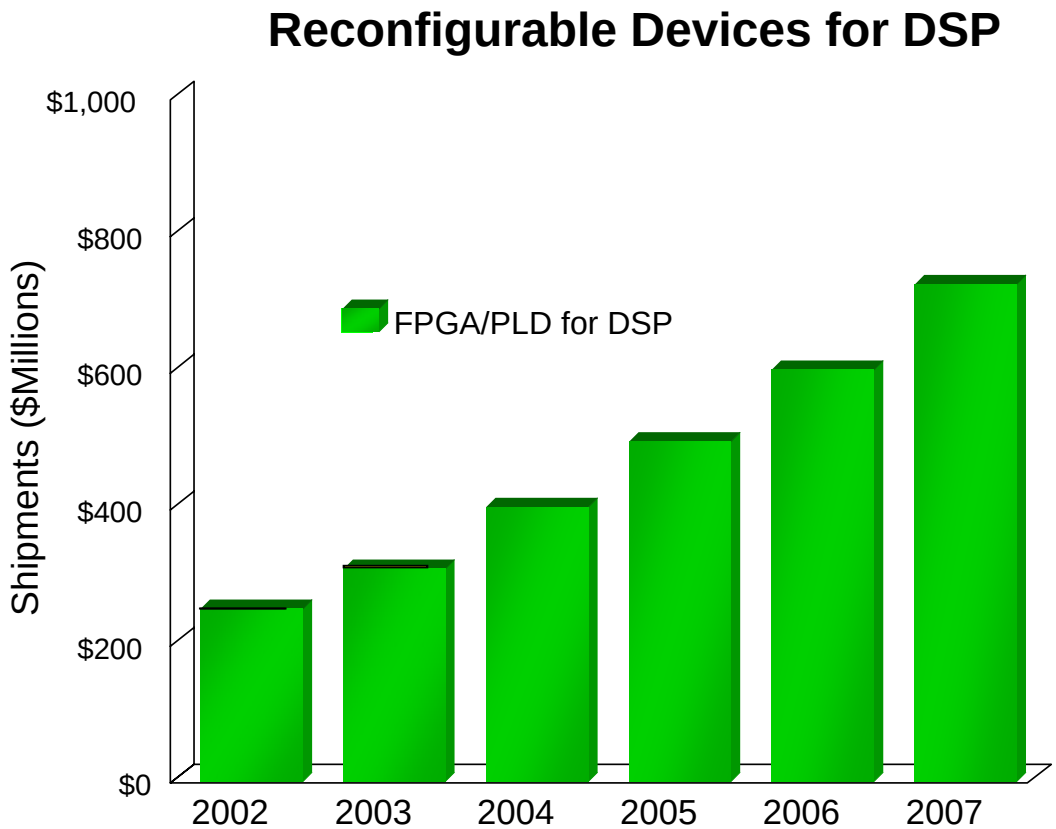
FPGA Growth for DSP: 26% Compound Annual Growth Rate



Mix Between Communications & Video & Image Processing

Source: 2004 Forward Concepts

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Altera's Industry-Leading Components

The Lowest-Cost CPLDs Ever

The Lowest-Cost FPGAs Ever

The Biggest & Fastest FPGAs Ever

The Industry's Only Low-Cost, Comprehensive ASIC Alternative

Altera's Components Applied To DSP

Small DSP Tasks Encryption,
Forward-Error Correction (FEC),
Small Filtering

Low-Cost DSP Performance
Replaces 1 or More DSP Processors

Industry's Highest Performance
Programmable DSP Processing
Replaces Arrays of DSPs & ASICs

DSP Structured ASIC Solution

Cyclone II Family Overview

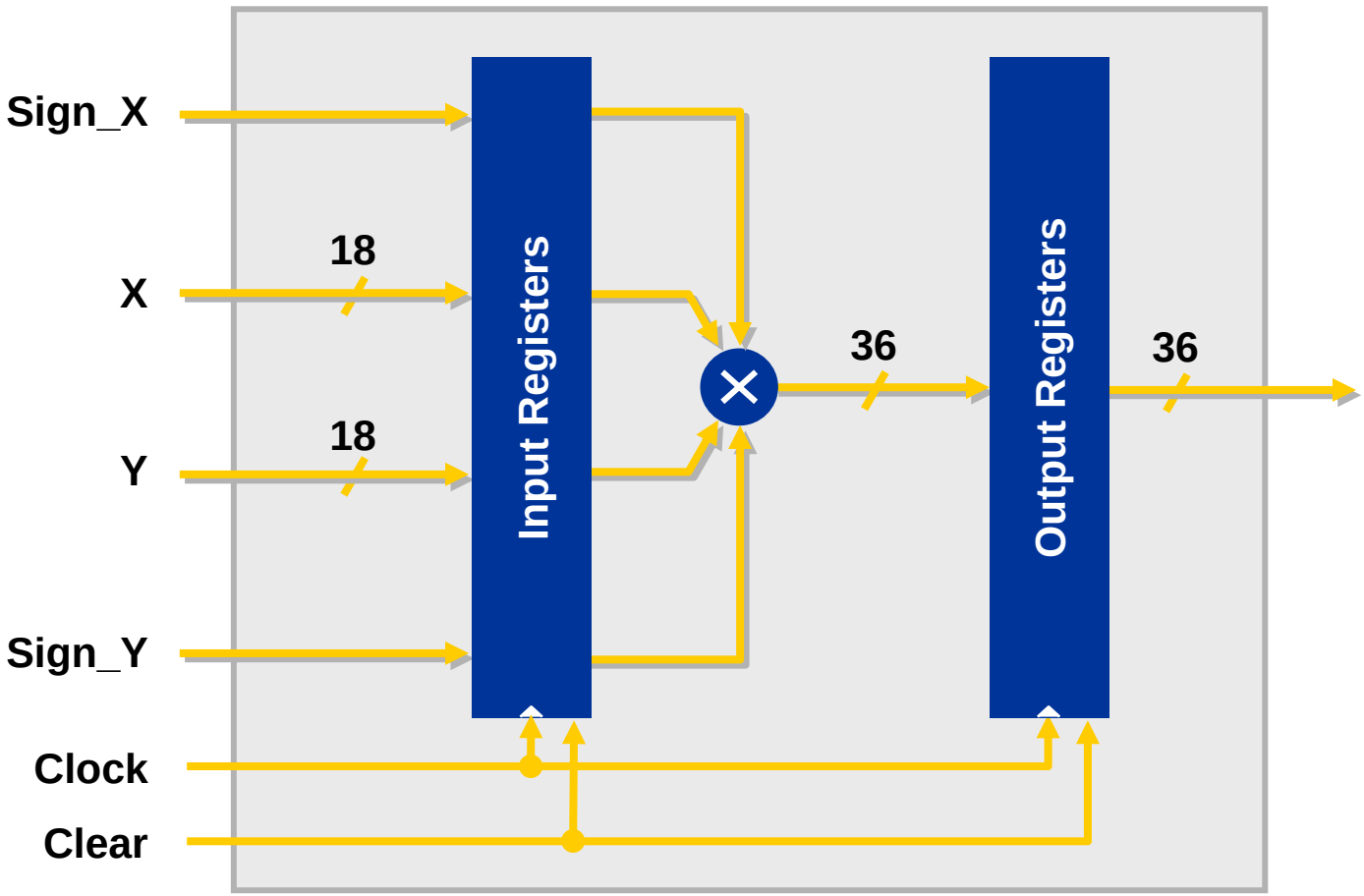
3.2 to 37.5 GMACS

EP2C35 Device Samples Available in Q1'05

Device	Logic Elements (LEs)	M4K Memory Blocks	Total Memory Bits	18x18 Embedded Multipliers	PLLs	Maximum User I/O Pins
EP2C5	4,608	26	119,808	13	2	142
EP2C8	8,256	36	165,888	18	2	182
EP2C20	18,752	52	239,616	26	4	315
EP2C35	33,216	105	483,840	35	4	475
EP2C50	50,528	129	594,432	86	4	450
EP2C70	68,416	250	1,152,000	150	4	622

Note: All Densities Will be Offered in All Speed Grades (-6, -7, -8). -6 is the Fastest Speed Grade.

Cyclone II Embedded Multiplier



250-MHz Performance

Note: Fastest Speed Grade with Registers Activated in 18x18 or 9x9 Mode

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Stratix II Device Family

Device	ALMs(1)	Equivalent LEs	M512 RAM	M4K RAM	M-RAM	Total Memory Bits	18x18 Multipliers(2)	PLLs(3)	Avail-ability
EP2S15	6,240	15,600	104	78	0	419,328	48	6	Q4'04
EP2S30	13,552	33,880	202	144	1	1,369,728	64	6	Q4'04
EP2S60	24,176	60,440	329	255	2	2,544,192	144	12	*Now!*
EP2S90	36,384	90,960	488	408	4	4,520,448	192	12	Q4'04
EP2S130	53,016	132,540	699	609	6	6,747,840	252	12	Q3'04
EP2S180	71,760	179,400	930	768	9	9,383,040	384	12	Q4'04

(1) ALMs: Adaptive Logic Modules.
(2) Does Not Include Soft Multipliers Implemented in Memory Blocks.
(3) Includes Enhanced & Fast PLLs.

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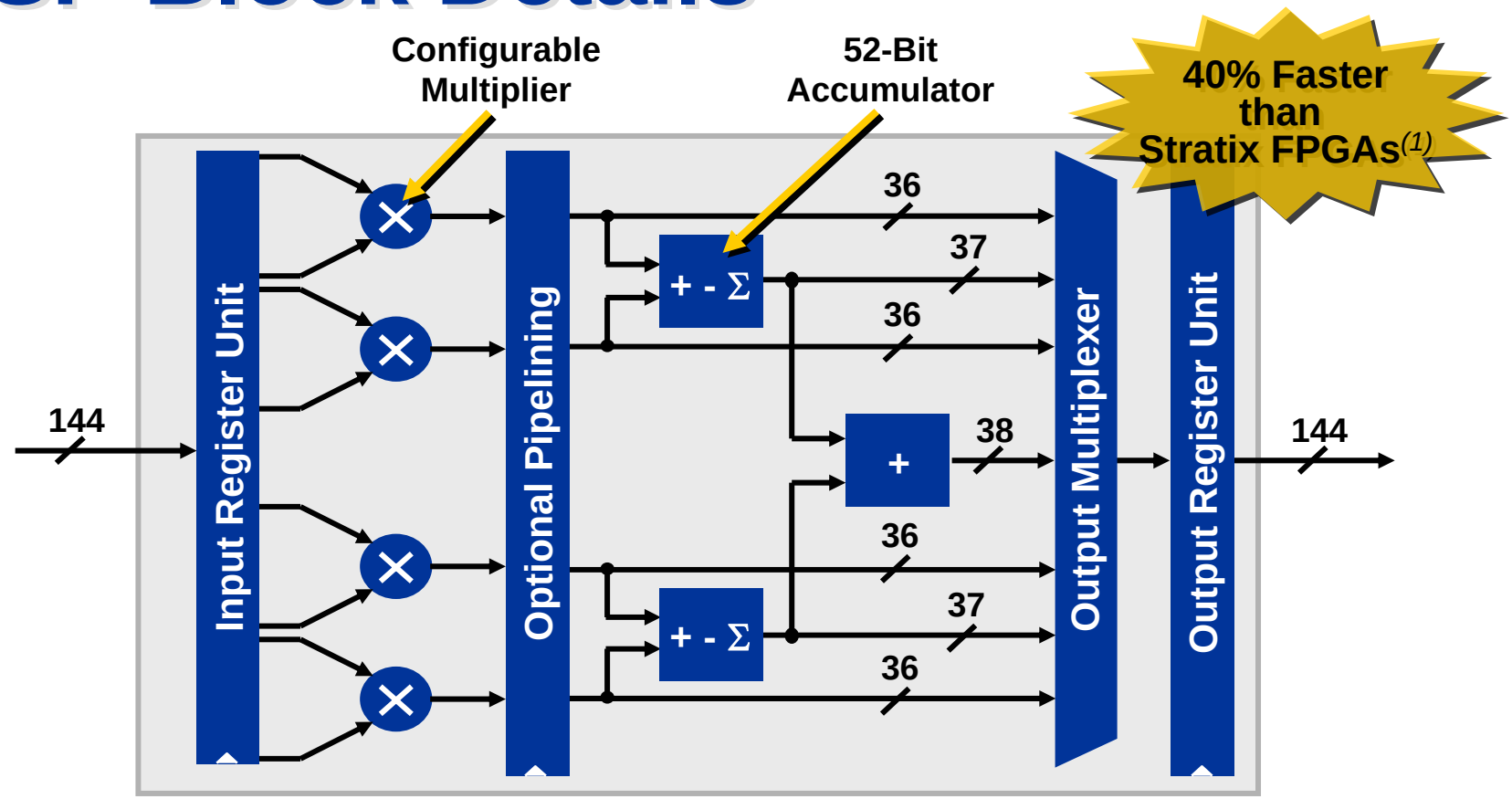
DSP Block Details



Includes Rounding & Saturation Support

(1) 370-MHz Performance Target for Registered 18x18 & 9x9 Modes.

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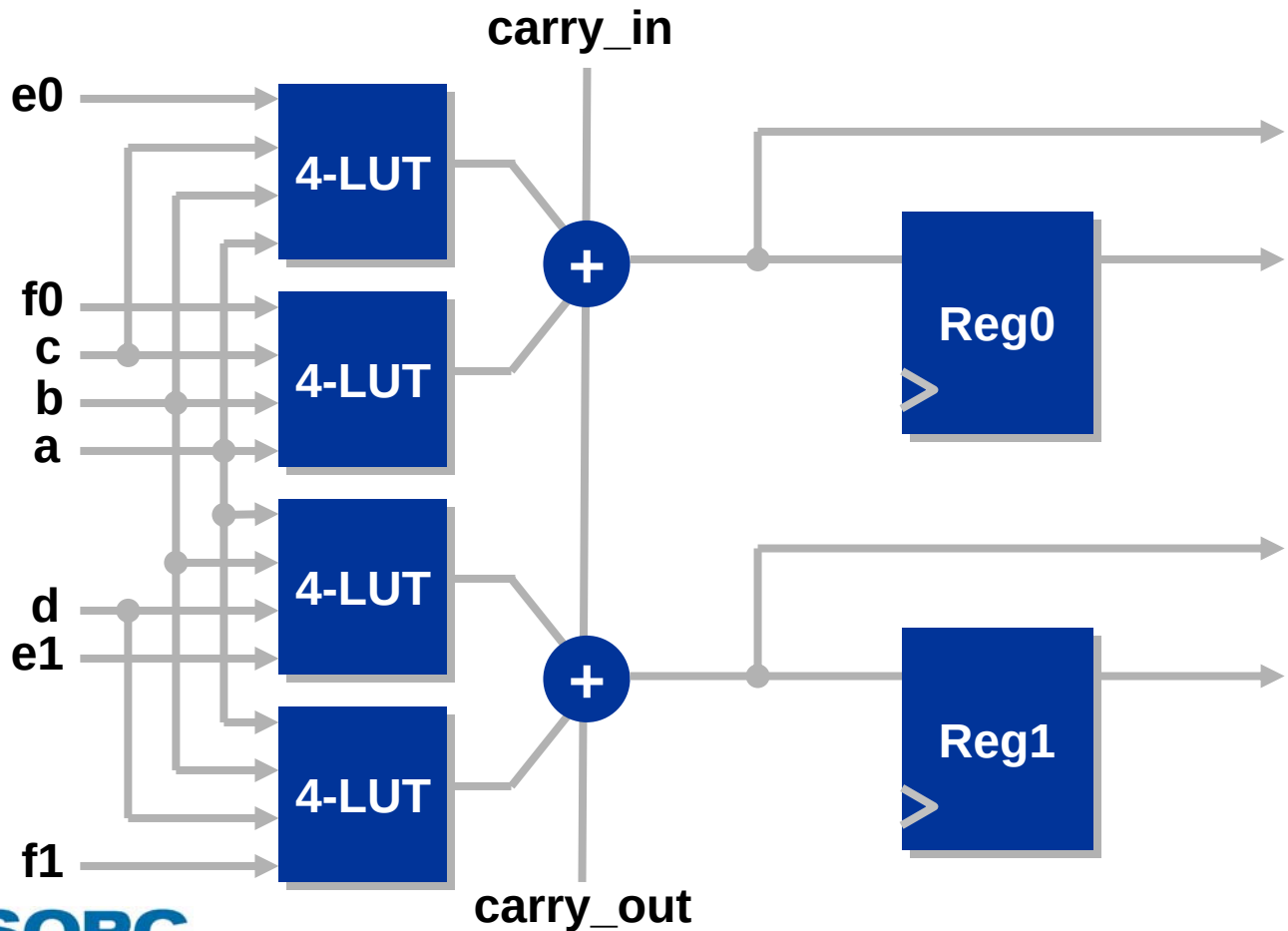
ALM (LE) Arithmetic Mode

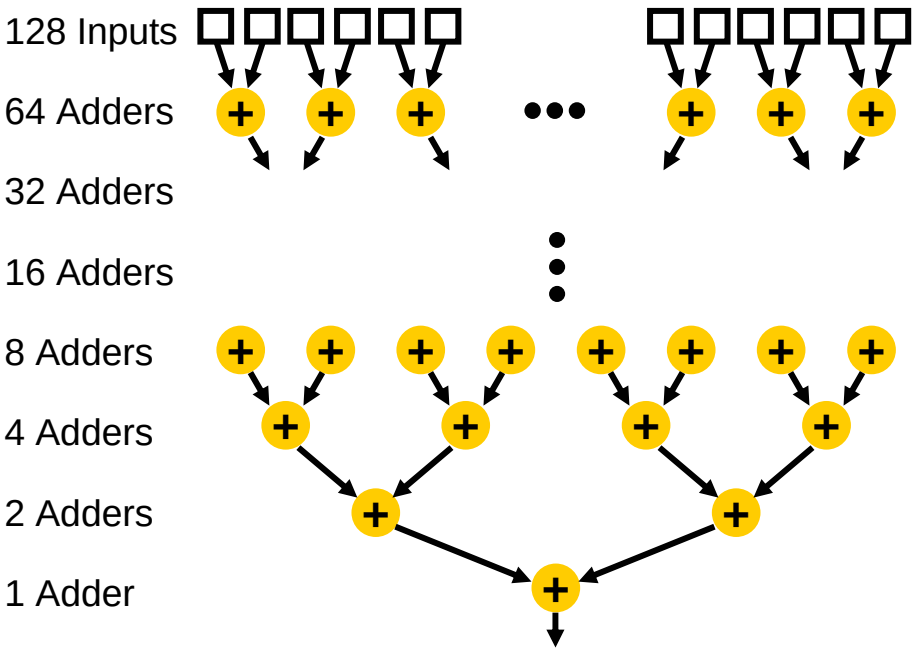
- Two Dedicated Adders per ALM



Stratix II Adder Tree Support

Stratix Adder Tree Implementation

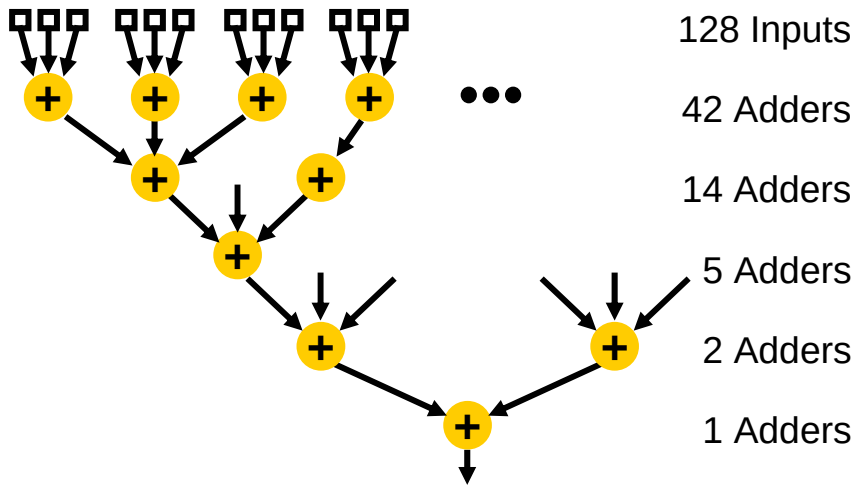
Add 2 Bits per LE



127 Adders, 7 Levels
~8,600 LEs

Stratix II Adder Tree Implementation

Two 3-Bit Adds per ALM



64 Adders, 5 Levels
~2,500 ALMs

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DSP Development Tools & IP Cores

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DSP IP Examples for Altera FPGAs

Error Correction

- Reed Solomon Compiler
- Viterbi Compiler
- Turbo Compiler

Encryption

- RSA
- Rijndael
- IPSEC

Modulation

- J.83
- QPSK
- OFDM

Image Processing

- JPEG2000 Codec
- MPEG2 HD Decoder
- DCT

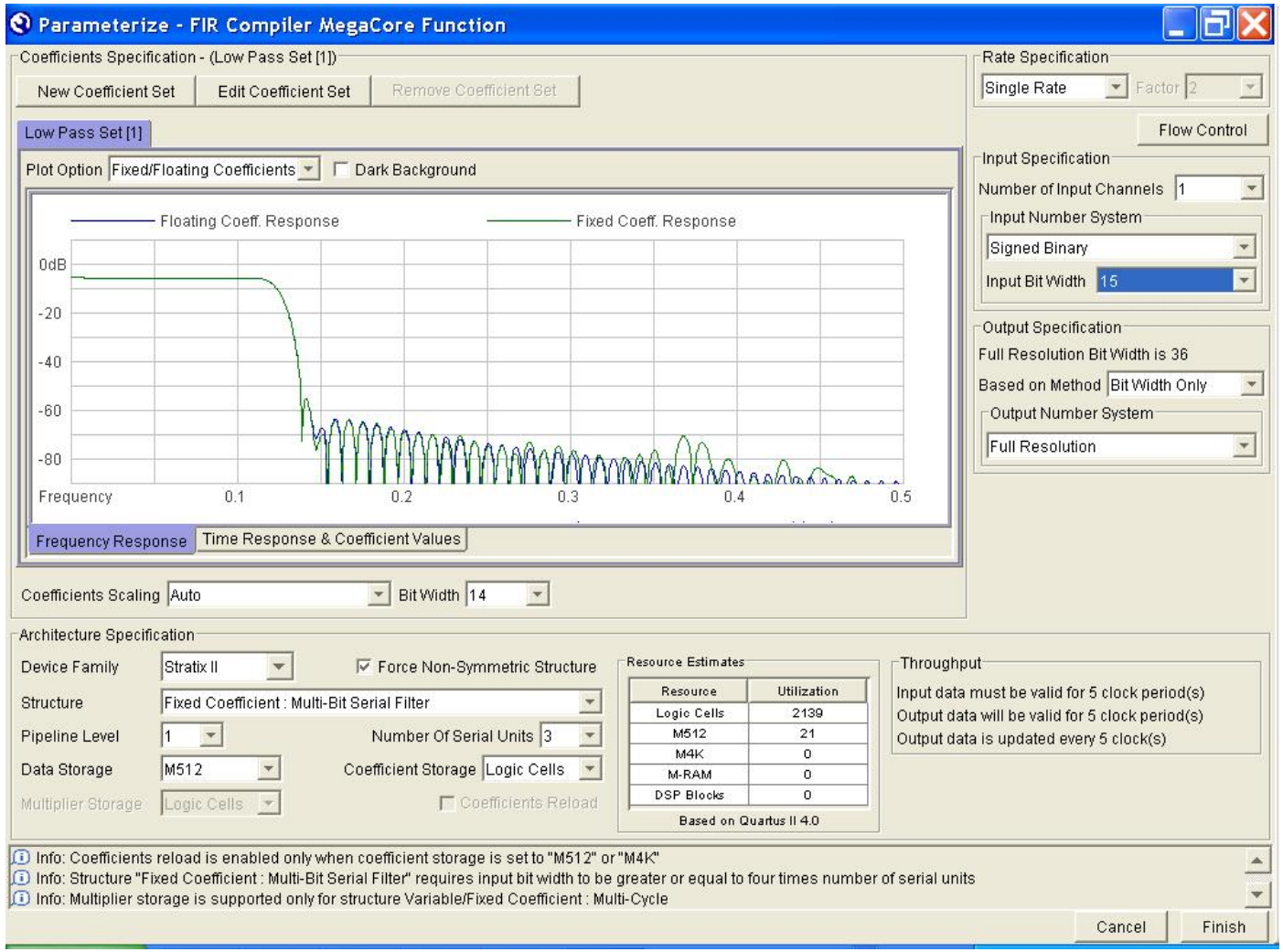
General

- FIR Filter Compiler
- FFT Compiler
- Floating Point Unit

Voice

- G.726
- G.711
- Tone Generation

DSP IP Example: FIR Compiler



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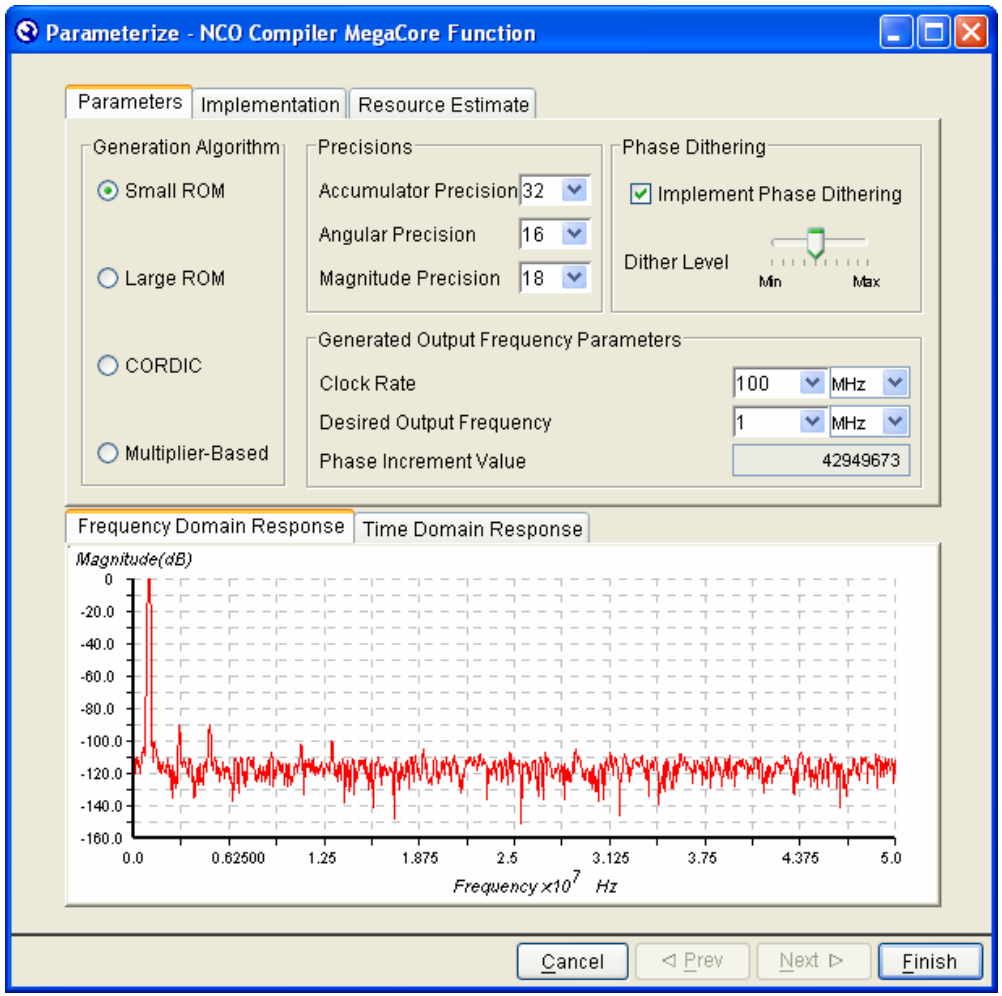
DSP IP Example: NCO Compiler



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DSP Builder Overview

DSP Builder

MATLAB® & SIMULINK®

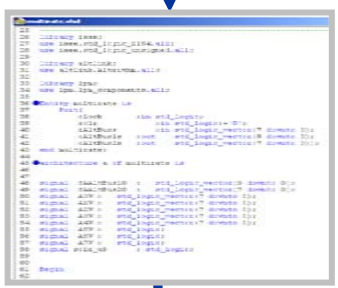
Creates HDL Code

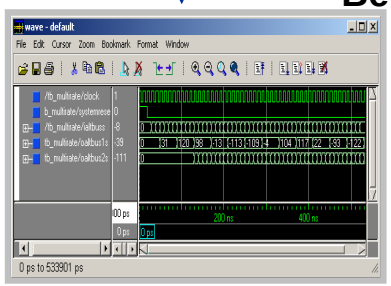
Creates Simulation Test Bench

Creates Processor Plug-In

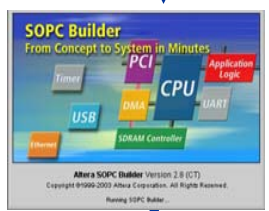
Downloads Design to Development Board

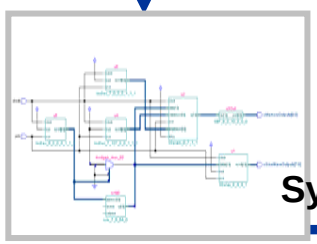
Verifies in Hardware





Model Technology
A MENTOR GRAPHICS COMPANY





HDL Synthesis

exemplar
A MENTOR GRAPHICS COMPANY

Synplicity

QUARTUS® II

QUARTUS® II

SignalTap® II

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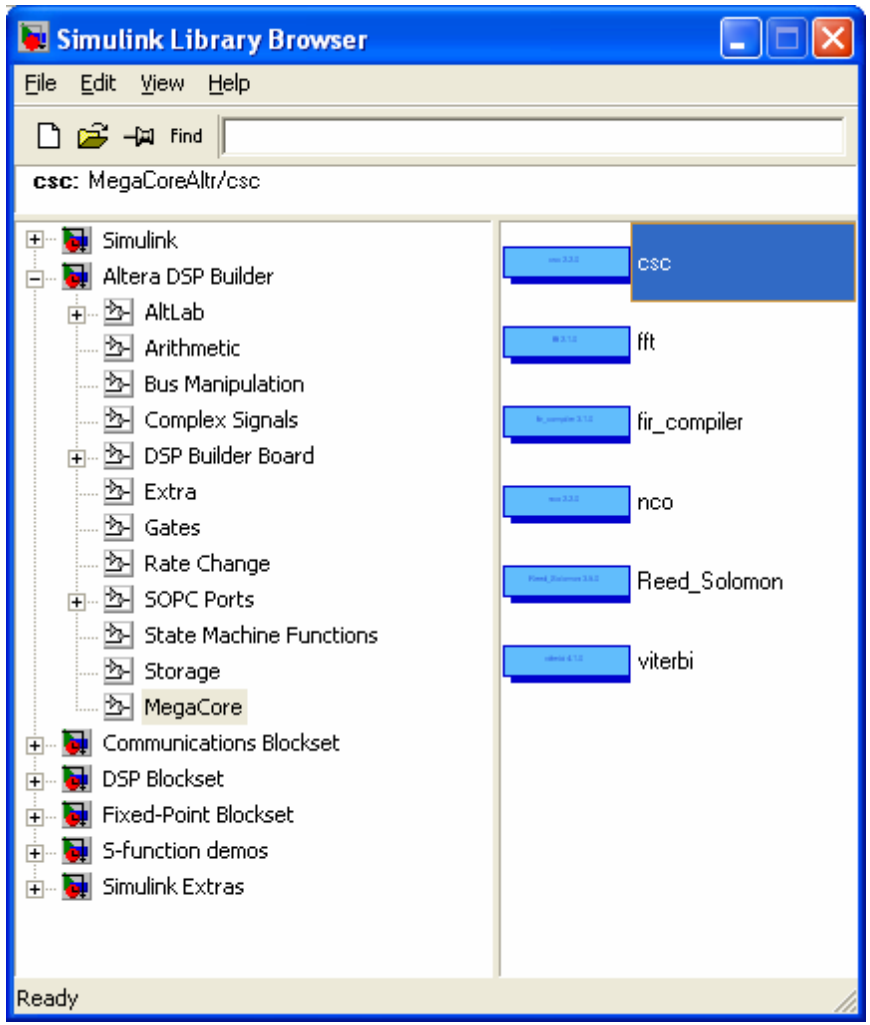
DSP Builder Library Components

- Arithmetic
- Bus Manipulation
- Complex Signals
- Logical Components
- SOPC Ports
- Storage
- MegaCore® IP
- Rate Change
- State Machine
- Altera Library
- DSP Board



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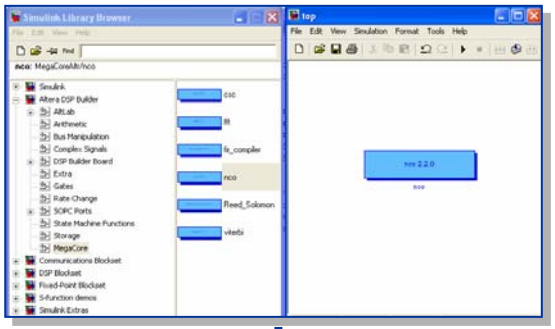
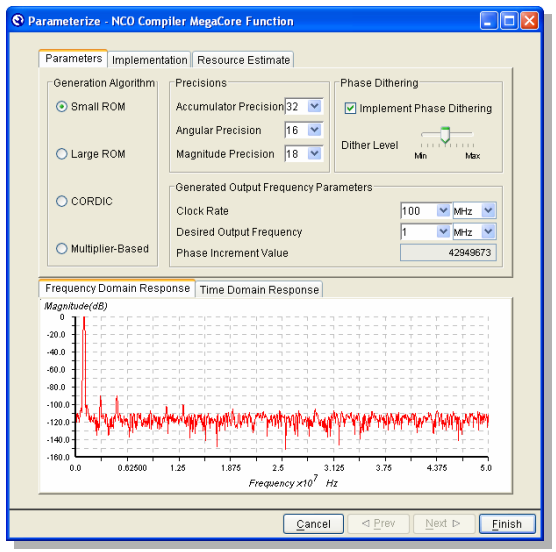
Adding IP to the Design

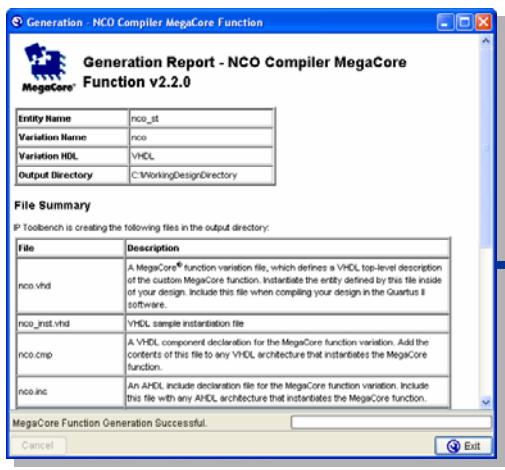


Configure

Parameterize



Generate



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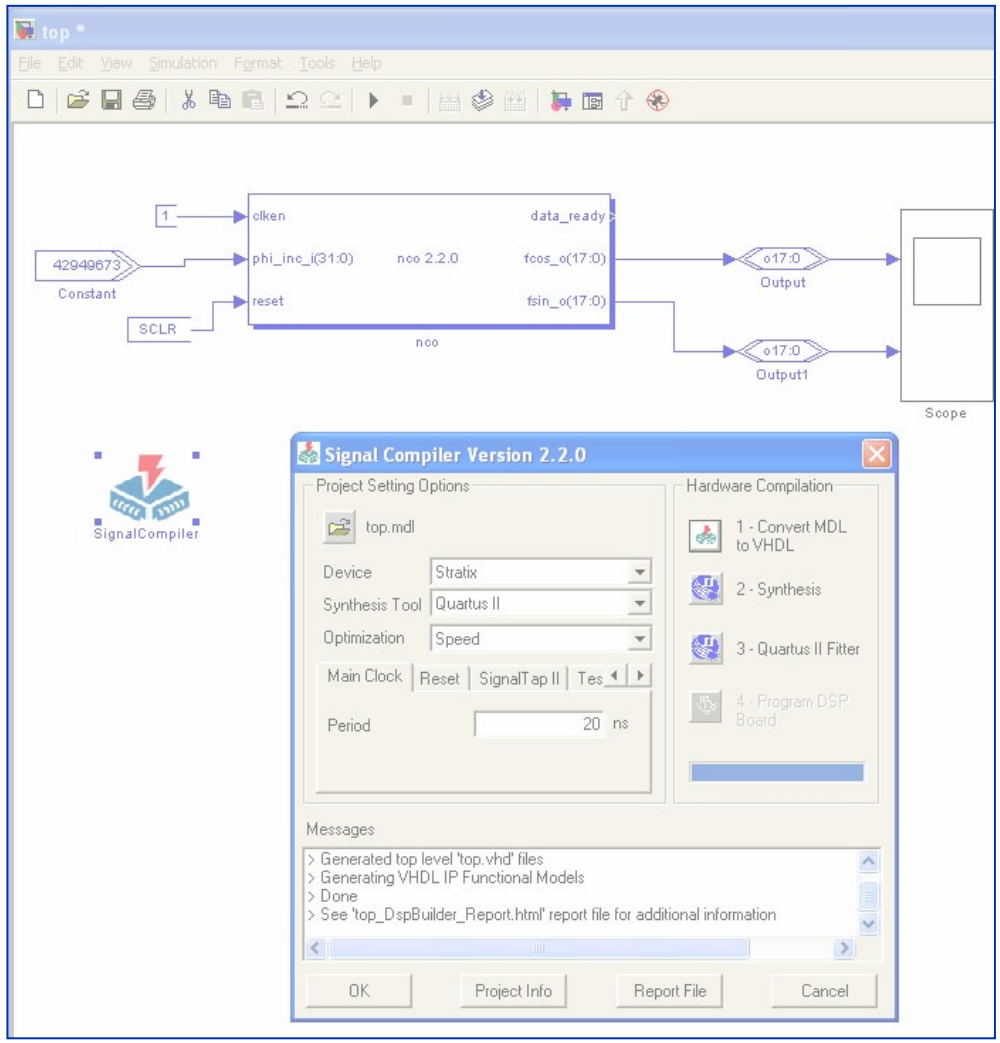
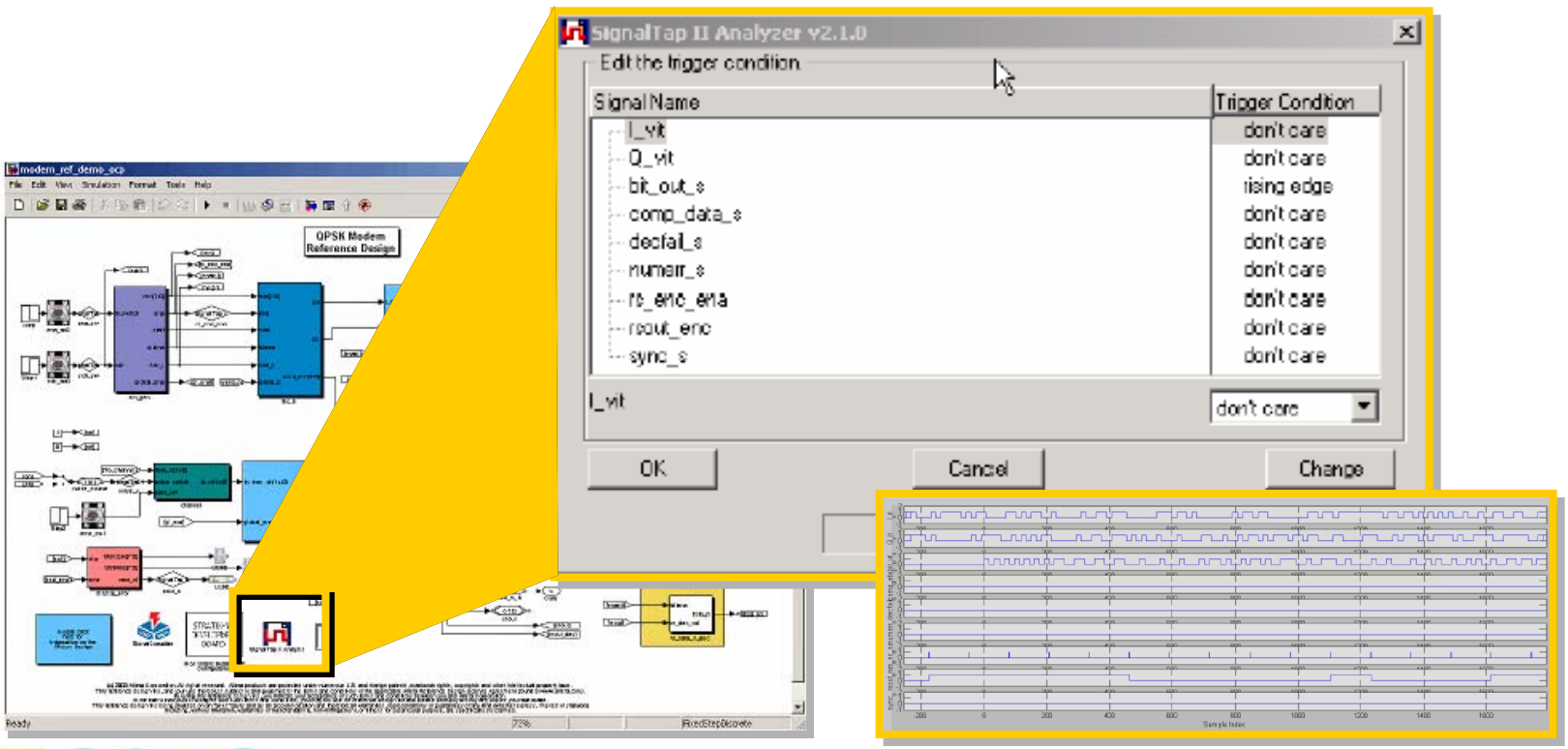
Hardware Implementation

- Support OpenCore® Plus Evaluation for IP Evaluation
- Signal Compiler Utility Can Program IP on Supported DSP Builder Board



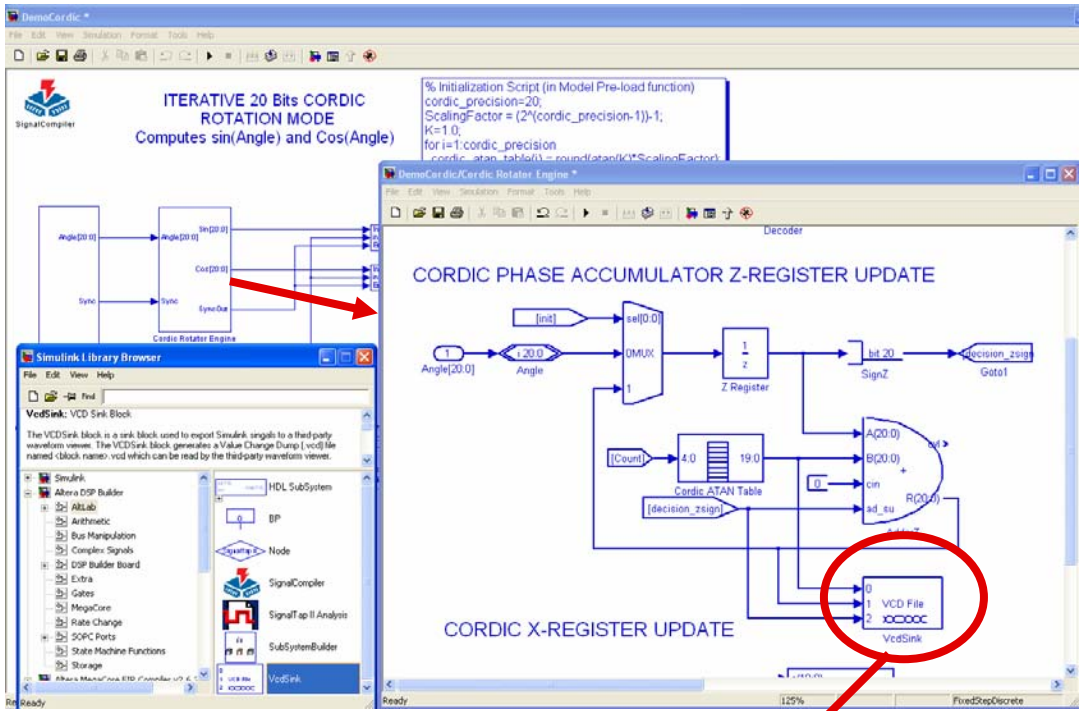
SignalTap II Logic Analyzer

- Interfaces to DSP Builder
- Captures Signal Activity from Internal Device Nodes
- Displays Captured Data in MATLAB/Simulink

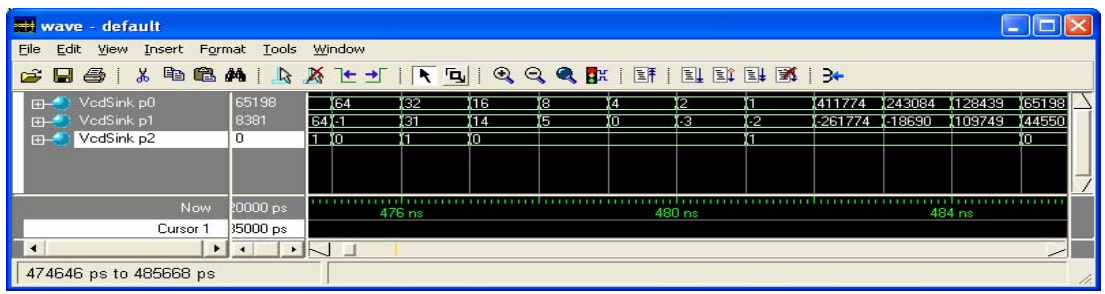


VCDSink Block

- Generates VCD Dump File to RTL Waveform Viewer & ModelSim® Tcl Script
- Provides Waveform Analysis for Internal Nodes



do VcdSink_vcd.tcl



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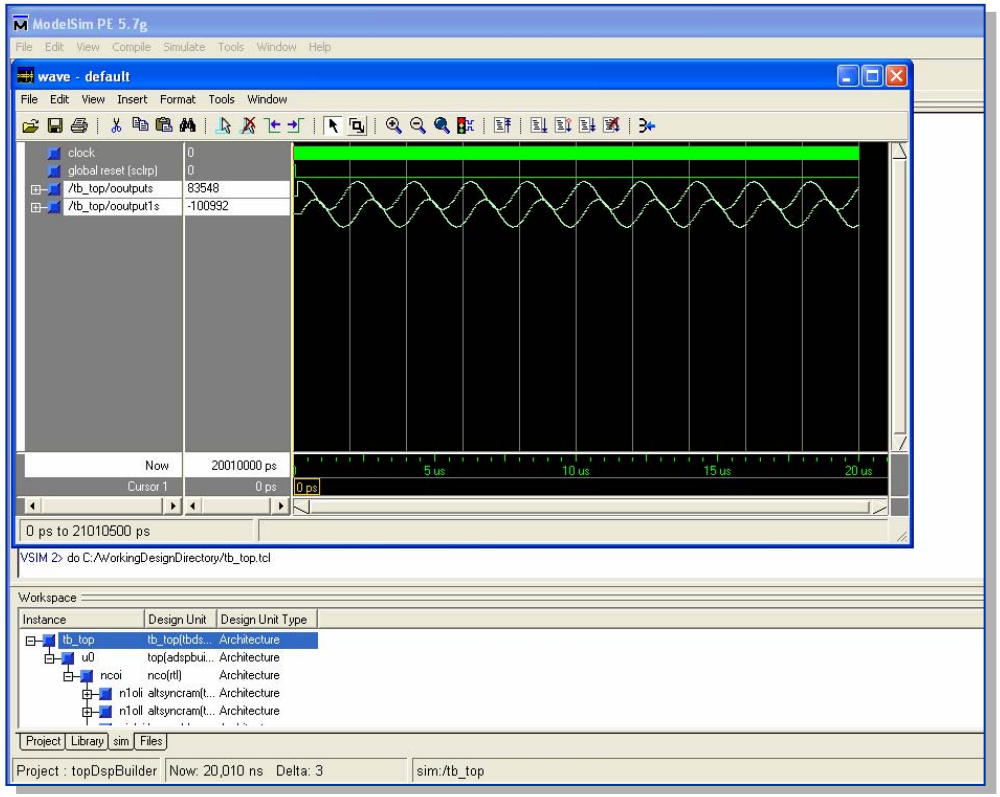
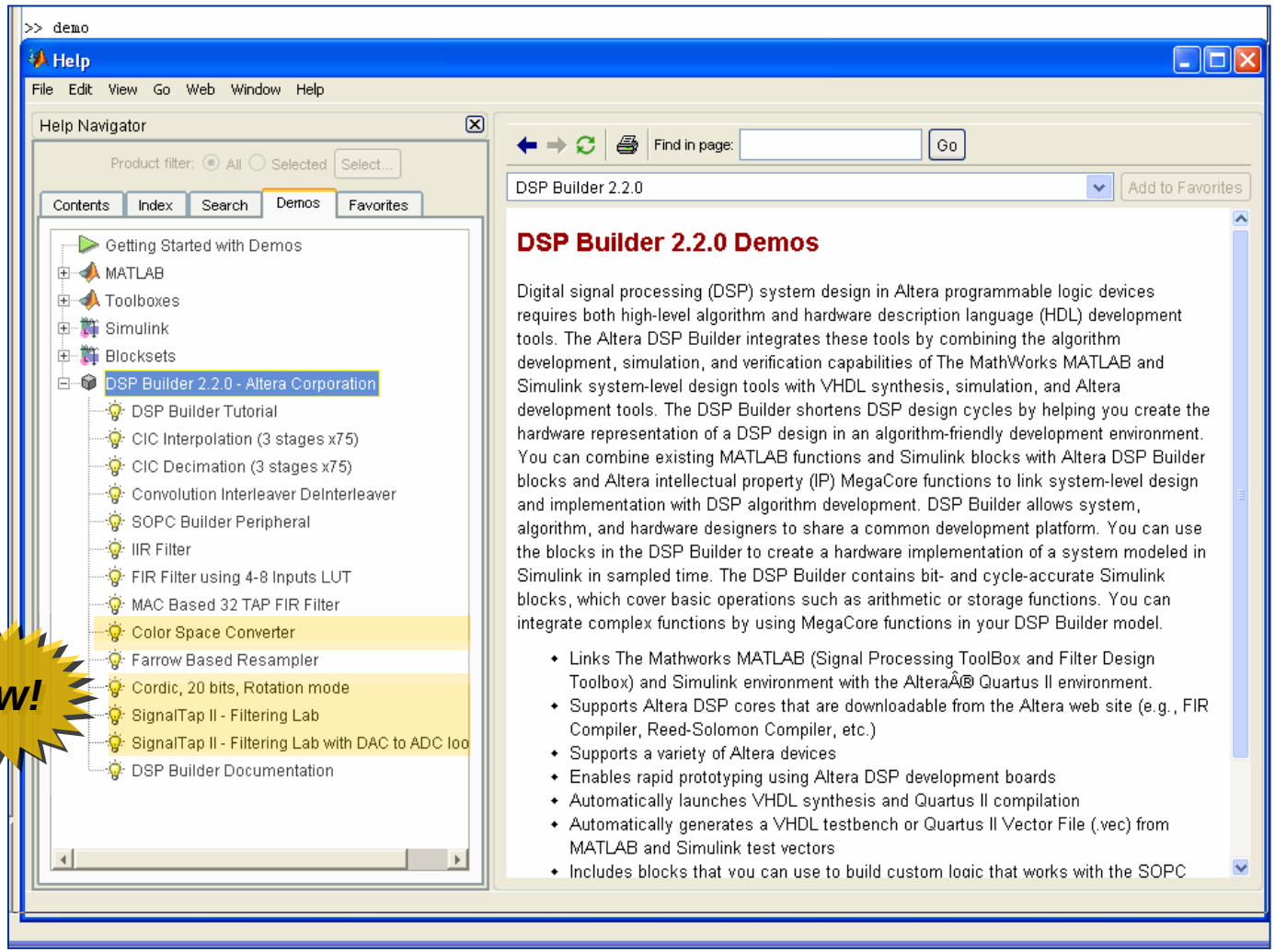
Hardware Simulation

- VHDL or Verilog Simulation of Simulink Design with IP
- Signal Compiler Generates Tcl Script to Automate MSIM Simulation
- Use IP Functional Model (.vho or .vo)



New Demos



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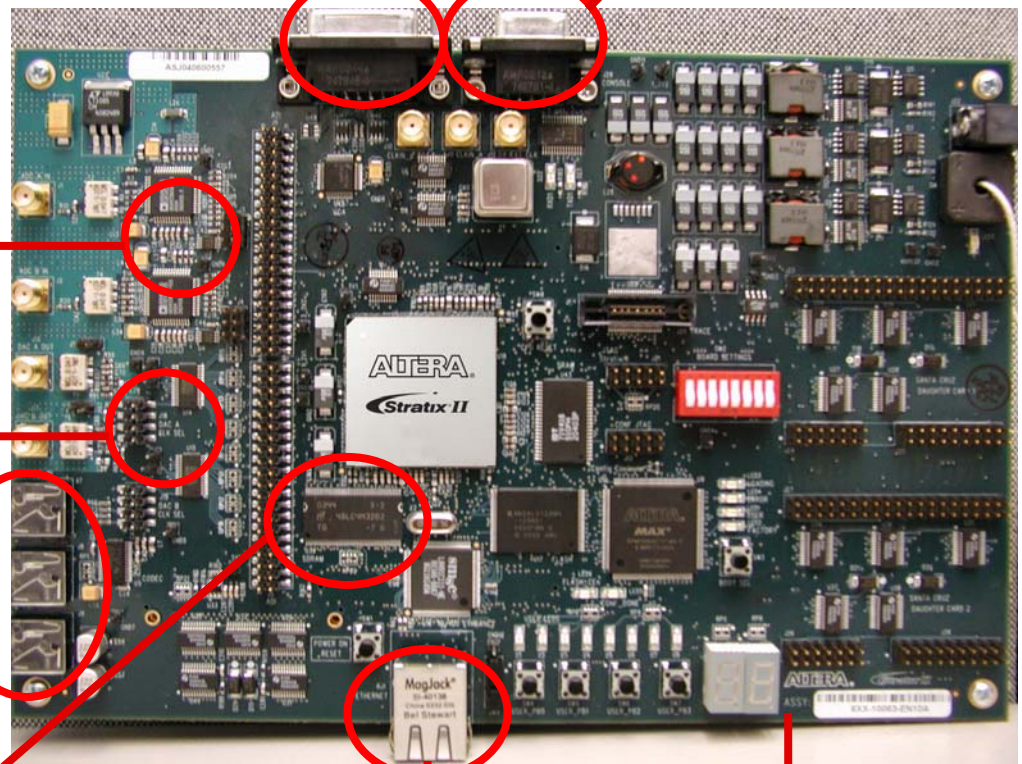
Stratix II DSP Development Board



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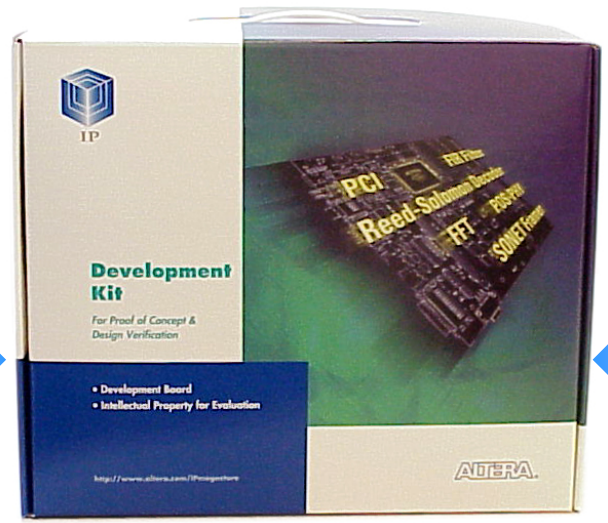
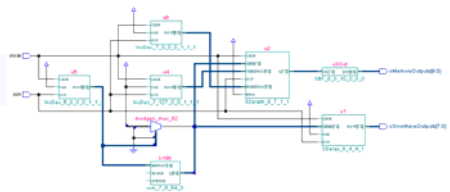
Altera DSP Development Kits

Contains Everything You Need to Develop High-Performance DSP Designs on FPGAs

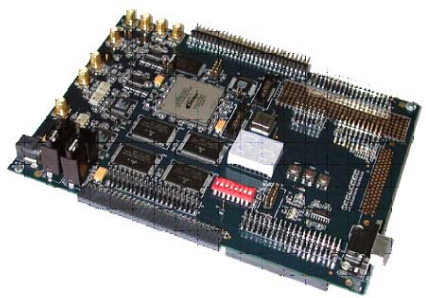
30-Day Evaluation Version



QUARTUS® II



System Reference Designs



OpenCore® plus

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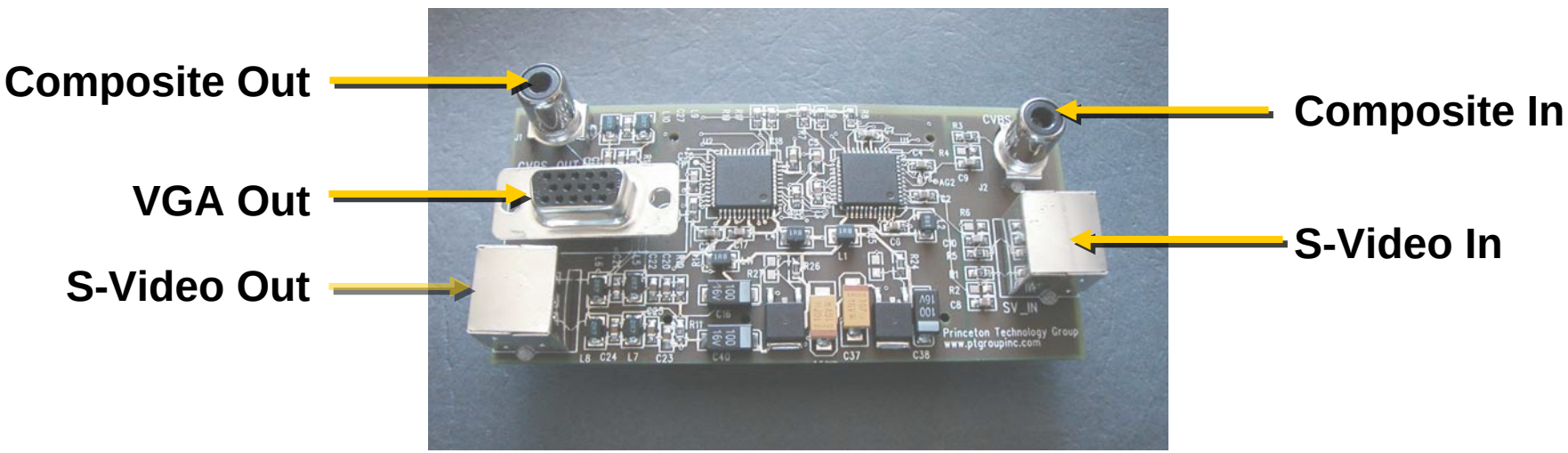
NTSC,PAL & S-Video Daughter Card

- Available from Third Party
- SOPC Builder-Ready

Altera Daughter Card Connector Format



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FPGAs for Control & Dataflow Processing

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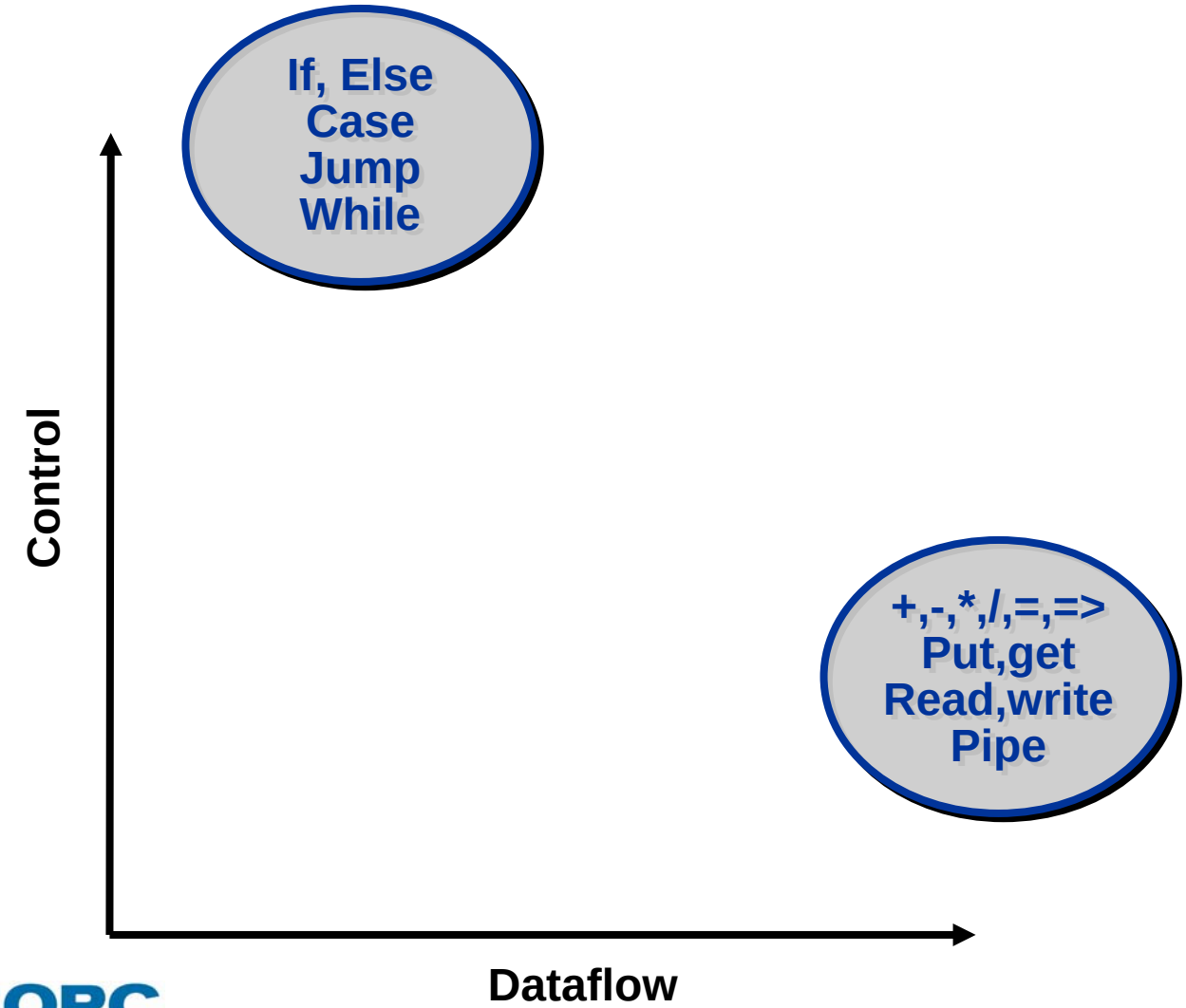
Applications Driving Signal Processing Performance Requirements

- Communications
  - Wireless Communications & High-Speed Data
  - Third-Generation (3G): CDMA2000, WCDMA, HSDPA, 1xEVDO/DV, etc.
  - WiMAX: OFDM
  - RF Linearization: DPD, CFR, DUC, DDC
- Imaging
  - Security, Medical Imaging, Copiers, Studio Editing, Broadcast High-Definition TV
  - H.264, WM9, JPEG2000

Control & Dataflow Processing Mix



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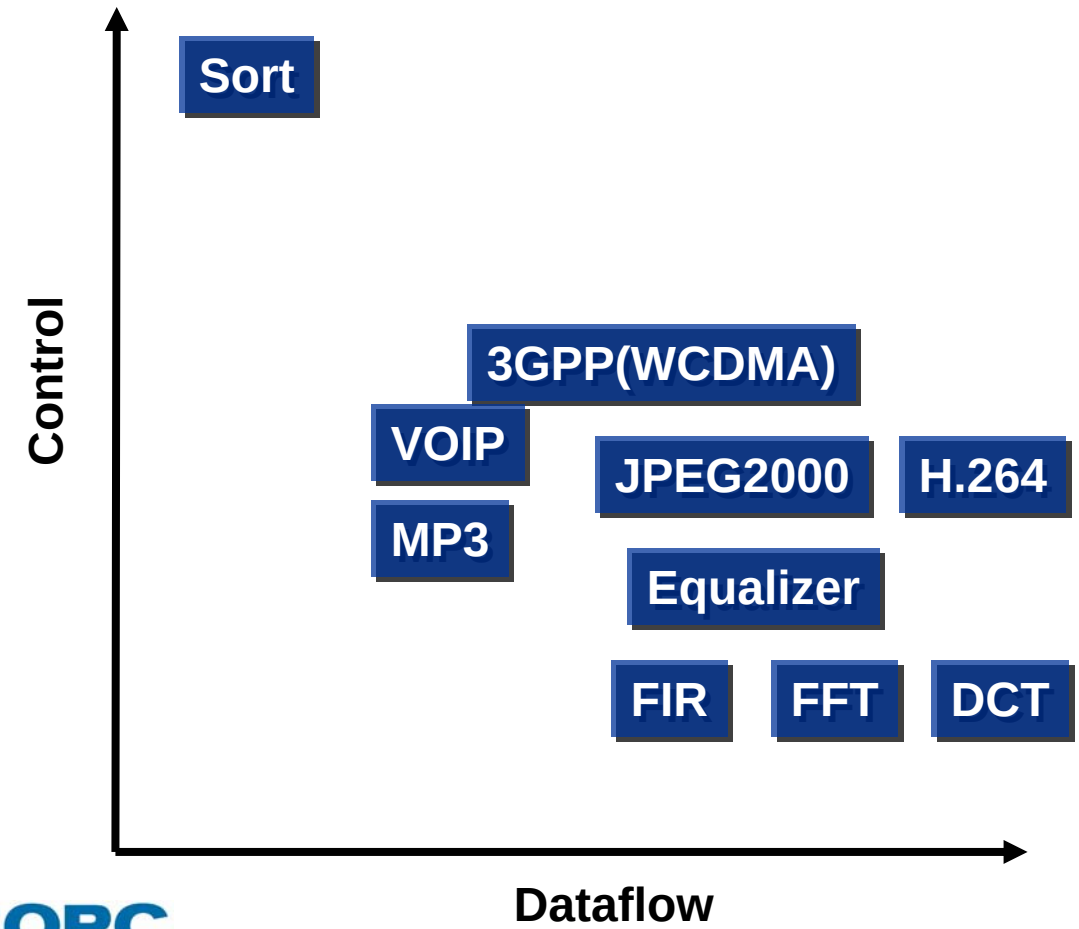
Control vs. Dataflow – Algorithm Mapping



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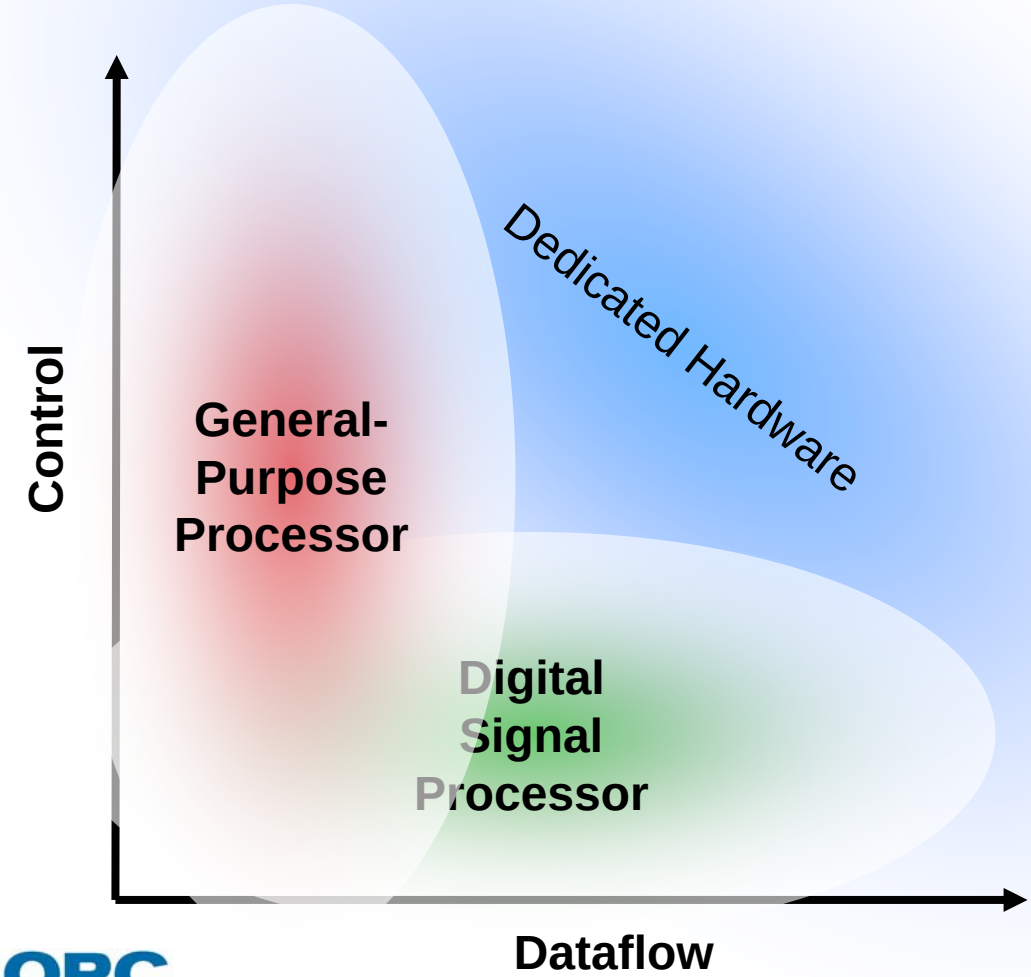
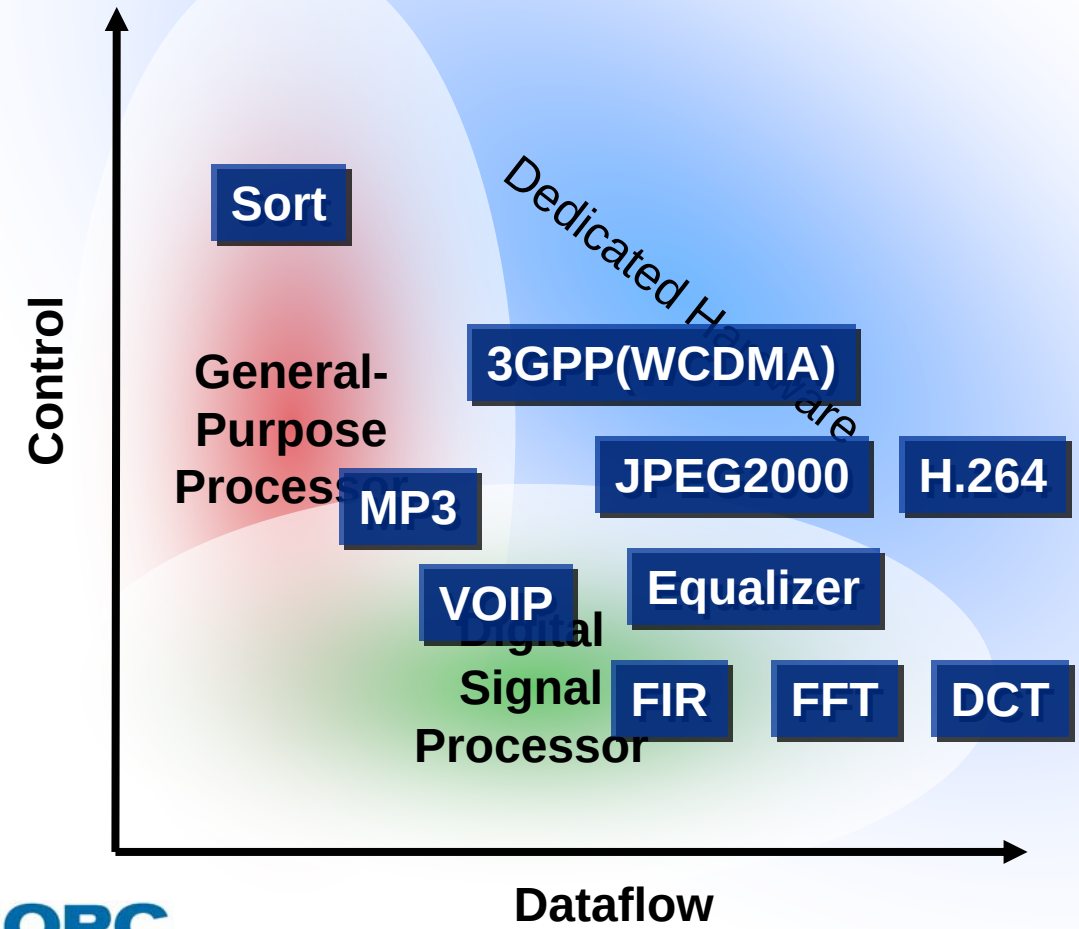
Control vs. Dataflow – GPP vs. DSP



Control vs. Dataflow – Algorithm Mapping



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Hardware vs. Software Comparison
FIR Filter Design

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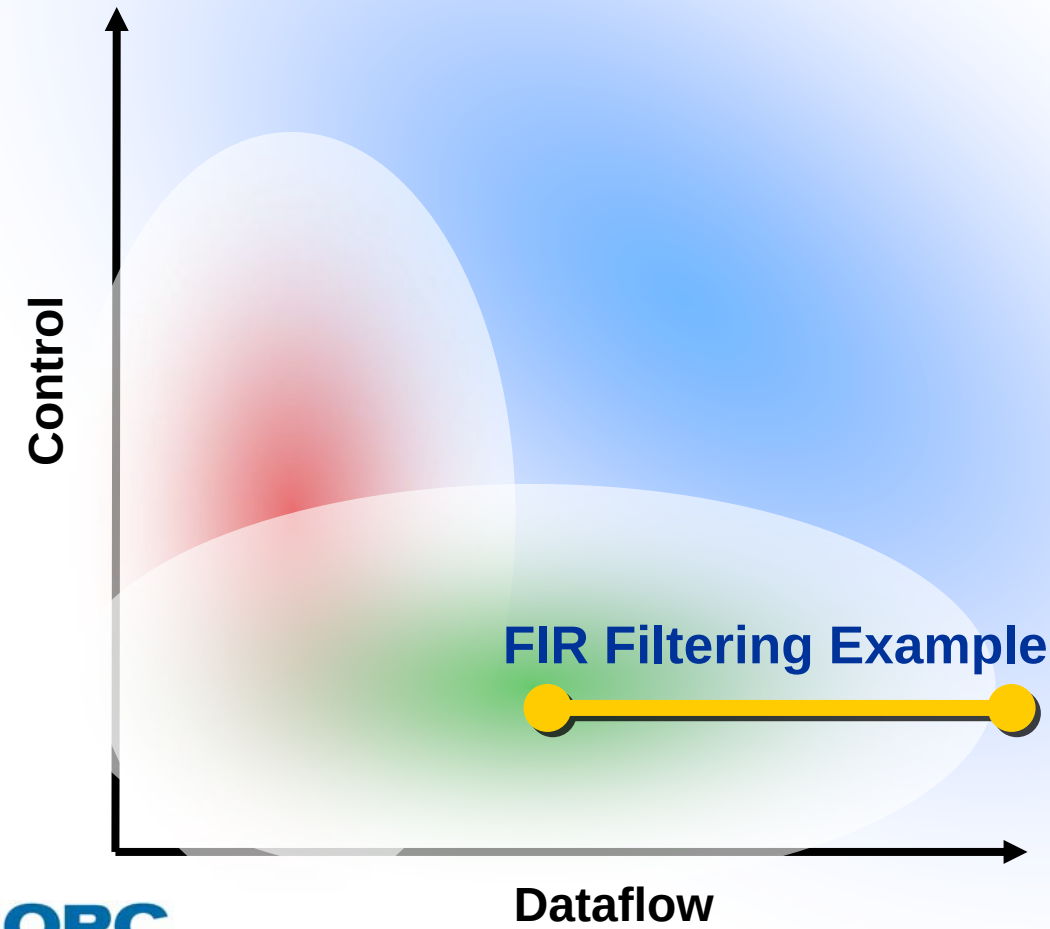
Control vs. Dataflow – Hardware vs. Software



FIR Filter Design Example

- FIR Parameters
  - 128-Tap
  - 16-Bit Data, 14-Bit Coefficients
- DSP Processor vs. FPGA
  - TI C6713 – Optimized TI DSP Library Function
  - Altera 8-Cycle FIR Co-Processor

TI Filtering Library (DSPLib)

- C-Callable Optimized Assembly Routines
- TI C67x DSPLib: FIR Filter (Radix 8)
  - Formula: Nh * Nr /2 + 13
    - Nh = Number of Coefficients
    - Nr = Number of Samples
  - ~1 Sample/ 64 Cycles (128 Tap Filter)

FIR Filter Example* – Higher Performance for Lower Cost

Device	Solution	FIR Performance (MHz)	Device Cost****	Cost per FIR MHz
TI C6713-200	64 Cycles** at 200 MHz	3.125	$33.97	$10.87
Altera 1C3-8	8 Cycles*** at 230 MHz	28.75	$16.40	$0.57

* FIR 128 Tap, 16-Bit Data, 14-Bit Coefficients
** DSPLib Optimized Assembly Libraries from Texas Instruments
*** Optimized MegaCore FIR Compiler from Altera
**** Pricing in Quantity of 100 from Arrow and Avnet 8/25/04

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Cyclic Redundancy Code (CRC) Calculation Example

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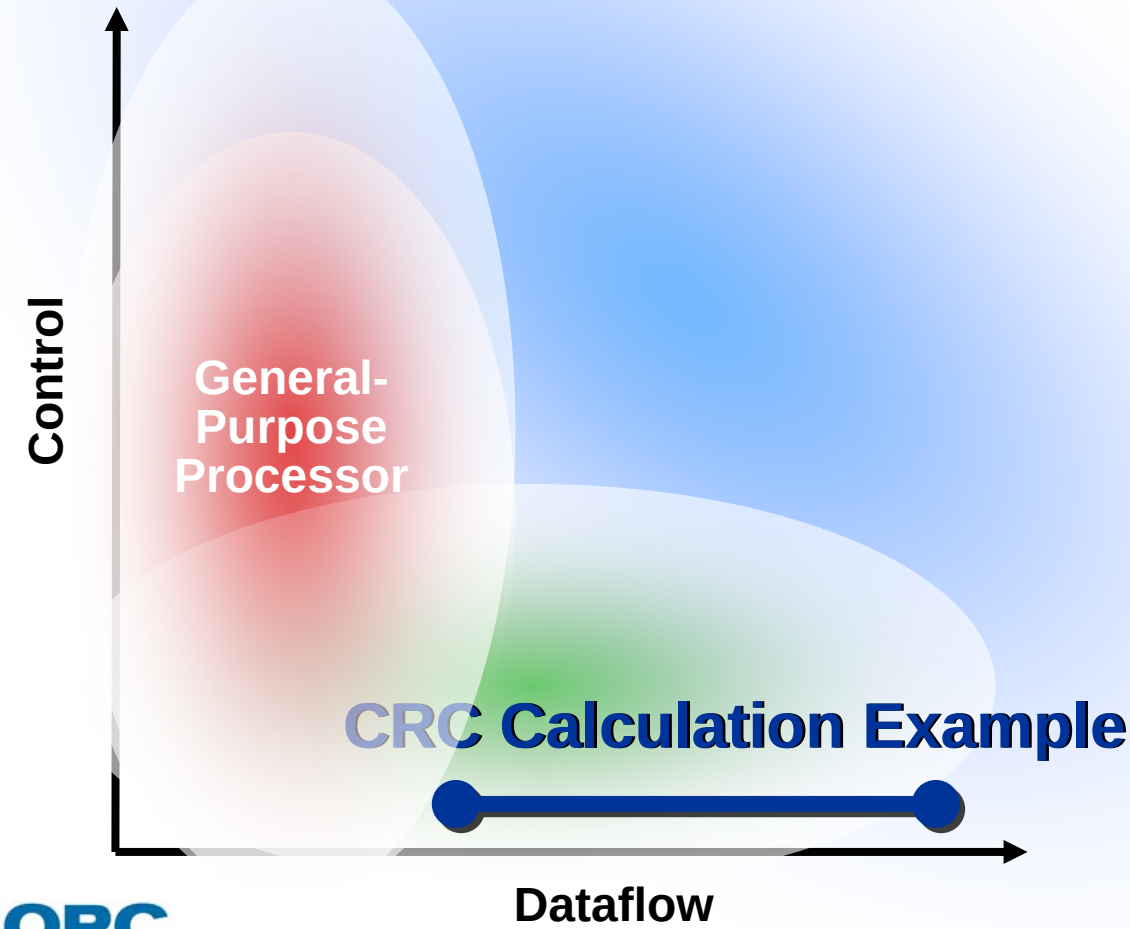
Control vs. Dataflow – Hardware vs. Software



CRC Algorithm – Pseudocode

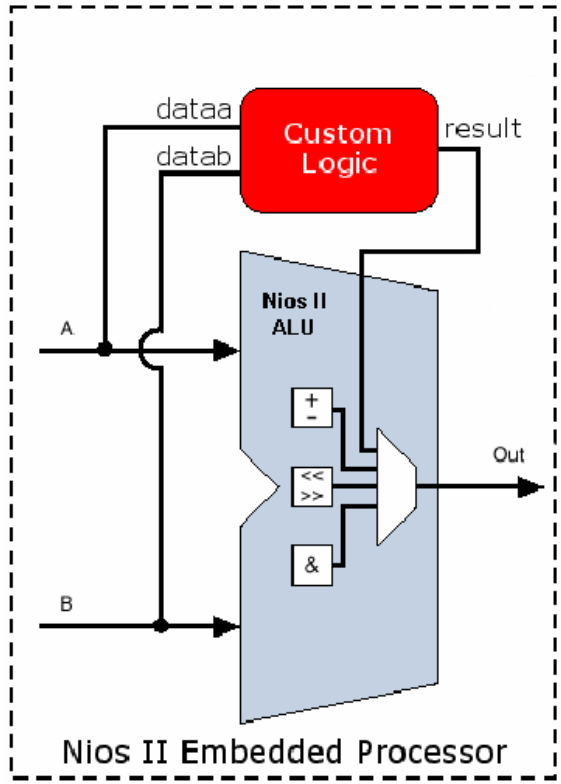
```
shiftregister = initial value (commonly 0x0000... or 0xFFFF...)
while bits remain in string:
    if MSB of shiftregister is set:
        shiftregister = (shiftregister leftshift 1) xor polynomial
        ("leftshift" assumes big-endian architecture) else:
        shiftregister = shiftregister leftshift 1
    xor next bit from the string into LSB of shiftregister
output shiftregister
```

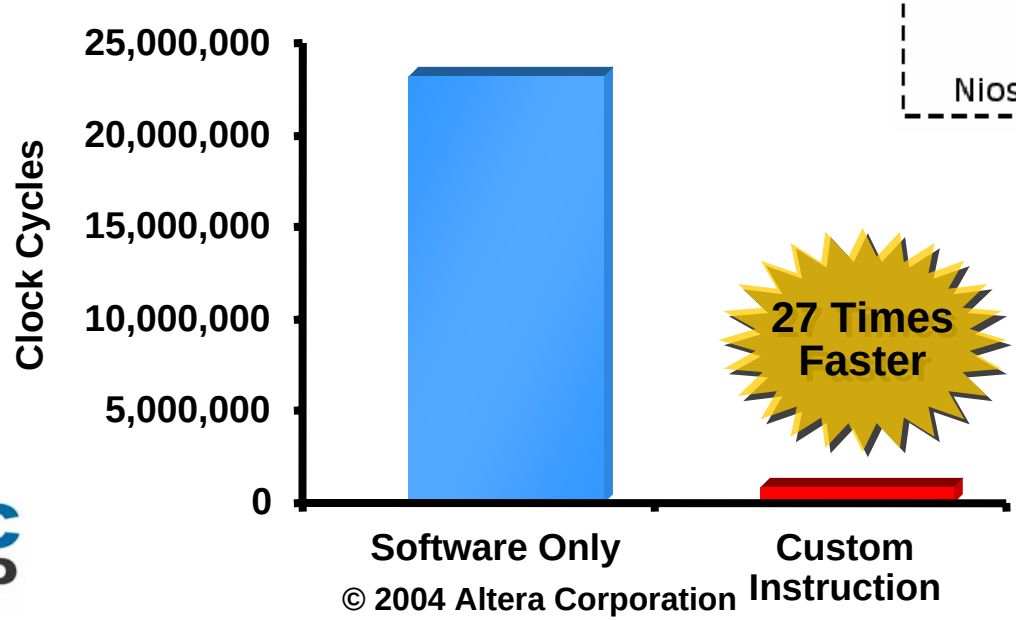
Mixed Control & Dataflow
Bit Level Manipulation of Dataflow

Great for HW Acceleration

Accelerating Software

- Nios II Custom Instructions
  - 256 User-Defined Instructions
  - Fixed & Variable Cycle Operation
  - User Logic Import Wizard
  - Called as C Subroutine
- Example: CRC Algorithm (64 Kbytes)





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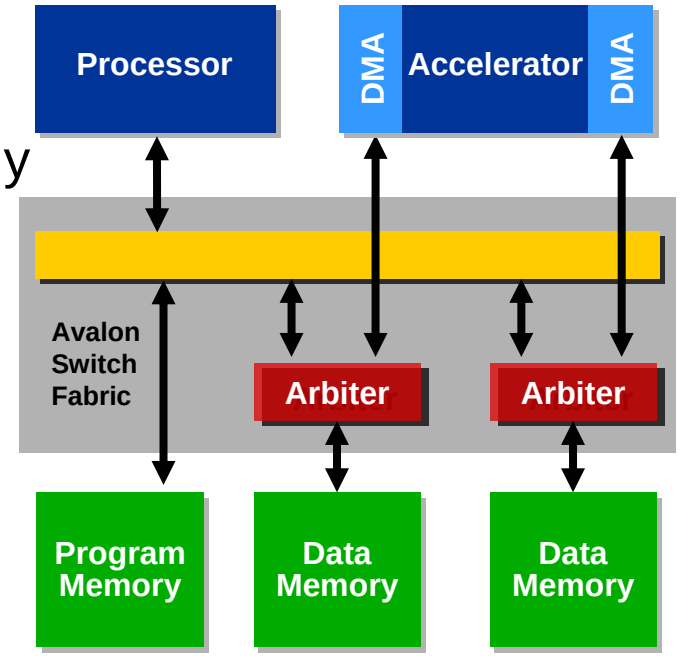
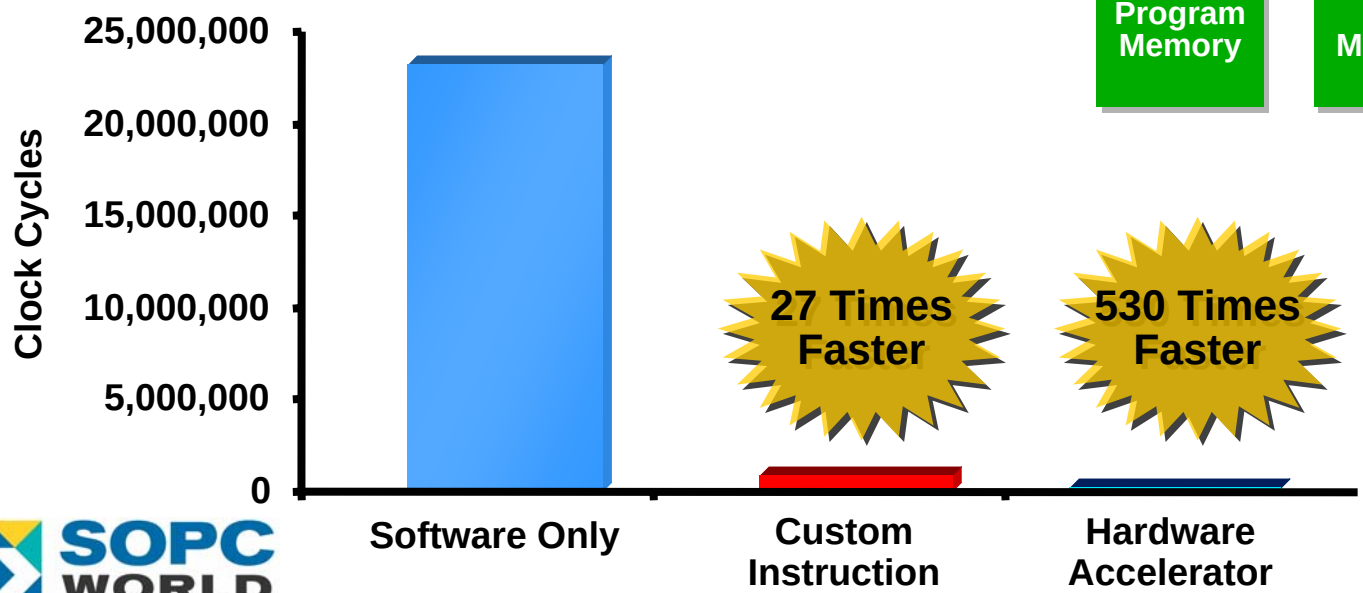
Accelerating Software

- Hardware Acceleration
  - Processor & Accelerator Run Concurrently
  - More Work Per Clock
  - Lower f_{MAX}, Power, Cost
- Example: CRC Algorithm (64 Kbytes)





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Utilizing Nios II for DSP Applications

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Nios II Architecture

- Classic Pipelined RISC Machine
  - 32-Bit Instruction Set Architecture
  - 32-Bit Data Path
  - 32 General-Purpose Registers
  - 3 Instruction Formats
  - Separate Instruction & Data Caches
  - On-Chip Hardware (Multiply, Shift, Rotate)

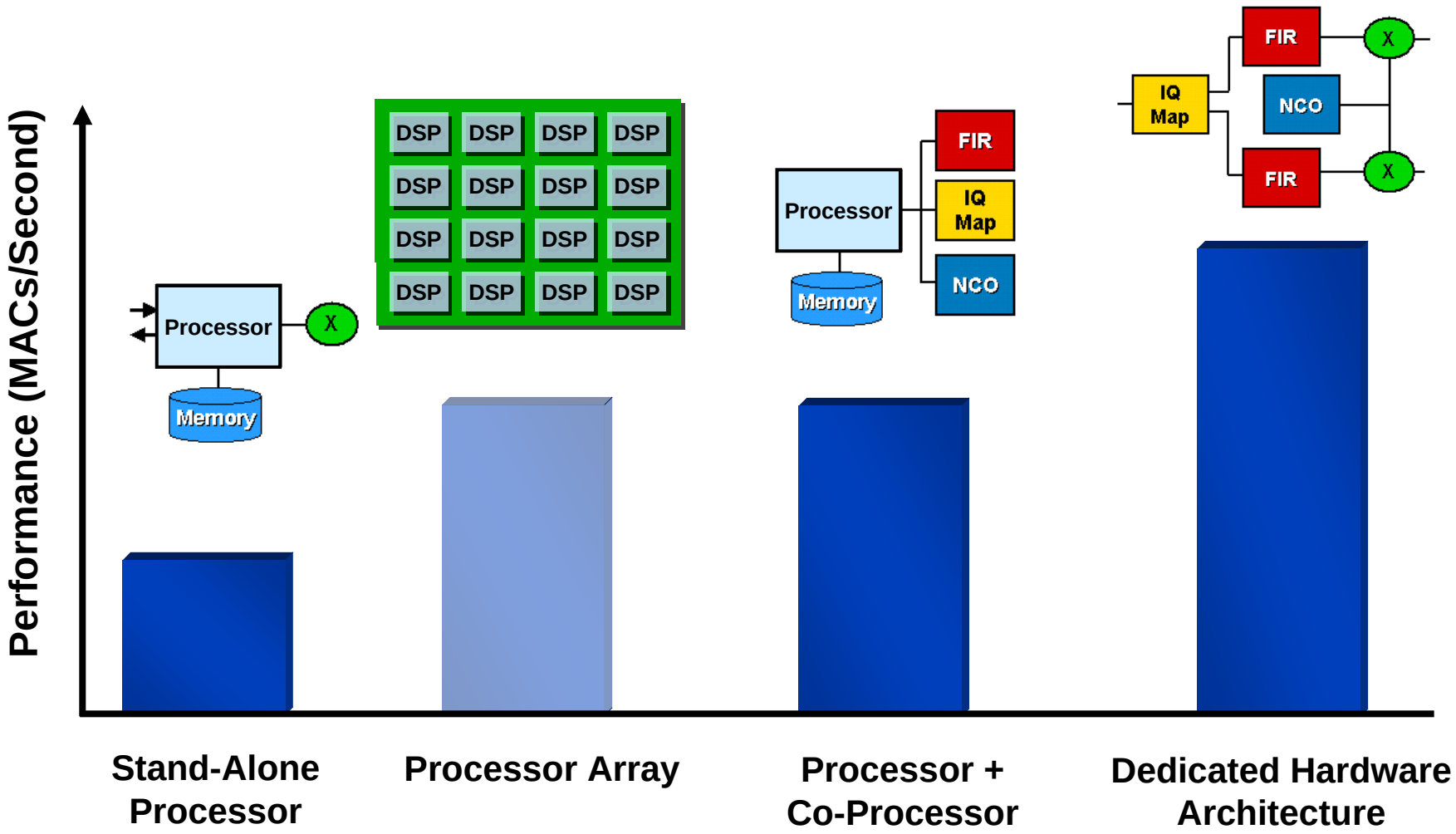
Binary Compatibility/Flexible Performance

	Nios II /f Fast	Nios II /s Standard	Nios II /e Economy
Pipeline	6 Stage	5 Stage	None
Hardware Multiplier & Barrel Shifter	1 Cycle	3 Cycle	Emulated in Software
Branch Prediction	Dynamic	Static	None
Instruction Cache	Configurable	Configurable	None
Data Cache	Configurable	None	None
Custom Instructions	Up to 256		

Nios II Features that Help in DSP

- Single-Cycle HW Multiplier & Shifter
- Custom Instructions
- Hardware Acceleration/Co-Processing
- Separate Instruction & Data Cache with Branch Prediction
- Flexible Direct Memory Access (DMA) Capabilities
- Shared & Switch-Fabric System Bus
- Single or Multi-Processor

DSP Processing Architecture Options



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JPEG2000 Example
Barco Silex

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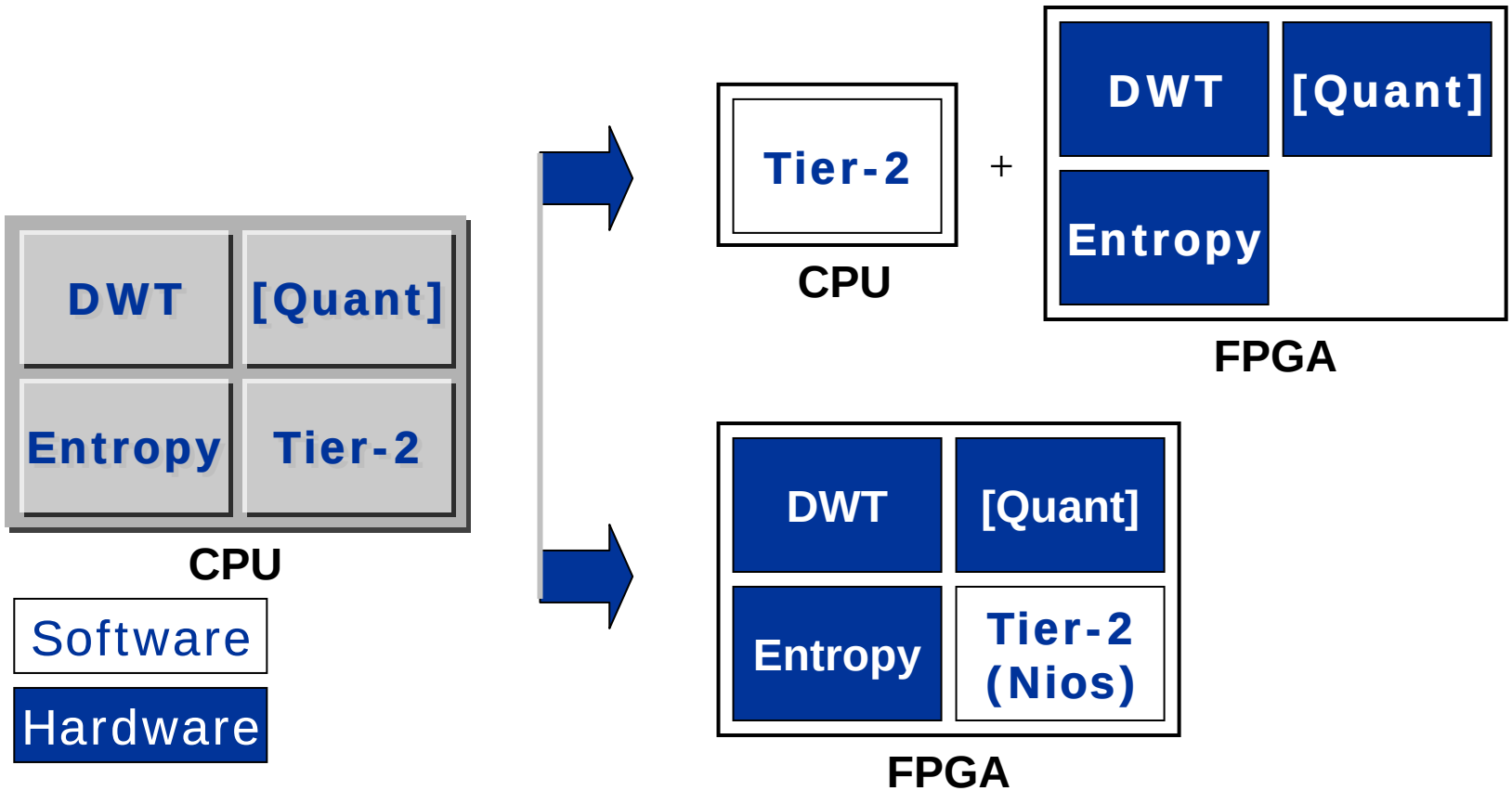
JPEG2000 Challenge

- Rich Feature Set of JPEG2000 Implies Higher Complexity Than JPEG
- Software & DSP Implementations Are Less Efficient
  - Arithmetic Encoding Implies Bit-Level Computations
  - Motorola StarCore SC 140 @ 300 MHz: up to 1 Mcomps/s (1 VGA per s)
  - Philips Trimedia TM1300 @ 180 MHz: up to 5 Mcomps/s (5 VGA per s)
  - Pentium IV 3GHz: Estimated up to 10 Mcomps/s (10 VGA per s)
- Hardware Acceleration Provides a Solution for Real-Time Applications
  - FPGAs & Structured ASICs Architectures Can Leverage JPEG2000 Acceleration

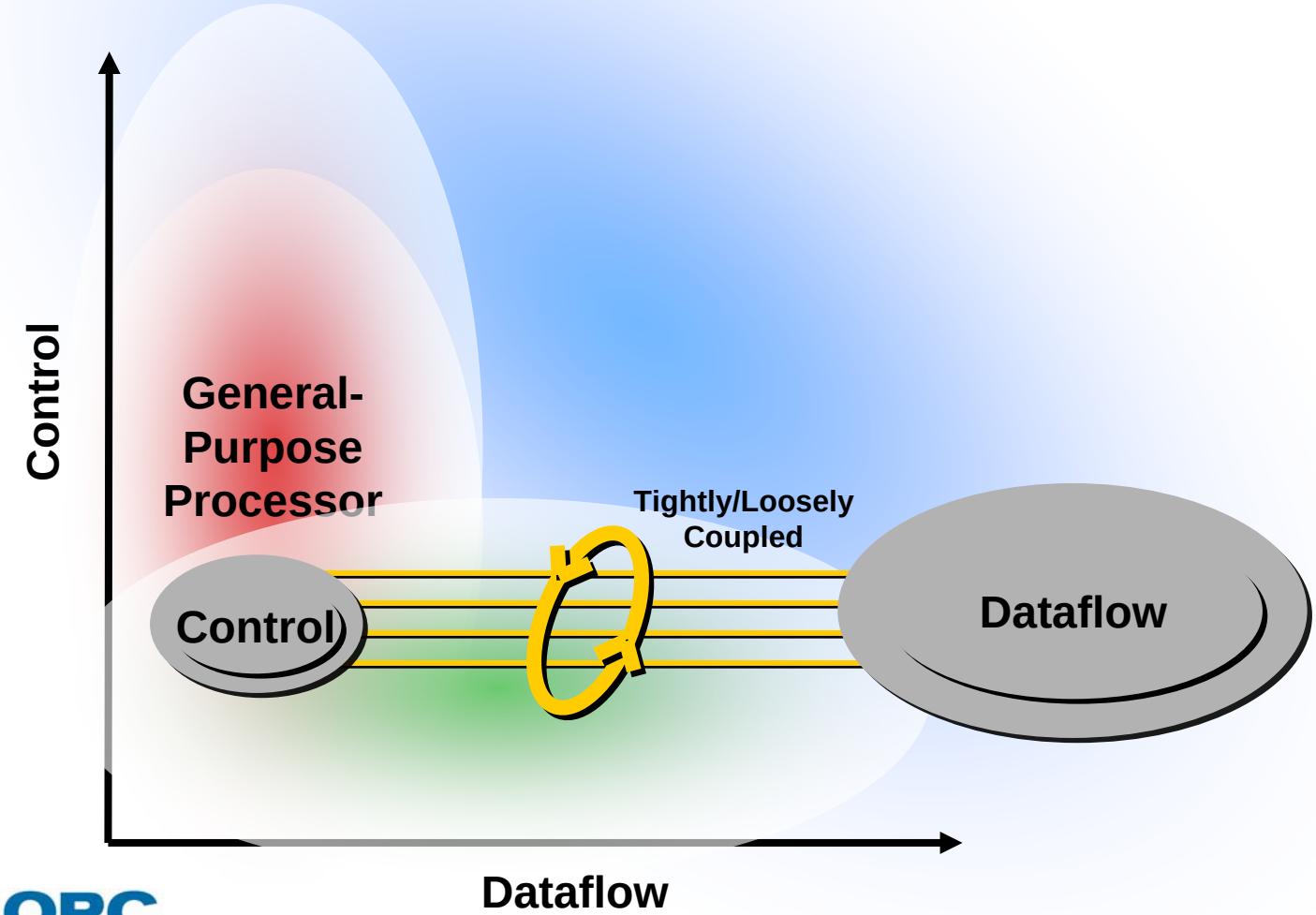
VGA = 640 x 480 RGB

JPEG2000 Accelerated by FPGAs

- Co-Processing: Unload CPU for Critical JPEG2000 Processing

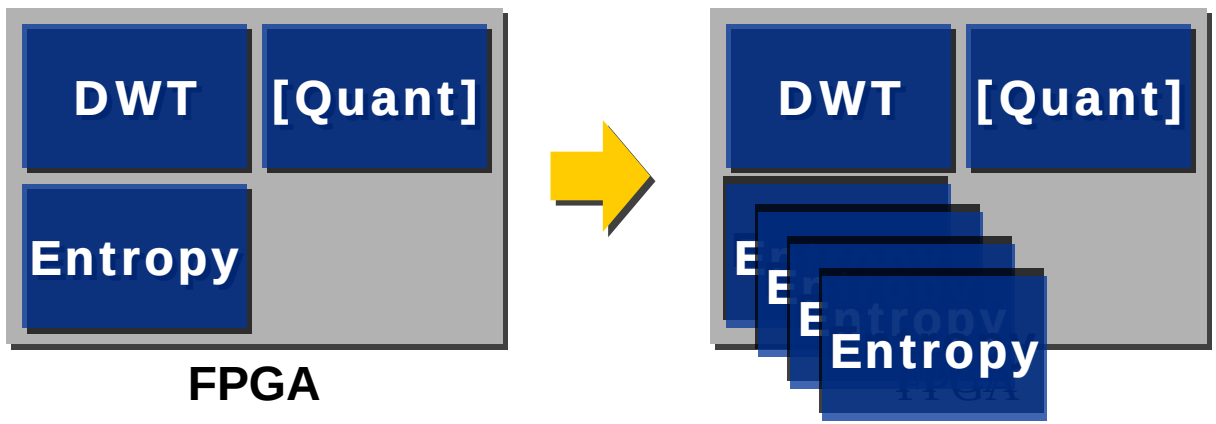


Control vs. Dataflow



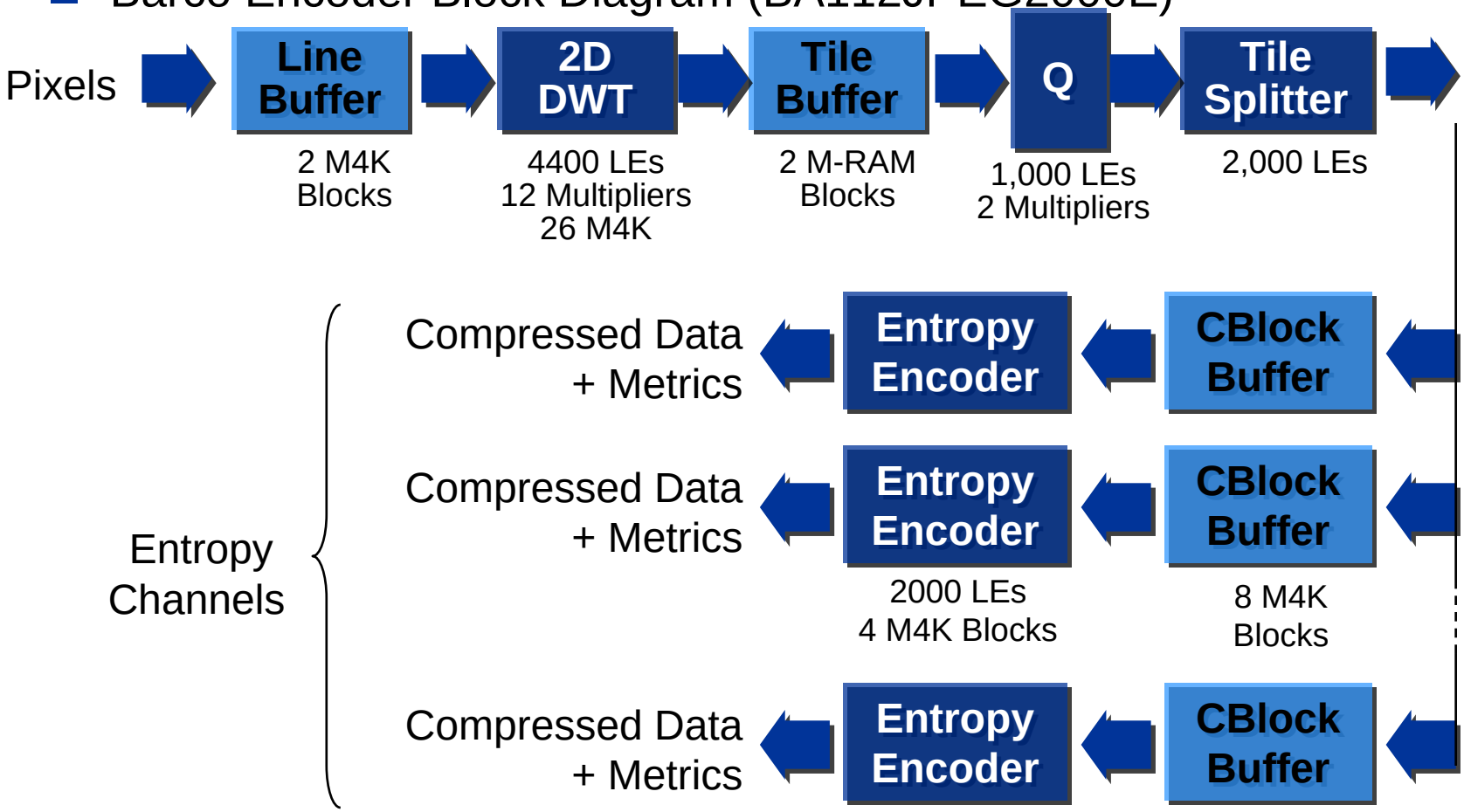
JPEG2000 Accelerated by FPGAs

- Paralleling: Boost Slowest Processing
  - Arithmetic Encoding (Bit-Level Algorithm)
  - Parallelism Configured at Synthesis Stage
    - Adapt the Number of Parallel Entropy Encoders to the Application Needs



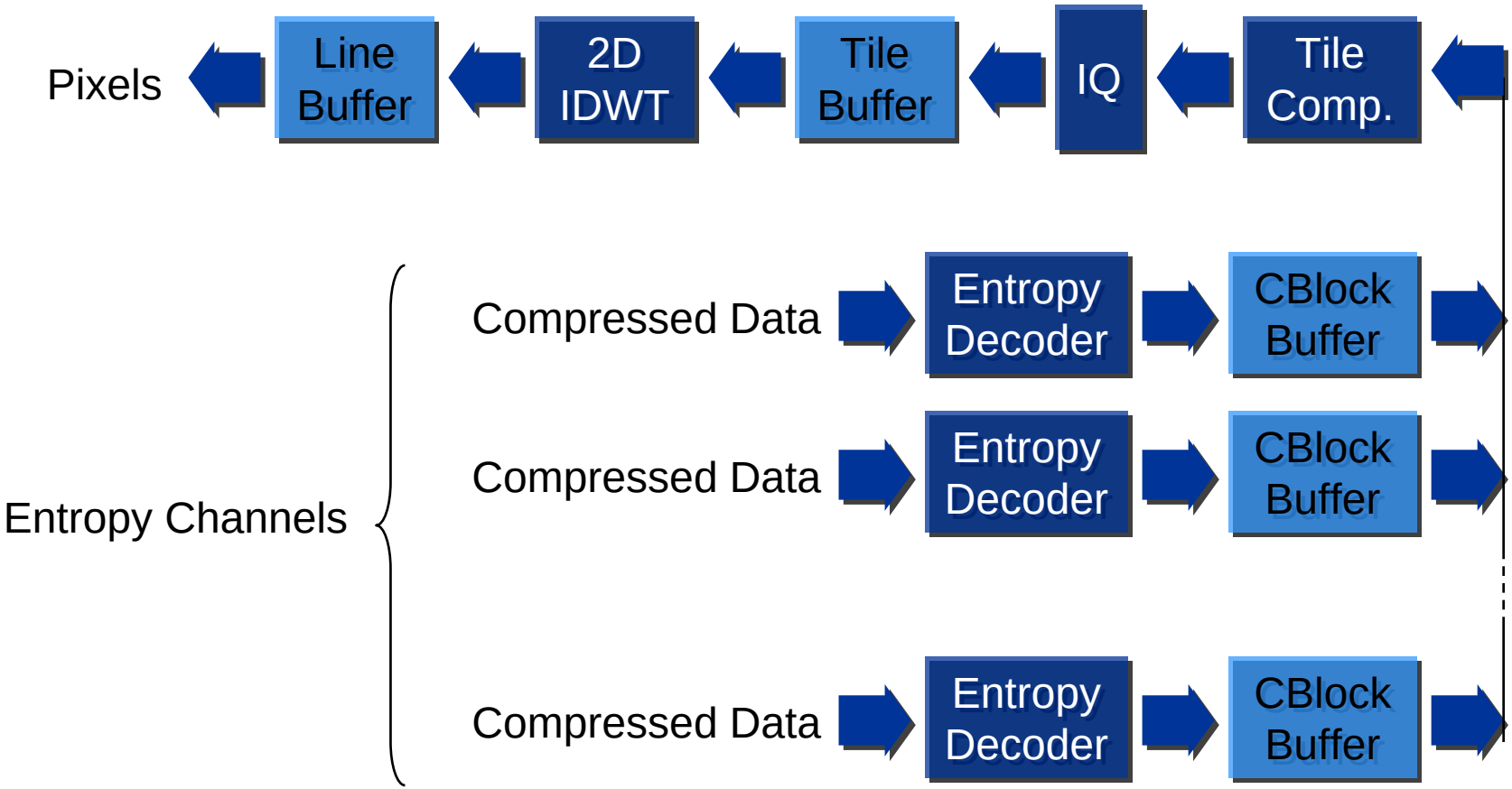
Barco JPEG2000 IP on FPGA

- Barco Encoder Block Diagram (BA112JPEG2000E)



Barco JPEG2000 IP

- Barco Decoder Block Diagram (BA111JPEG2000D)



Altera Performance Data

Encoder Configuration	Speed (comp/s)	Area (#LEs)	Memory (#M4K Blocks)
Encoder with 1 Channel	10M (> *CIF 30 Hz*)	9,400	40 (+2 M-RAM Tile Buffer)
Decoder with 1 Channel	8M (> *CIF 30 Hz*)	8,400	44 (+2 M-RAM Tile Buffer)
Encoder with 8 Channels	72M (>> *SVGA 30Hz*)	23,400	124 (+2 M-RAM Tile Buffer)
Decoder with 8 Channels	57M (>> *SVGA 30Hz*)	25,000	156 (+2 M-RAM Tile Buffer)

Altera Stratix EP1S-C5, Results Given for Typical Lossy Compression

Altera Performance: Stratix FPGAs

Stratix Device	Area (*#LEs, % Usage*)	# Entropy Channels	Sample Rate†/‡	VGA* (Hz)	PACS 3M** (ms)
EP1S20C5	10,500 (58%)	2	14M/10M	15/10	225/315
EP1S25C5	20,500 (79%)	6	39M/29M	42/31	81/109
EP1S40C5	25,000 (61%)	8	50M/37M	54/40	63/85
EP1S60C5	50,000 (87%)	8	100M/74M	108/80	32/43

* *Decoding Capability Based on VGA 640x480 RGB 4:4:4*

** *Decoding Capability Based on Monochrome 3-Mpixel (PACS) 2048x1536*

† *Typical Lossy*

‡ *Typical Lossless*

Pentium IV	1M - 10M	1 - 10
Trimedia	0.5M - 5M	0.5 - 5
StarCore	0.3M - 1M	0.3 - 1

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Altera Performance: Stratix II FPGAs

Stratix II Part	Area (*#LEs, % Usage*)	# Entropy Channels	Sample Rate†/‡	VGA* (Hz)	PACS 3M** (ms)
EP2S15C5	10,500 (67%)	2	14M/10M	15/10	225/315
EP2S30C5	25,000 (74%)	8	50M/37M	54/40	63/85
EP2S60C5	50,000 (83%)	8	100M/74M	108/80	32/43

* *Decoding Capability Based on VGA 640x480 RGB 4:4:4*

** *Decoding Capability Based on monochrome 3-Mpixel (PACS) 2048x1536*

† *Typical Lossy*

‡ *Typical Lossless*

Pentium IV	1M - 10M	1 - 10
Trimedia	0.5M - 5M	0.5 - 5
StarCore	0.3M - 1M	0.3 - 1

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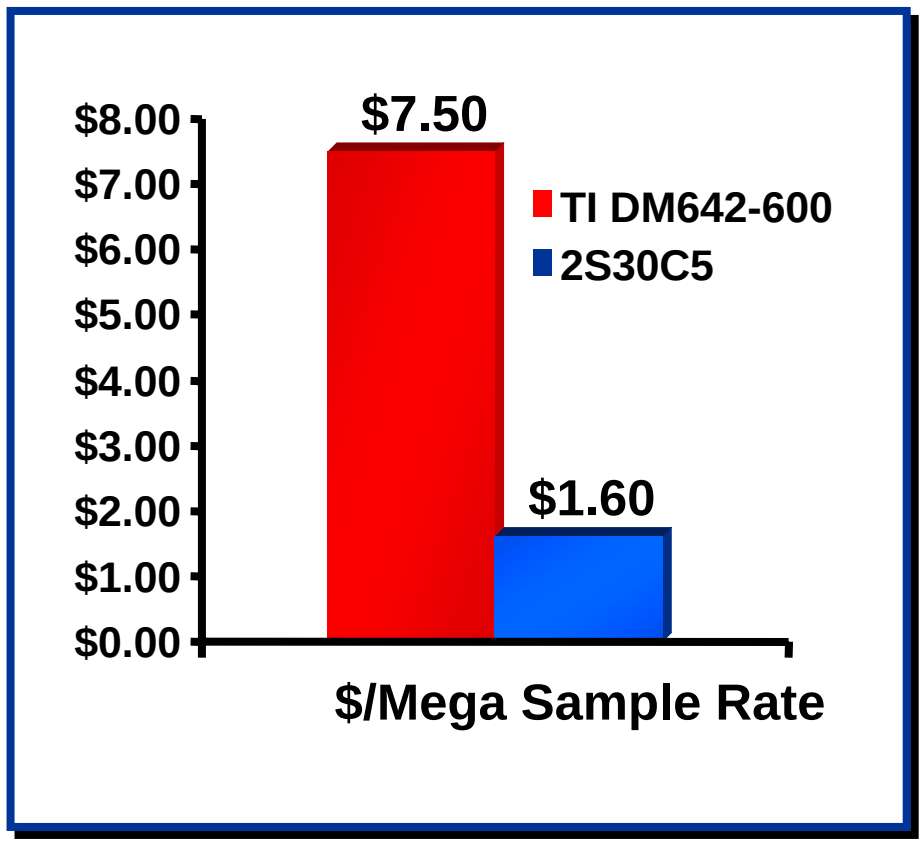
Price/Performance Comparison

- Based on 8 Channels in a EP2S30 Device (Typical Rate of 50 Msamples/s)
- Based on 10k-Unit Pricing: TI TMS320DM642 ($45), EP2S30C5 ($80)
- Typical Decoding Rate on DM642 Estimated to Be 6 Msamples/s
- Advantage in Price/Performance
  - FPGA: 4.5x
  - HardCopy® Series: 9x



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Digital Pre-Distortion Example

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Example: Digital Pre-Distortion

- Third-Generation (3G) Wireless Communication
  - Linear Operation for Power Amplifier
- RLS Algorithm Detail
  - Solve for Complex Array b_N Where:
    - $z`_N$ is a Single-Dimensional Complex Array
    - R_{NN} is a Two-Dimensional Complex Array

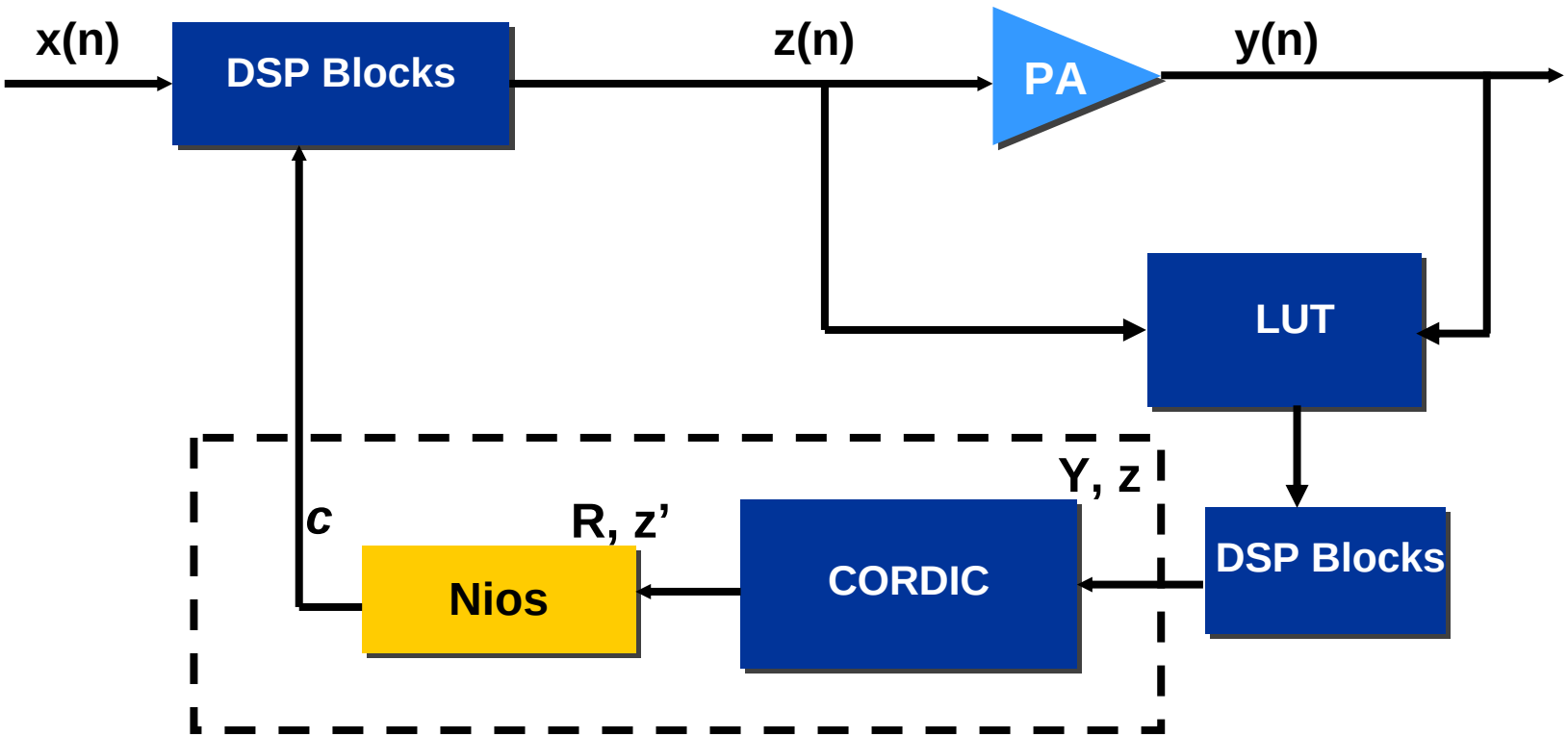
$$b_N = \frac{z'_N}{R_{NN}}$$

$$b_i = \frac{1}{R_{ii}}\left(z'_i - \sum_{j=i+1}^{N} R_{ij} b_j \right)$$

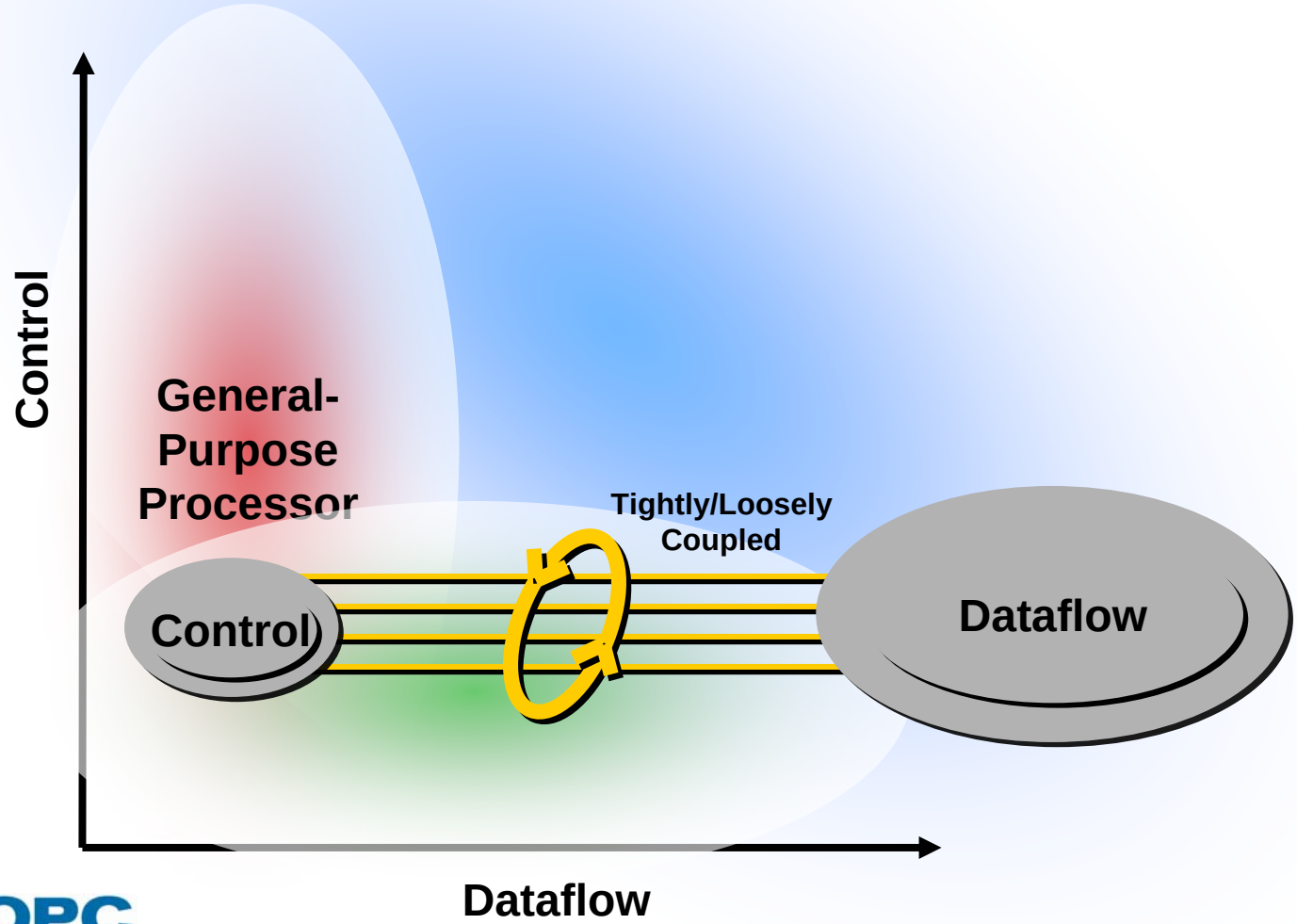
$$for\ i = N-1,\ldots,1$$

Resource Mapping for QRD-RLS

- CORDIC for QR Decomposition
- Nios Processor for Back Substitution



Control vs. Dataflow – QRD-RLS



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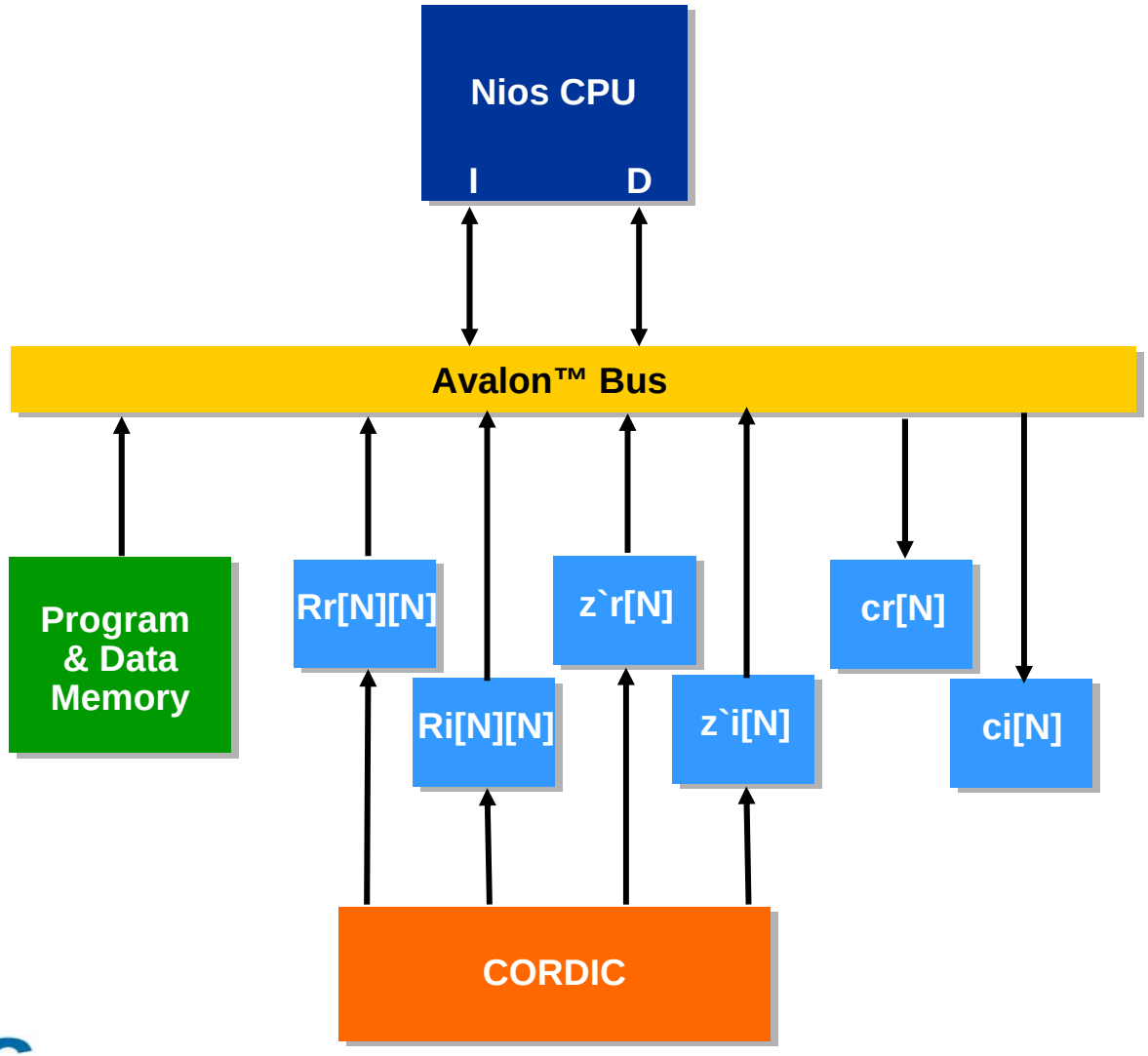
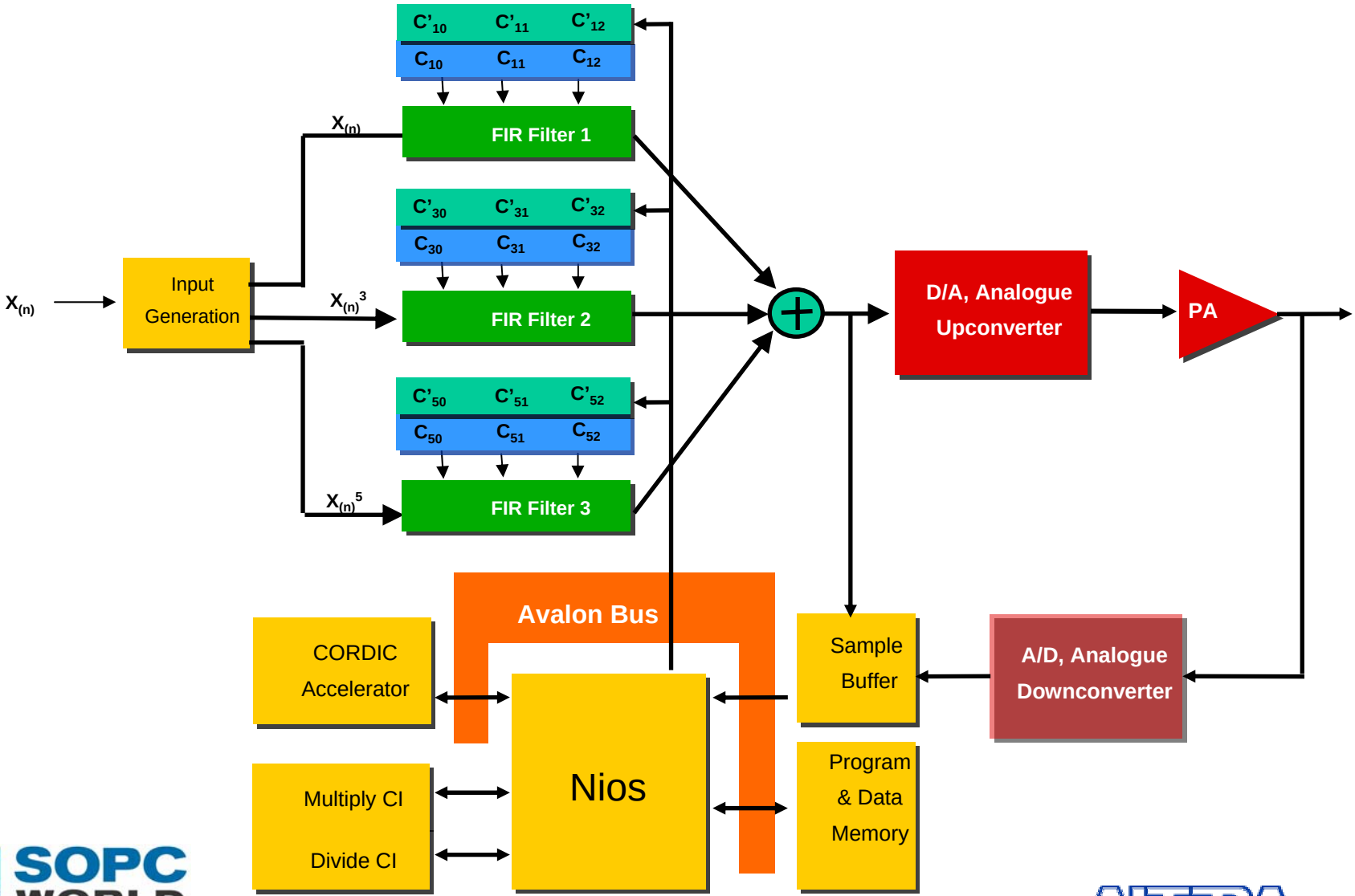
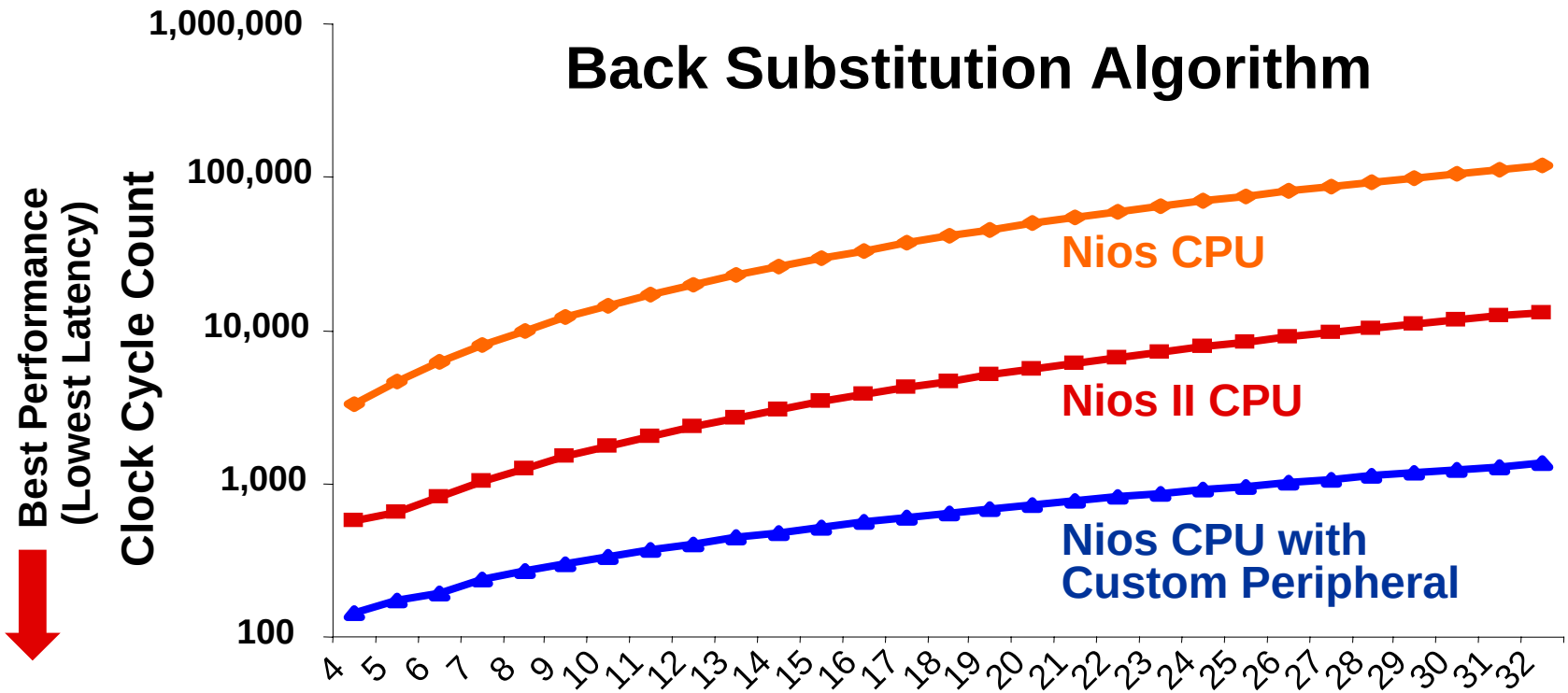
Back Substitution Using Nios



Block Diagram



Back Substitution Results – Latency Comparison



Software Flexibility + Hardware Acceleration with Custom Instructions & Custom Peripherals

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Resource Estimate

- Pre-Distorter Described by Memory Polynomial Model
- Coefficients Determined in Feedback Path Using:
  - QRD-RLS Algorithm
  - CORDIC Used in Discrete Mapping Scheme to Implement Systolic Array
  - Nios Processor Used for Back Substitution
- Estimates Do NOT Include:
  - Memory Requirements (Abundant Supply in All Stratix II Devices)
  - Control Logic

Polynomial type	CORDIC blocks	LEs for CORDIC + Nios	Number of Multipliers		Update Delay	Suitable Stratix Device
			18x18 Multiplier	DSP Blocks		
K=2 (5th Order), Q=2 (2 Previous Terms)	2	4,100	23	6	320 us	EP2S15
K=2 (5th Order), Q=5 (5 Previous Terms)	2	4,100	42	11	900 us	EP2S15
7th Order (Both Even & Odd Terms), Q=2 (2 Previous Terms)	2	4,100	50	13	Less Than 1.05 ms	EP2S30

Maintaining Accuracy

- Fixed Point Solution
  - Larger Bit Widths for CORDIC & in Forward Path Intermediate Products
- Floating Point Solutions
  - Forward Path: Floating Point Operations (multiply, add)
  - Feedback Path
    - Implement Systolic Array with Floating Point Operations—No CORDIC
    - Implement Systolic Array with Floating Point CORDIC
- Hybrid Solution
  - Floating Point Operations
    - Forward Path
    - Calculation of High Order Terms to Be Fed into Systolic Array in Feedback Path
  - Fixed Point Operations
    - CORDIC Blocks (with Floating Point Extension) in Feedback Path
- Right Solution
  - Depends on Performance—Cost Requirements for Individual Customers

Resource Comparison of Options

- Fixed Point Solution (e.g., Extending Bit Widths from 16 to 32)
  - CORDIC Resources Increase by ~250%
  - Multipliers Required Increase by up to 300%
- Floating Point Operators (multiply, divide, add)
  - Require ~20-30% More Resources than Equivalent Fixed Point Operators
  - Employ the Use of Barrel Shifters
- Floating Point CORDIC vs. Fixed Point CORDIC
  - ~20-30% Larger
  - Requires Barrel Shifters
  - Slower Throughput as Non-Pipelined (Serial Architecture)

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FPGA Co-Processor Reference Design

Turbo Encoder for HSDPA

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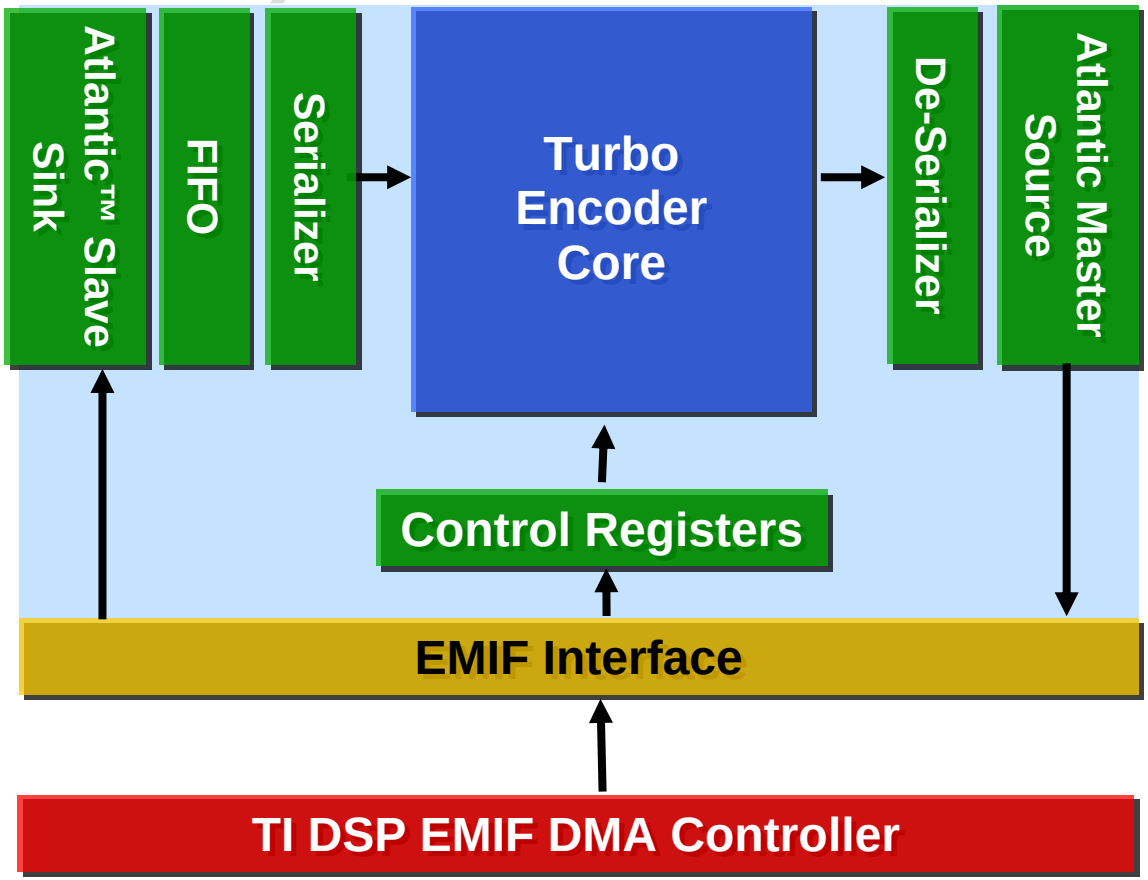
Turbo Encoder Co-Processor Reference Design (TI Solution)

- Interface to TI DSP EMIF (External Memory Interface)
  - Other Processor Interfaces in Development
- Uses DSP Processor's On-Chip DMA
- Wrapper for Turbo Encoder MegaCore Function
  - Can Select a Different Configuration (e.g., Block Size) for Each Data Packet/Block
- Software Libraries

Turbo Co-Processor Block Diagram (TI Solution)



Turbo Core Wrapper

Data Buffering

- FIFOs in Atlantic Slave Sink Store EMIF 64-Byte Bursts While Being Serialised into Core
- Slave Sink in Receive Converter Has Similar FIFO
- FIFOs Introduce Latency But:
  - Throughput Is Maintained
  - System Bus Not Tied Up During Serialization/Deserialization

Example Software Environment

- Running on TI DSP
- Uses EDMA Controller to Transfer Data
  - To & From Accelerator
- Asynchronous, Streaming, Interface
  - Callback when Packet is Complete
  - Can Submit 2nd Packet Before 1st Is Done
    - Callbacks Occur in Order

Cost Analysis Example (1)

14.4 Mbps Turbo Encoder

Cyclone FPGA:
$7.00

- 2,544 LE-Equivalent Cost Based on EP1C3T100C8 10k Units (July 2003)

TI C64 DSP:
$29.50

- 136/600 MHz Based on 9.7 cycles/bit (Source: TI)
- C6416/600MHz @ $130 10k-Units Pricing (Source: TI)

Cost Analysis Example (2)

58Mbits/s Turbo Encoder

Cyclone FPGA:
$10.50

- 2,544 LE-Equivalent Cost Based on EP1C3T100C6 10k Units (July 2003)

TI C64 DSP:
$122.00

- 563/600 MHz Based on 9.7 cycles/bit (Source: TI)
- C6416/600MHz @ $130 10k-Units Pricing (Source: TI)

Advantages of Altera Solution

- Bit Streams Make it Difficult to Exploit Digital Signal Processors' Fixed Data Width
  - Most Operations Are on Bit Level (CRC, Turbo Coding, Interleaving, Scrambling, etc.)
- Multiple Channels Easy to Implement
  - Highly Parallel Implementation Possible
    - Minimizes Latency (HSDPA)
    - Minimizes Need for Temporary Storage
  - Efficient Timesharing Architectures for Main Elements on PLDs
- PLDs Allow Full Control for Size/Speed Trade-Off for Each Component
- Low-Cost Cyclone Family Provides Cost Advantage

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Thank You !

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