

Mentor Graphics Solutions Enable Fast, Efficient Designs for Altera's FPGAs

Fall 2004

**Mentor
Graphics®**

Agenda

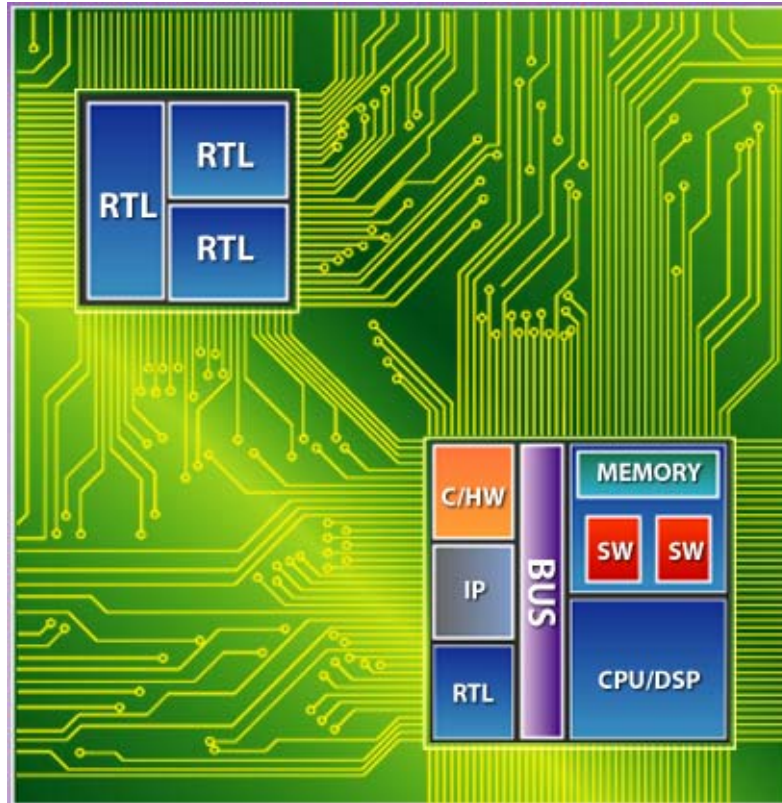
- FPGA design challenges
- Mentor Graphics comprehensive FPGA design solutions
- Unique tools address the full range of complex device- and system-level challenges
 - HDL Designer Series
 - ModelSim
 - Precision Synthesis
 - I/O Designer

Complex FPGA Systems Demand New Design Approaches

Mainstream / Ready-to-use FPGA/PLDs

- Synthesize
- Place & Route
- Simulate/Debug

Low-cost tools
Push-button flow



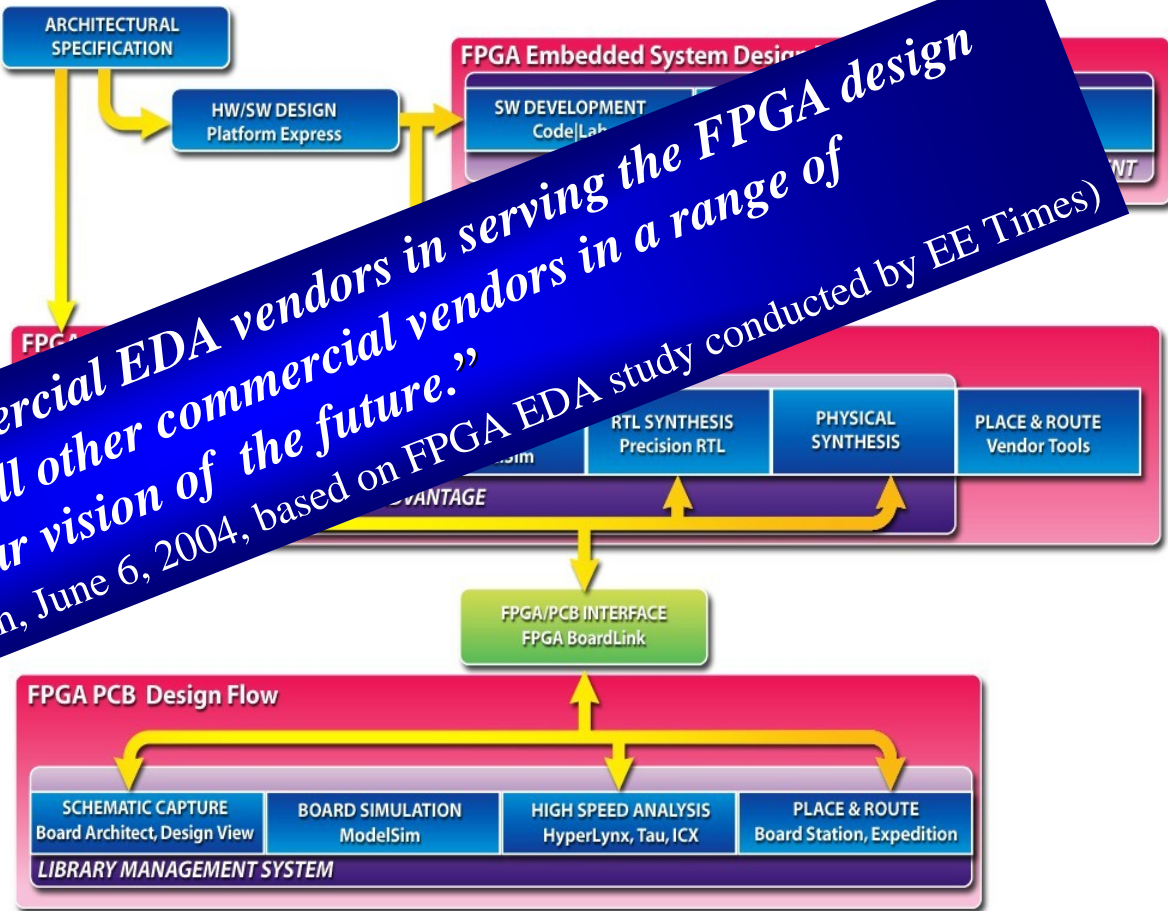
High-end FPGA/FPSoC

- Complex timing
- Physical timing problems
- IP integration
- HW/SW design
- Complex debug
- Prototyping
- SDC constraints
- C-based design
- PCB integration issues
- Team design

Sophisticated tools
ASIC-like flow

Mentor Graphics FPGA Design Flow

- Most comprehensive in the industry
- Incorporates complex FPGA design aspects
 - Embedded systems
 - RTL simulation and synthesis including incremental design



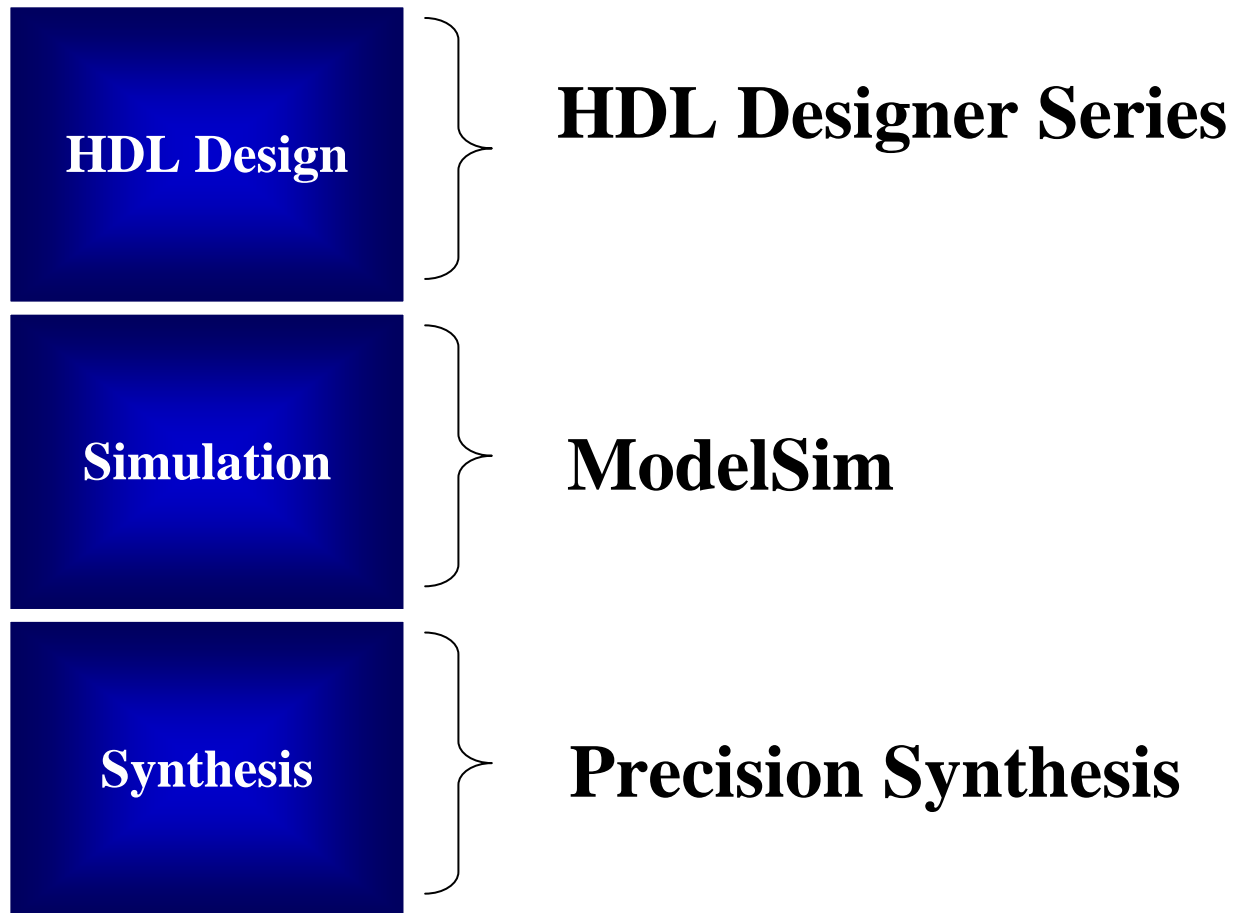
Mentor HDL Flow.psd Rev09.03

Some Mentor Graphics FPGA Design Product Names

- **FPGA Advantage®**
 - Complete FPGA design environment
- **HDL Designer Series™**
 - Design creation, reuse, management, documentation, and design flow control environment
- **ModelSim®**
 - HDL simulation
- **Precision® Synthesis**
 - RTL synthesis
 - Physical synthesis
- **Catapult™ C Synthesis**
 - Algorithmic, untimed C/C++ synthesis for FPGA/ASIC
- **LeonardoSpectrum™**
 - FPGA and ASIC synthesis
- **Seamless™**
 - Hardware/Software co-verification environment
- **XRAY® Debugger**
 - Software debug for embedded processors
- **Inventra™ IP**
 - IP cores for faster, reliable time to market
- **Nucleus™**
 - RTOS family of embedded software
- **HyperLynx®**
 - SI and EMC analysis suite
- **I/O Designer™**
 - Integrated systems design, enabling concurrent FPGA-on-board design

FPGA Advantage

The FPGA Design Flow



HDL Designer Series: Design Creation

- Interface-based design (IBD)
 - Structural design definition
 - Synthesis properties specified for flow
 - Aids documentation
- Block diagram
- Text entry
- State machine
- Flow chart
- Truth table
- ModuleWare

The image displays three overlapping windows from the HDL Designer Series software. The top window is a truth table editor for a module named 'preview'. The table has columns for inputs (A-L) and outputs (F-L). The bottom-left window is a block diagram showing a 'TRAINING' block connected to a 'pp_and' block. The bottom-right window is a code editor showing Verilog code for the 'preview_struct' module.

	A	B	C	D	E	F	G	H	I	J	K	L
1						+						
2		Order	Name	Bounds	Type	preview	gb1	inter	pp_and	max_load		Comments
3			Instance Ref:			1	1	11	10			
4			Frame Label:									
5			Port Map:									
6	+		Port Map Exp:									
7	1	2	PC		pp_array							
8	2		PS		pp_array							
9	+	3	A	(3:0)	std_logic_vector	I						
10	+	4	B	(3:0)	std_logic_vector	I						
11	5		PROD	(7:0)	std_logic_vector	O						
12	6		X	(7:0)	std_logic_vector	O						
13	7		PP	(7:0)	pp_array							
14												

```
-- Architecture concurrent statements
-- (See Embedded Text Block 3 on)
PROD(7) <= PC(4)(3);
PROD(6 downto 4) <= PS(4)(3 downto 1);

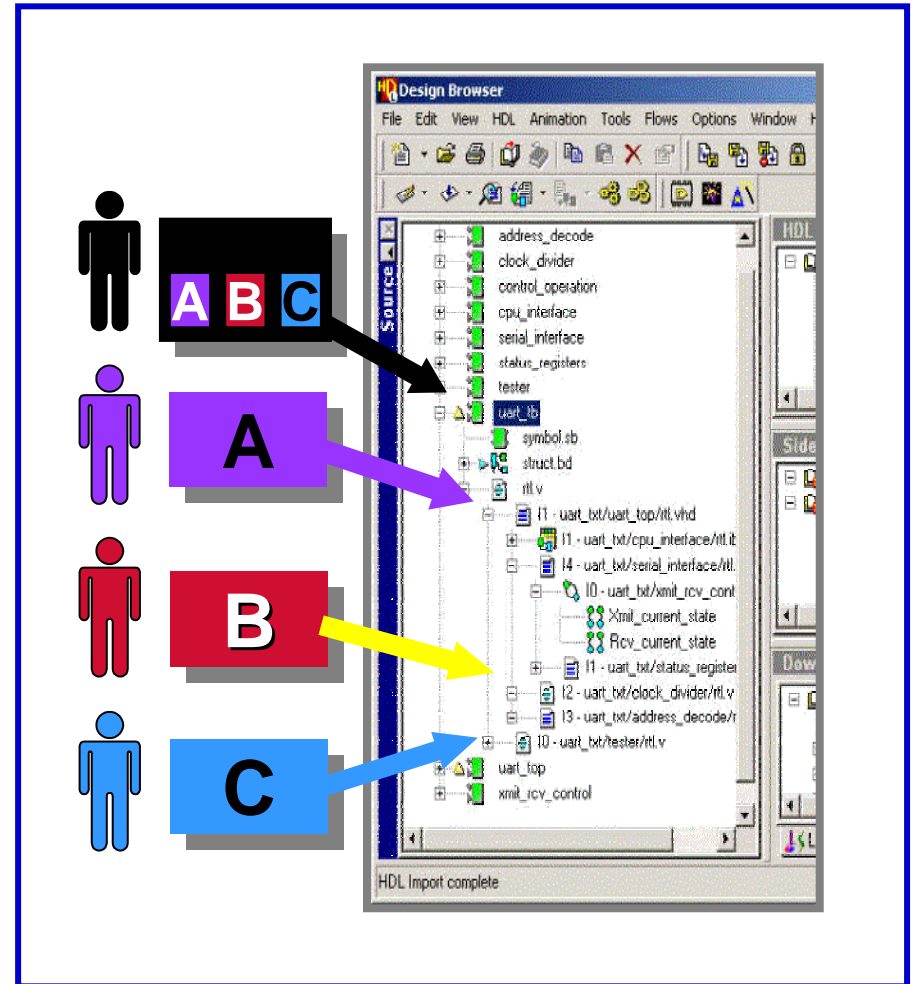
-- Instance port mappings
port map (
  A => A,
  B => B,
  PP => PP,
  X => X
);

-- Instance port mappings
I0 pp_and
port map (
  A=>PC(3)(k),
  B=>A(3),
  B(0:2)
);

g4: FOR k IN 1 TO 3 GENERATE
  I2: pp_array
  port map (
    A=>PC(3)(k),
    B=>PC(3)(k-1),
    C1=>PC(4)(k-1),
    C0=>PC(4)(k),
    S=>PC(4)(k)
  );
end generate g4;
end struct;
```

HDL Designer Series: Team Design Environment

- FPGA design teams
 - 1, 5, 10+ engineers
 - Blocks designed separately but in context of entire design
 - Version control



HDL Designer Series: Design Visualization & Documentation

Design structure

ModelSim SE PLUS 5.6b with Debug Detective

File Edit View Compile Simulate Tools Debug Window Help

100

Project Library sim

Project : mixed Now: 0 ns Delta: 0

```

//
# Loading work.proc
# Loading work.cache
# Loading work.std_logic_util(body)
# Load
# Load
# HDS
# D:/hd
osplash
# Conn
# hds_
VSIM 3
  
```

A	B	C	D	E	F	G	H	I	J	K	L
Order	Name	Bounds	Type	serial_interface	status_registers	ab1	er_out_muxcombar	conv	MCrv_control	Comments	
1											
2		Instance Ref:			11	3	2	1			
3		Frame Label:									
4		Port Map:			++						
5	1	done_rcvng		std_logic							
6	2	done_xmitting		std_logic							
7	3	rcv_bit_cnt	(2 DOWNTO 0)	std_logic_vector							
8	4	rcvng		std_logic							
9	5	read_bit		std_logic							
10	6	recvdt	(7 DOWNTO 0)	std_logic_vector							
11	7	status	(7 DOWNTO 0)	std_logic_vector							
12	8	xmitdt	(7 DOWNTO 0)	std_logic_vector							
13	9	xmitting		std_logic							
14	10	zeros	(7 DOWNTO 0)	std_logic_vector							
15	11	MW_ser_out_muxdin0l	(7 DOWNTO 0)	std_logic_vector							
16	12	MW_ser_out_muxdin1l	(7 DOWNTO 0)	std_logic_vector							
17	13	MW_ser_out_muxdin2l	(7 DOWNTO 0)	std_logic_vector							
18	14	MW_ser_out_muxdin3l	(7 DOWNTO 0)	std_logic_vector							
19	15	clear_flags		std_logic							
20	16	clk		std_logic							
21	17	data_in	(7 downto 0)	std_logic_vector							
22	18	enable_write		std_logic							
23	19	rst		std_logic							
24	20	sample		std_logic							

Block diagrams

work/TopOnly (Block Diagram)

File Edit View Diagram Simulation Window Help

Panel0 Spy_On Some Signals

work/control_operation/Current_state (Read-only) (State Diagram)

File Edit View Diagram Simulation Animation Window Help

Simulation time: 1015000

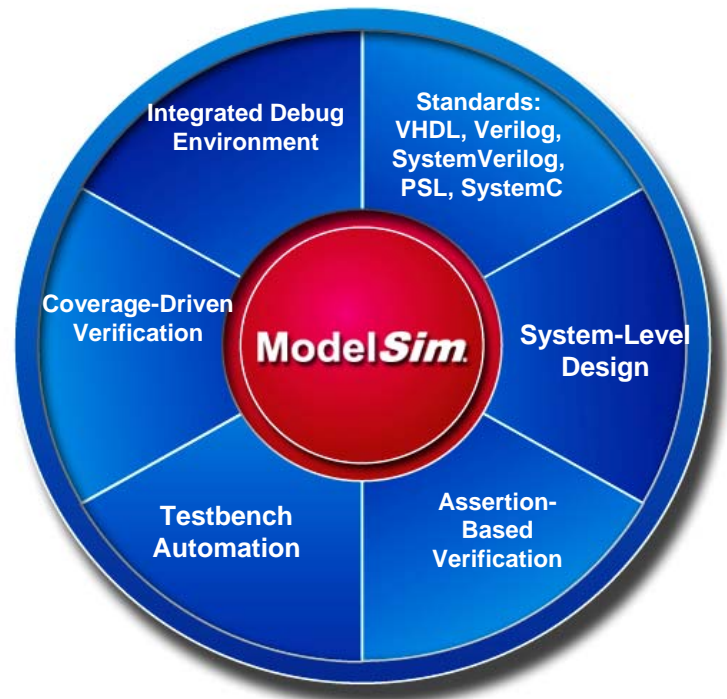
Interface-based design

State diagrams

ModelSim 6.0

Verification Environment

- Most widely used simulator in the world
 - **#1 in Mixed-HDL simulation**
- Only unified verification environment supporting all major standards
 - **VHDL, Verilog, SystemVerilog, SystemC and PSL**
- Complete path from simulation to “Scalable Verification”
- Dedicated to high-performance
- Powerful and easy-to-use
- Award-winning Technical Support
- Best price/feature/performance



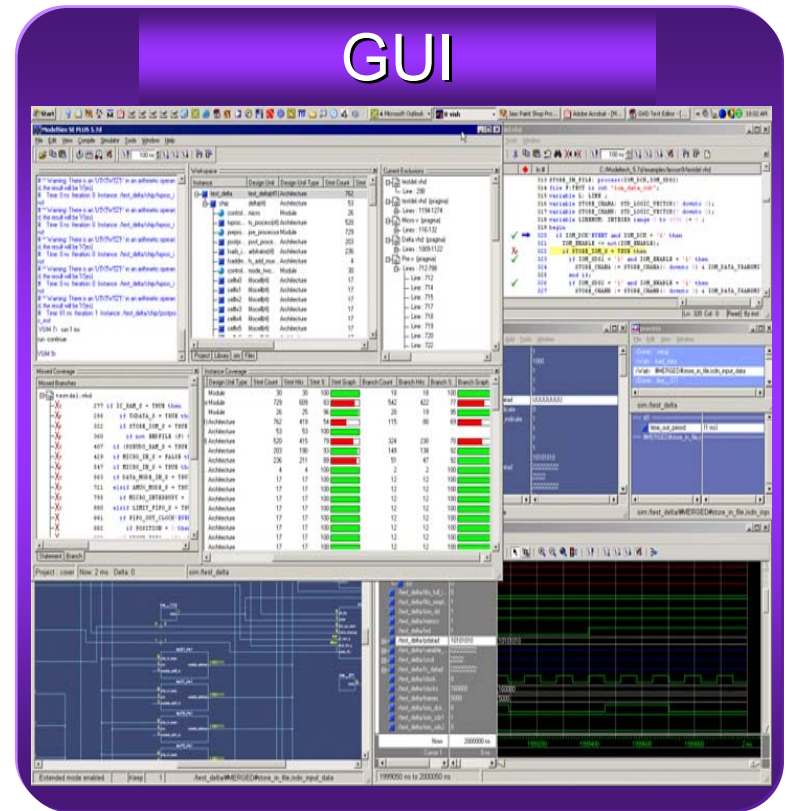
ModelSim 6.0

Verification Highlights

- Add Verilog PSL to existing VHDL support
- Functional coverage
 - **Based on PSL**
- SystemC enhancements
- More performance
- More SystemVerilog
 - Nearly all design constructs
 - DPI
- Highly intelligent GUI
- Shipping now (August 2004)

ModelSim 6.0 Modernized GUI

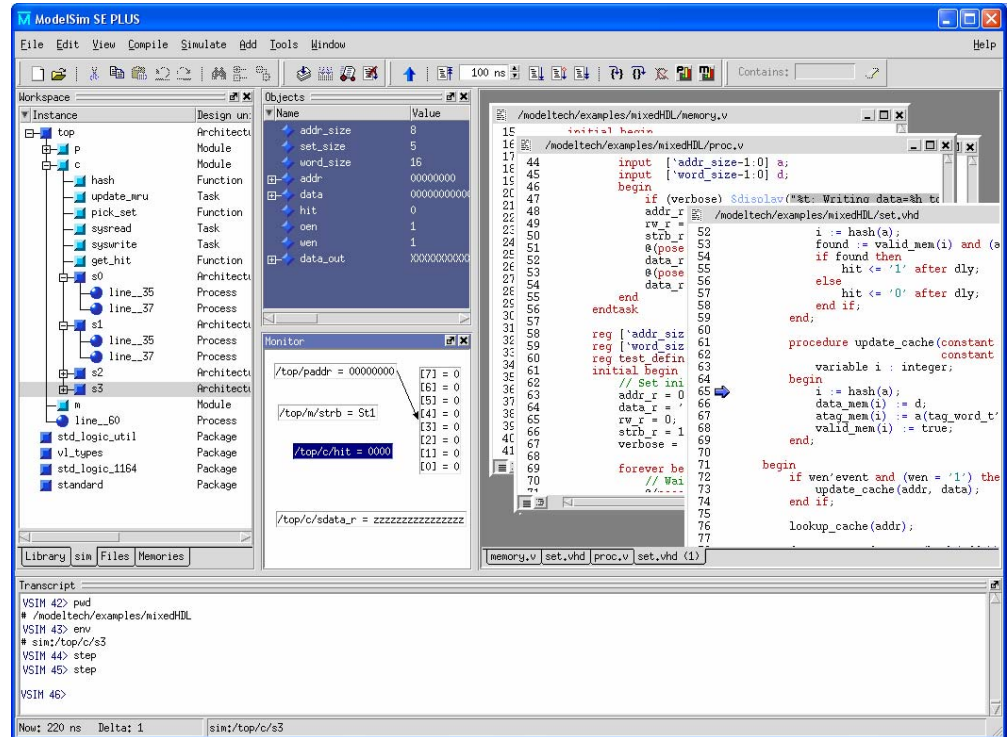
- Support for new methodologies
 - Assertion browser supports control and debugging with ABV
 - Functional coverage browser provides loading, control and reporting of functional coverage directives
- ModelSim is recognized as having best native GUI in the industry...
 - Best interactive debugger
 - All-in-one
 - Language Independent
 - Tcl/tk expandability



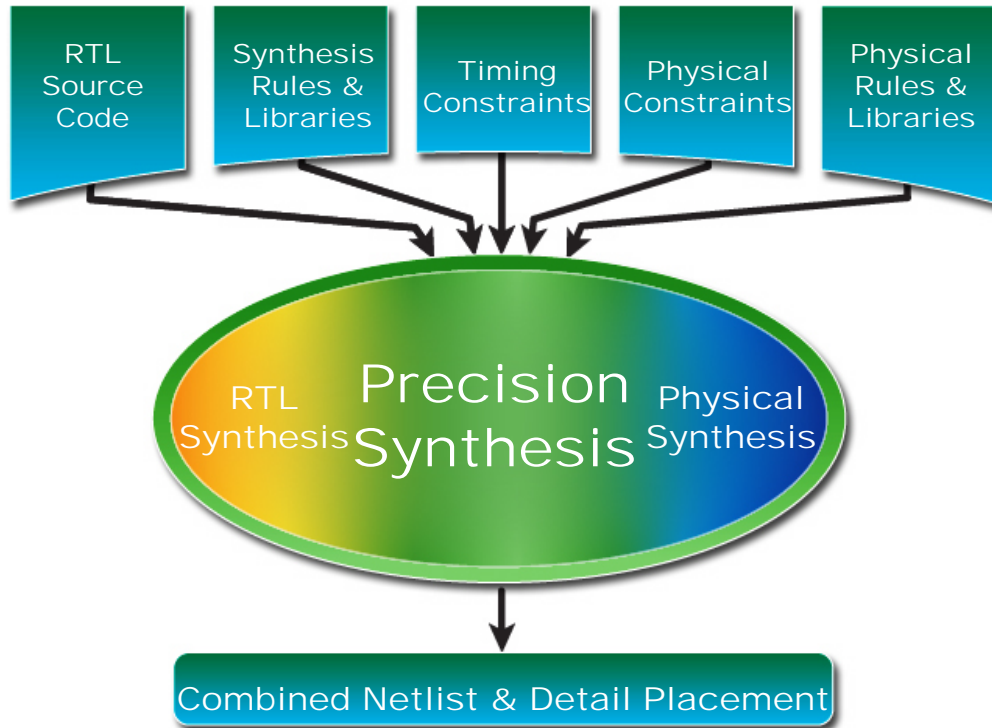
ModelSim 6.0

Improved User Interface

- New window layout
- Reorganized display of data
- Uses fewer windows
- Improved window manager
- More efficient use of screen real estate



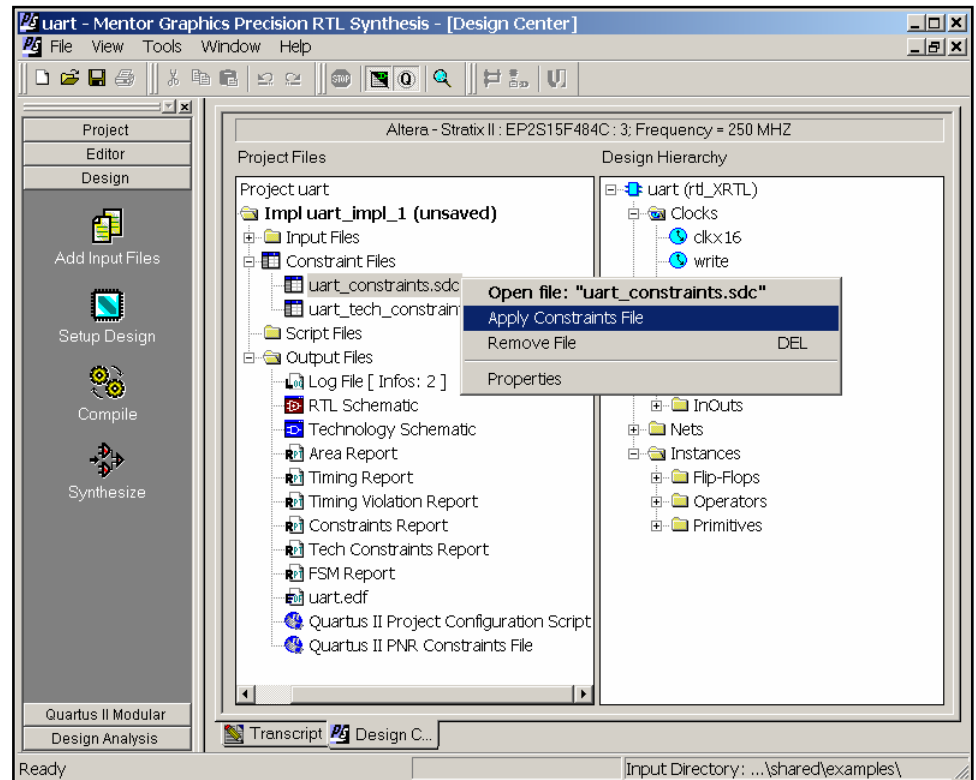
Precision Synthesis: Integrated Logical & Physical Synthesis



- Productivity enhancing synthesis tool suite
 - RTL + Physical
- Addresses design challenges of advanced, complex devices
 - Predictable design schedules
 - Reduced number of design iterations
 - Achieves timing closure

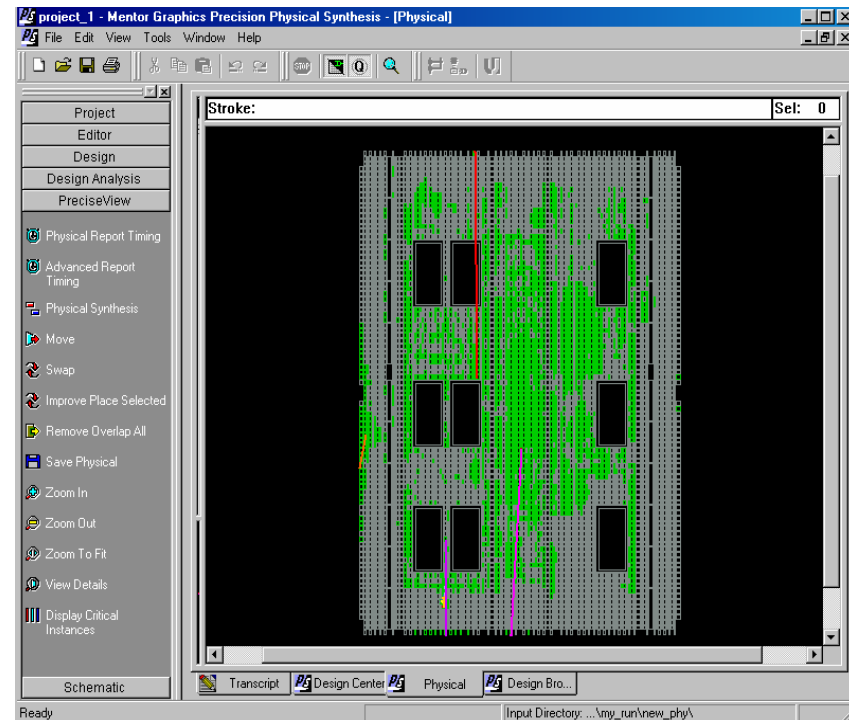
Precision RTL Synthesis

- Ease of use and competitive quality of results (QoR)
 - Incremental timing analysis allows rapid constraint debug iterations
 - Eliminates the need to re-run synthesis, or even a full static timing analysis again
 - Fewer design iterations
 - Precision RTL finds and incrementally fixes timing closure issues, early
 - Easy migration from ASICs
 - Standard SDC constraint file format



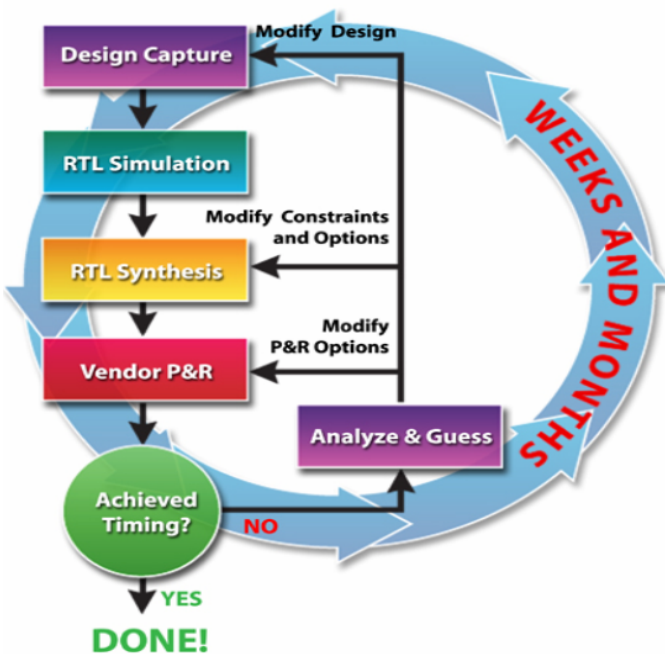
Precision Physical Synthesis

- The market leader that integrates RTL and Physical domain knowledge
 - Reduces design iterations by linking physical data with logic synthesis
 - Improves timing convergence by enhancing design analysis with ease of use
 - Intelligent and easy-to-use timing analysis
 - Cross-probe between RTL code, schematic, physical and timing views
 - Improves performance by interactively optimizing the placed design
- Supports Altera devices beginning with May 2004 release
 - Stratix, Stratix GX and Cyclone

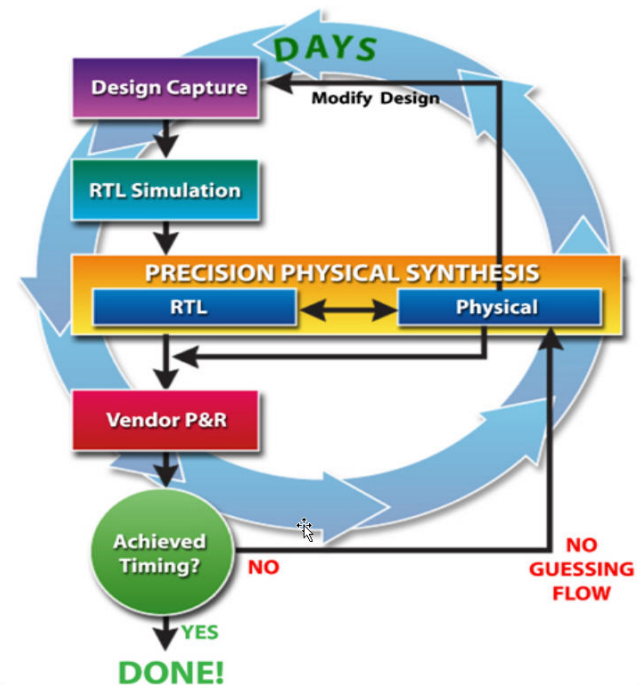


Why Precision Physical Synthesis?

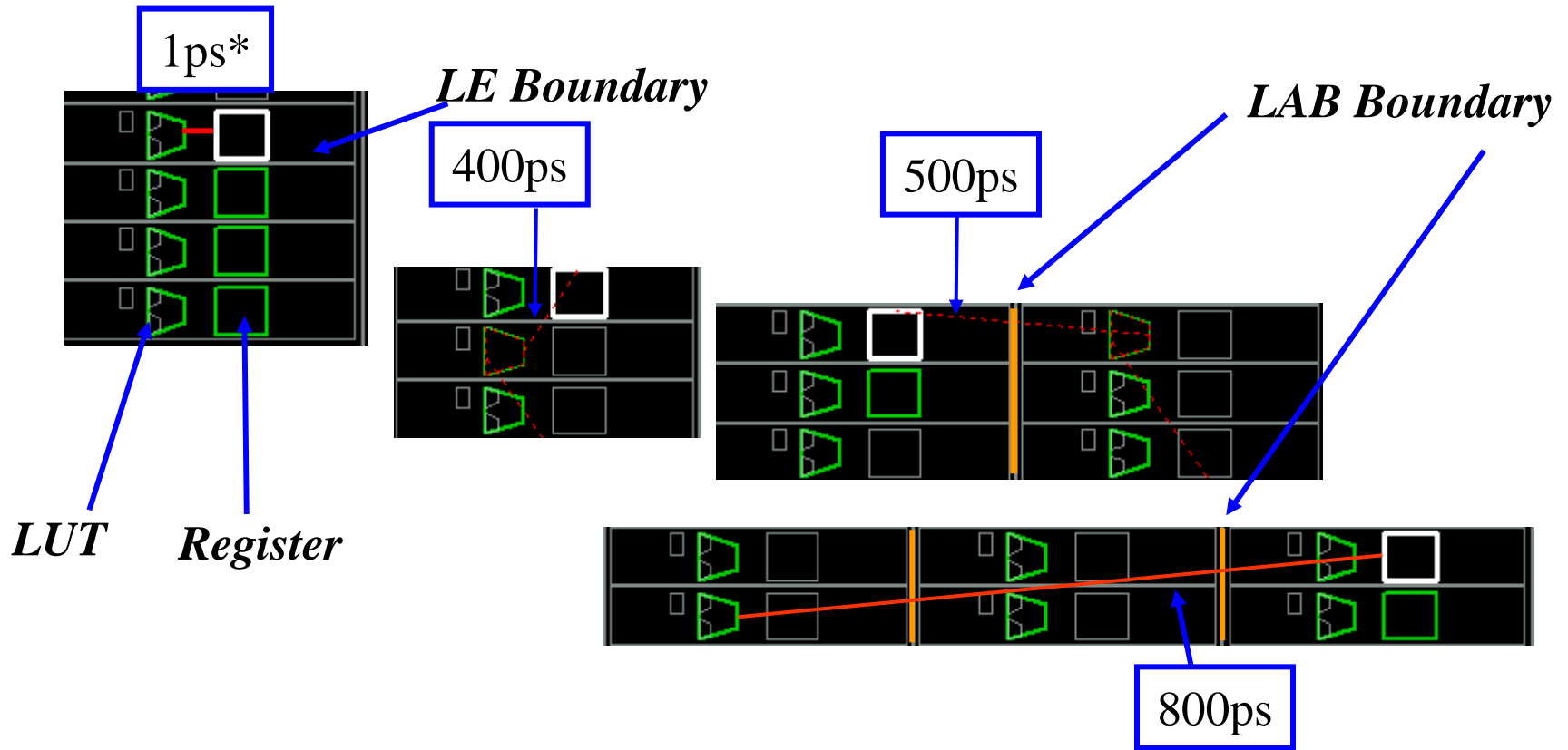
- Traditional approach to timing convergence
 - Iterative methods
 - Writing/re-writing RTL code
 - Modifying constraints/attributes
 - Multiple synthesis runs
 - Multiple P&R runs
 - Floorplanning



- With Precision Physical
 - Faster time to performance
 - Uses exact knowledge of placement / physical delays
 - Fast, incremental, deterministic
 - Placement optimization based on physical delays
 - Available resources guide optimization



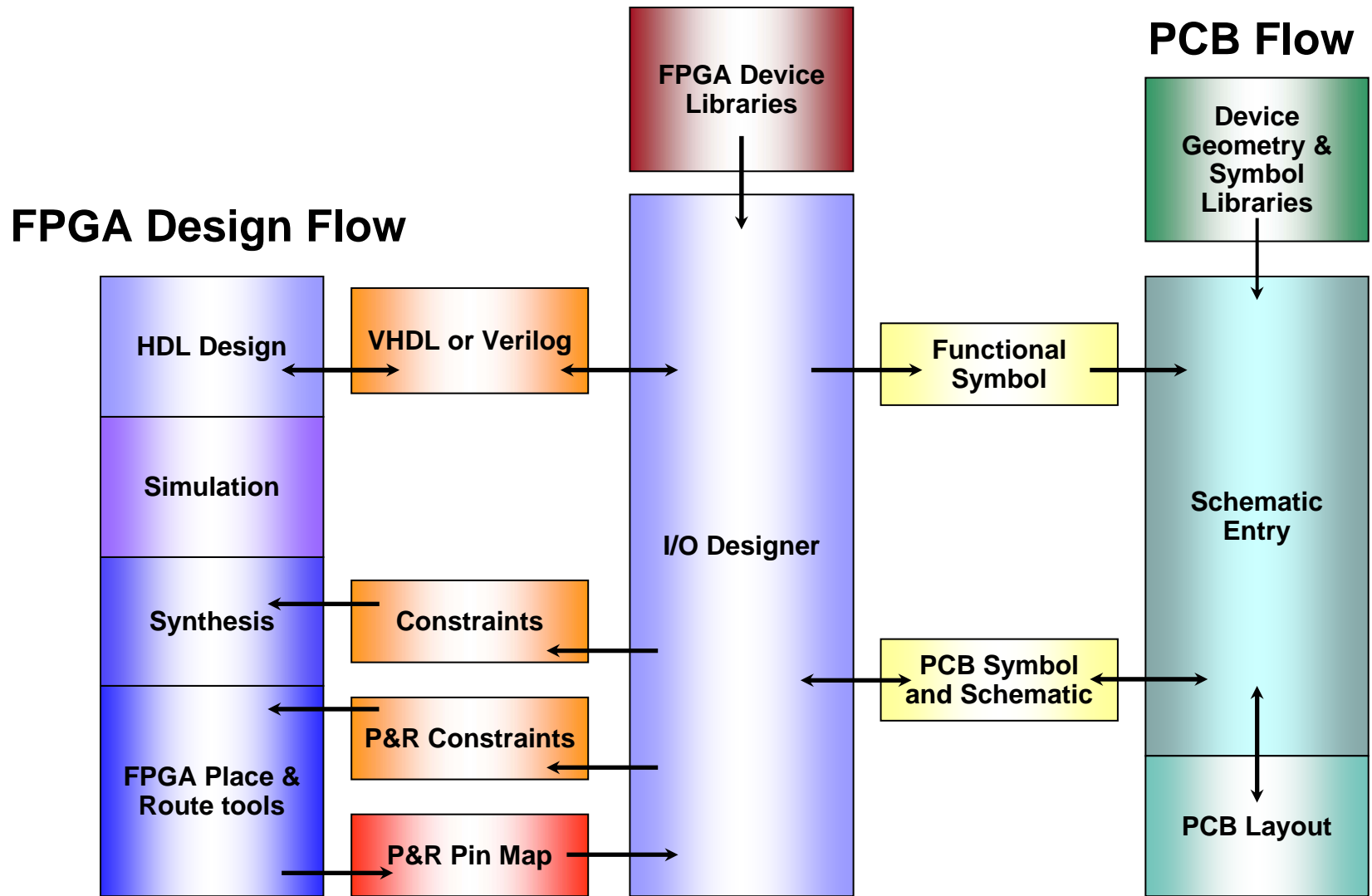
Traditional Floorplanning Fails



Delay is not a regular function of distance at a detailed placement level

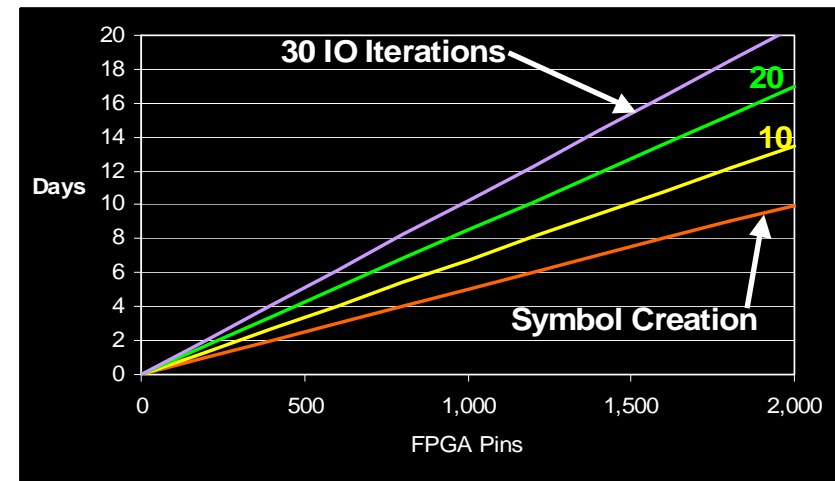
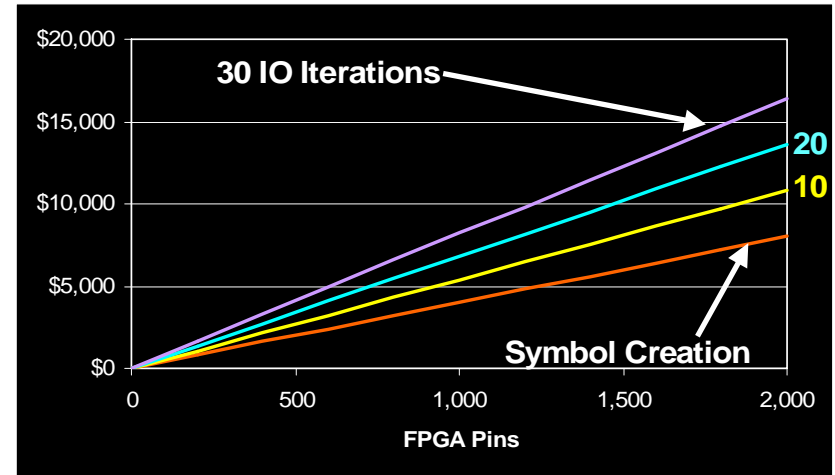
*Stratix-specific delay values

I/O Designer: Concurrent FPGA-PCB Design



I/O Designer: Productivity

- Automatic FPGA – PCB symbol integration
 - Eliminates symbol creation and maintenance costs
 - Eliminates man-weeks of effort
 - Eliminates manual data entry issues
 - Promotes correct by construction

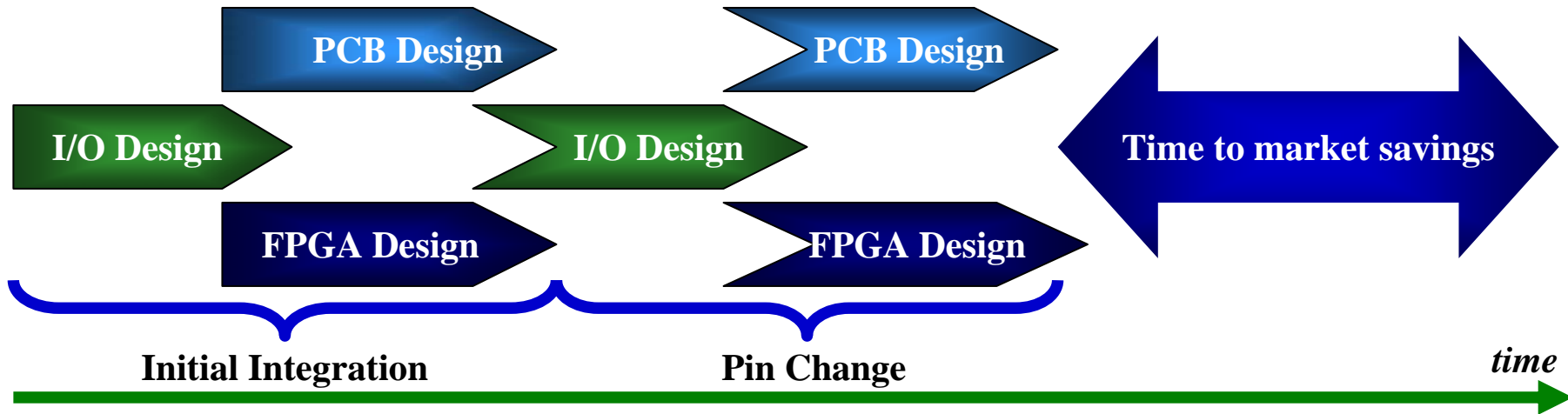


I/O Designer: Serial versus Concurrent

Traditional Flow:

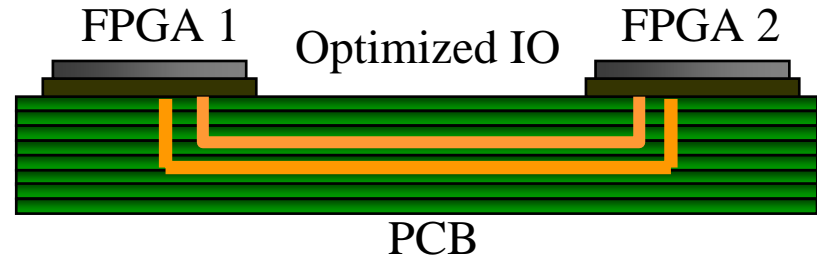
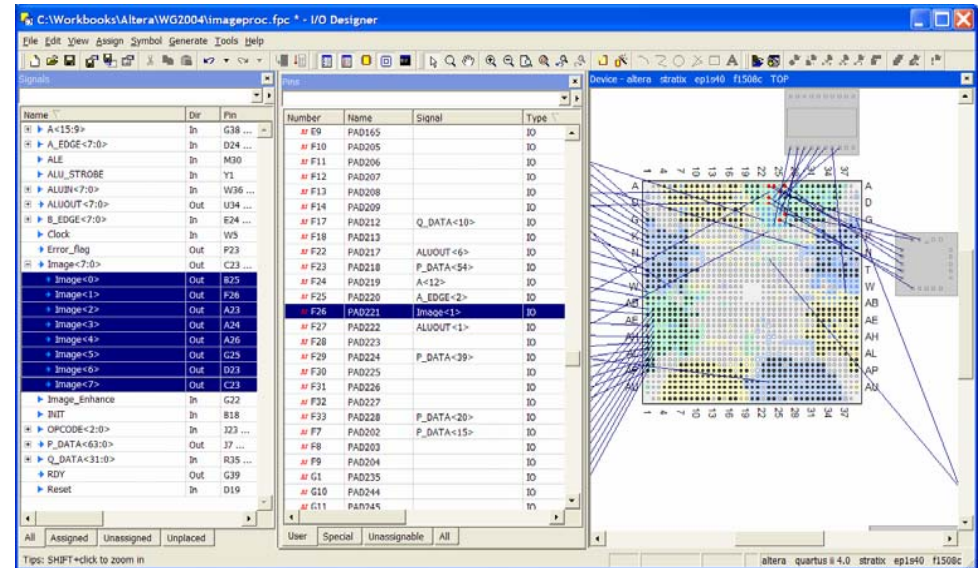


I/O Designer Flow:



I/O Designer: PCB Manufacturing Optimizations

- Multi-component, view-driven I/O design and optimization
 - Minimize crossovers
 - Unravel busses
 - Assign compatible I/O standards across multiple FPGAs
 - PCB design leads FPGA
 - Drives FPGA design flow
 - FPGA leads PCB
 - PCB floorplanning drives PCB design flow



Design Project Saving > 1 Month per complex FPGA on a PCB

Summary

- Mentor Graphics has all the tools you need to handle your next advanced Altera FPGA design
 - HDL Designer
 - ModelSim
 - Precision Synthesis
 - I/O Designer
- Industry leading tools
- Unique functionality
- Significant productivity gains

To Learn More

- Go to <http://www.mentor.com>
- Visit the Mentor Graphics Booth

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