Designing Video Surveillance Equipment Using Altera and TI Technology

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Agenda

- Digital video recorder (DVR) market and technical overview
- Key system diagrams
- Altera solutions for DVR application
  - Video intellectual property (IP) library suite
  - Video compression IP
  - Interface IP
- Altera and Texas Instruments (TI) solution for DVR applications
- Development kit

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DVR Market and Technical Overview

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DVR Market Dynamics

- Strong growth expected
  - Increasing public security consciousness
  - Updating old analog systems
  - Extending into new vertical markets (e.g., banking, retail, roads, prison)
- Asia Pacific manufacturers are playing important role
  - Lower price wins the market share
  - Increased investment in R&D

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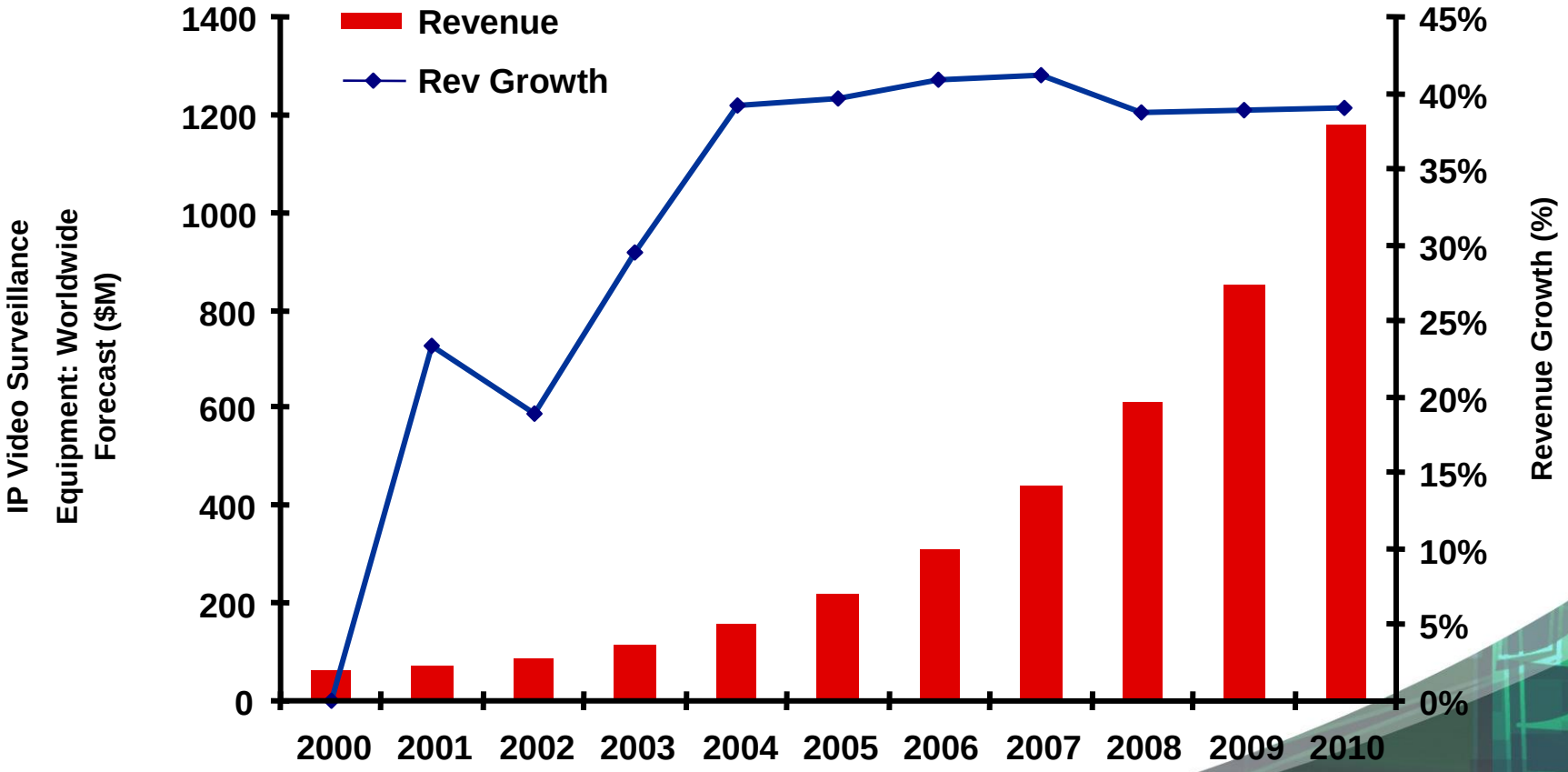
System Revenue Forecasts



Source: Frost & Sullivan 2005

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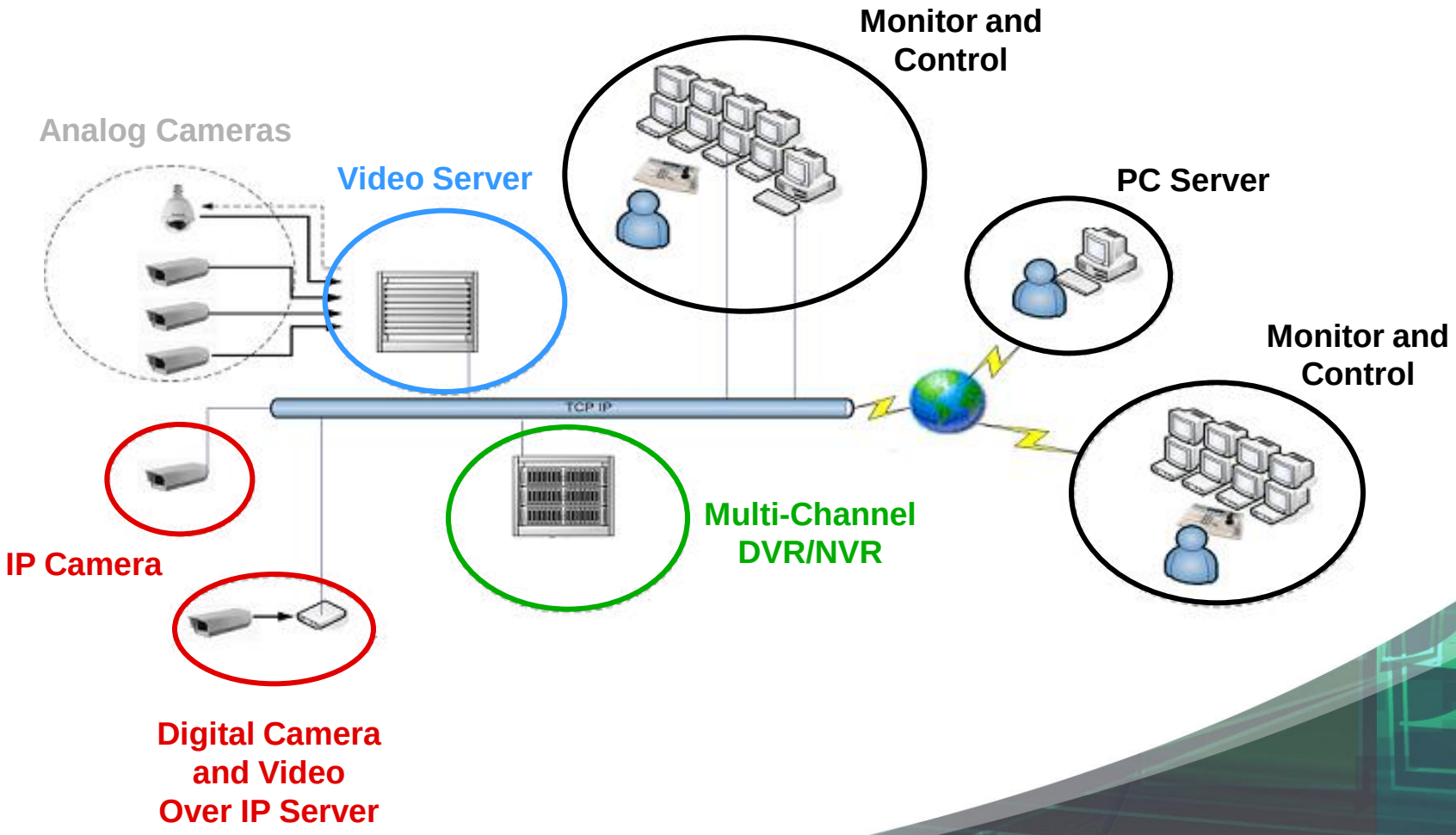
Technical Trends

- New compression algorithm improve video quality and saves storage space
  - M-JPEG to MPEG4 to H.264
- Increasing number of IP-based systems
  - Distributed capture and centralized storage
  - IP-based camera and IP video server
  - Network DVR
- Further improvements on intelligent image analysis and accurate video motion detection algorithm

IP Network Video Surveillance System



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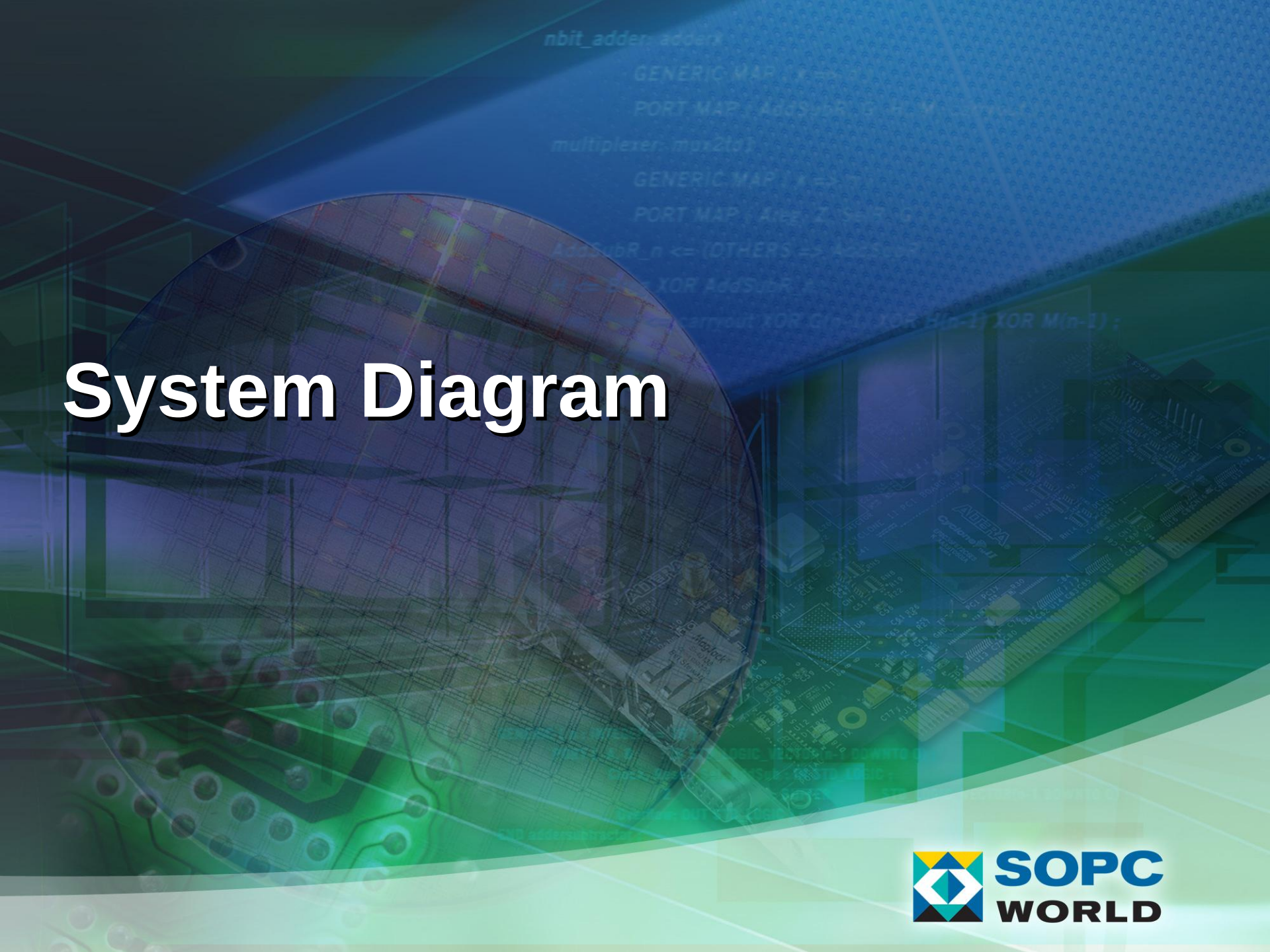
System Diagram



Typical Platforms

- Hardware compression DVR system
  - Embedded DVR (stand-alone)
  - PC/IPC-based DVR system
- Software compression DVR system
  - PC/IPC-based system
- Video server
- IP camera
- Network DVR

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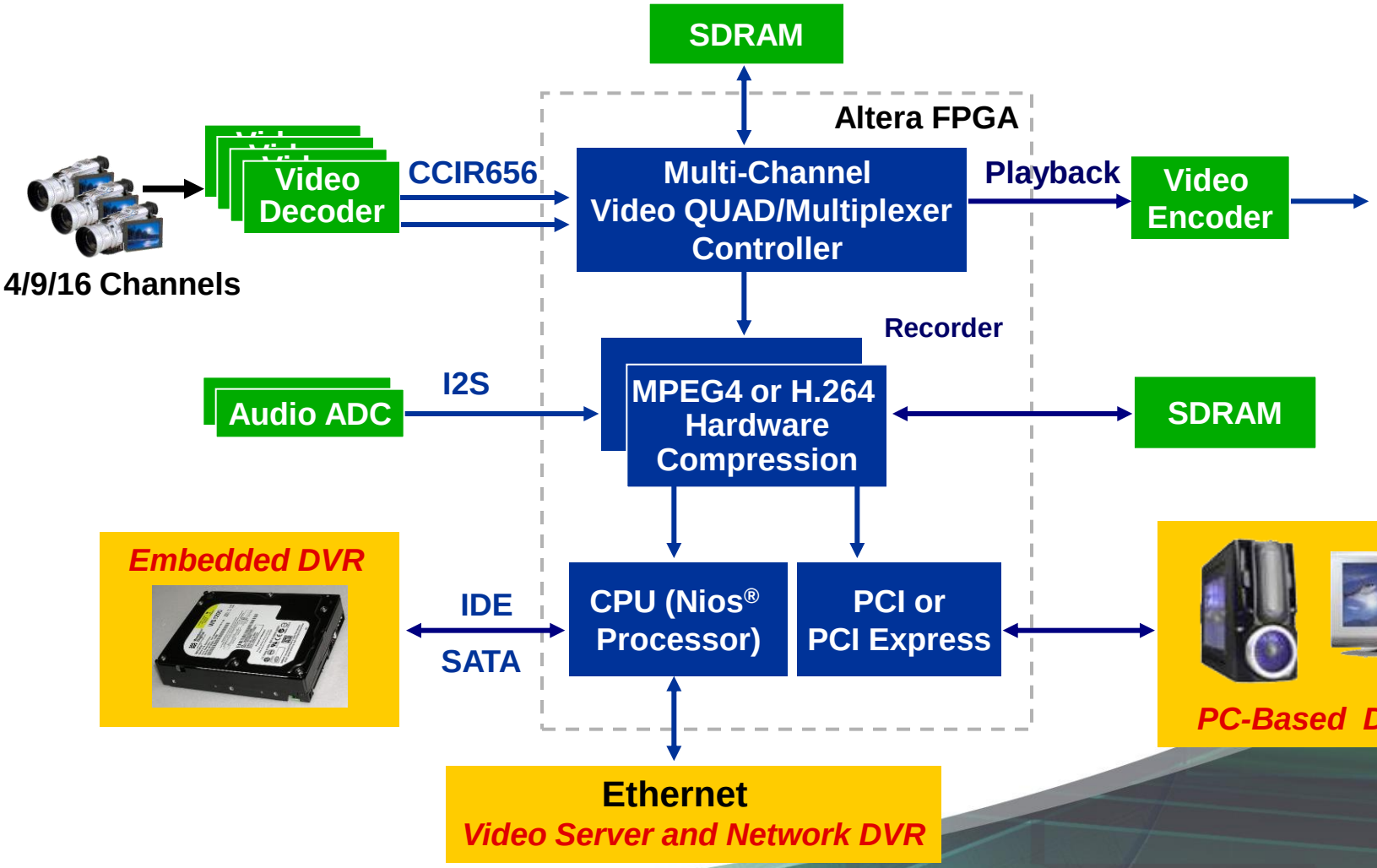
DVR System: Hardware Compression



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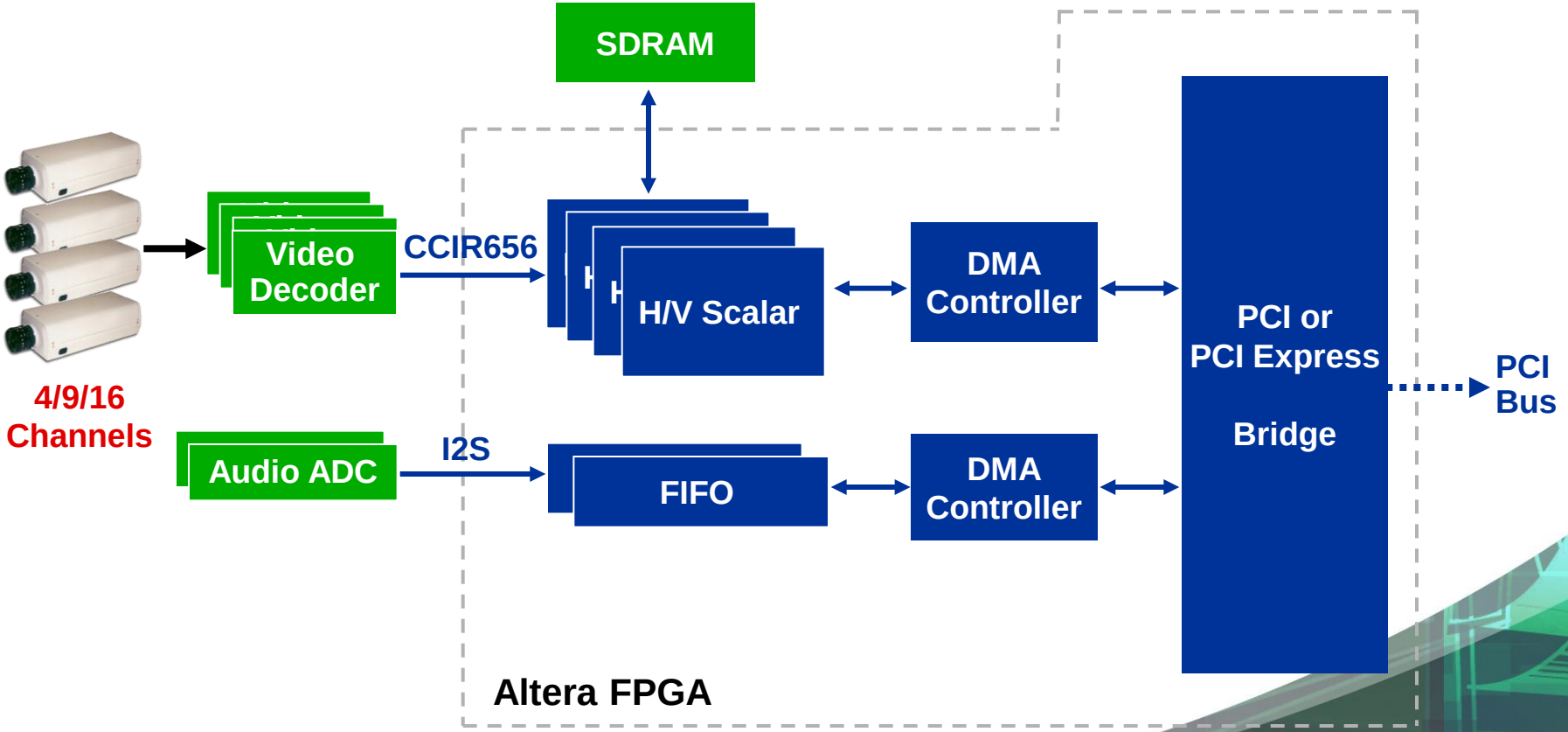
PCI Based DVR: PC Software Compression



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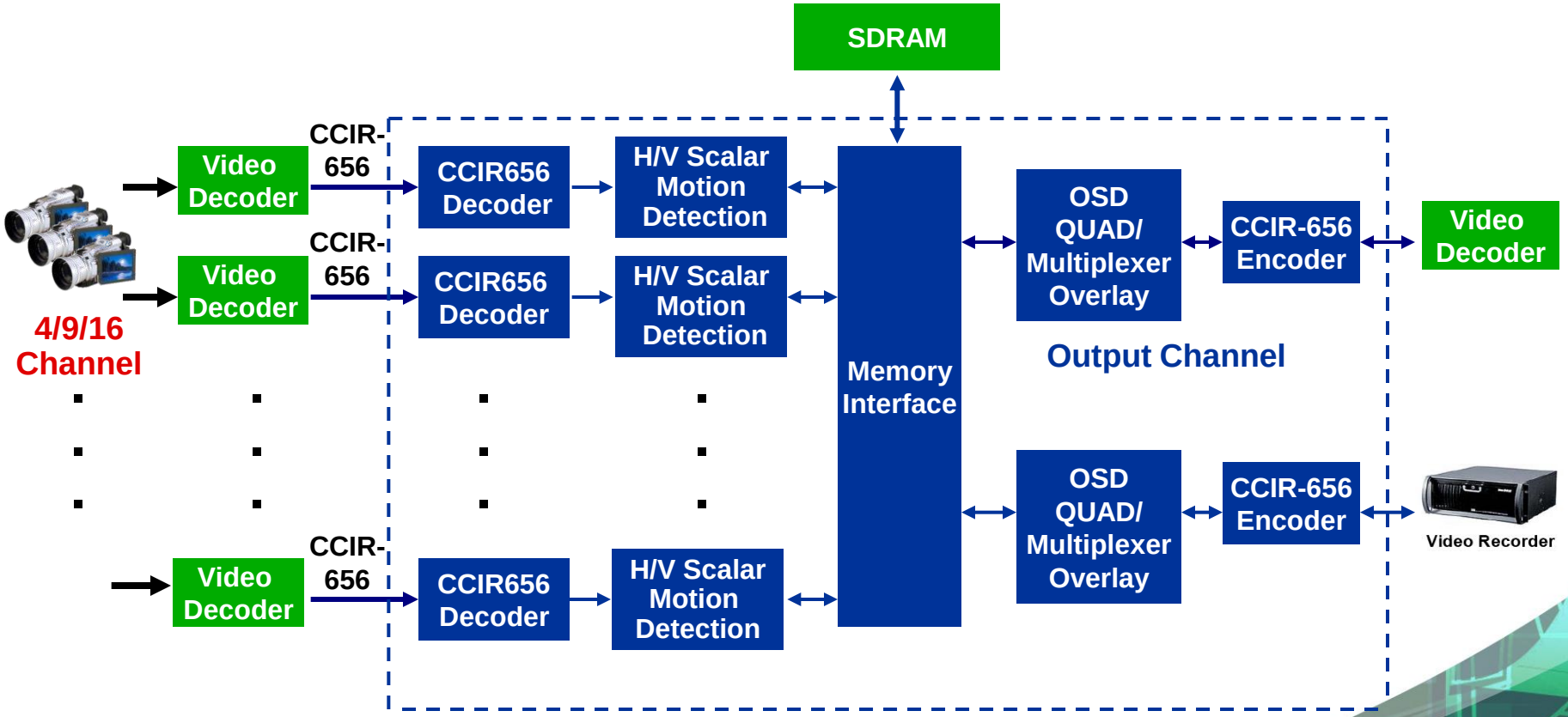
Video QUAD/Multiplexer Controller Diagram



Other Key Functions:

- PIP
- Overlay or Blending

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Altera Solutions

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Altera Video Surveillance Solutions

- Video compression algorithms
- Video IP library and imaging reference design
- Memory controller and bus interfaces
- Development kits
- Digital signal processing (DSP) system and FPGA design tools/utilities (see demo area)

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Altera Video Compression Solutions

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Choosing the Compression

Feature	M-JPEG	M-JPEG2000	H.264
Compression	10-20	10-20	25-50
Bit Rate (Mbps)	6-12.5	6-12.5	2.5-5
Motion Compensation	No	No	Yes
Variable Bit Rate (VBR)	Yes	Yes	Yes
Constant Bit Rate (CBR)	No	Yes (Instant Tier 2)	Yes (Buffered)
Latency	Low	Low to Medium	Medium to High
Blocking Artifacts	Yes	No (Full Frame)	Yes
Lossless Support	No	Yes	No
RGB Support	Yes	Yes	No
Stream Scalability	No	Yes	No
Relative Cost	1x	3x	2x

Note: MPEG-4 AVC (Main Profile)
- **Higher Compression**
- **Higher Complexity (3-4x)**

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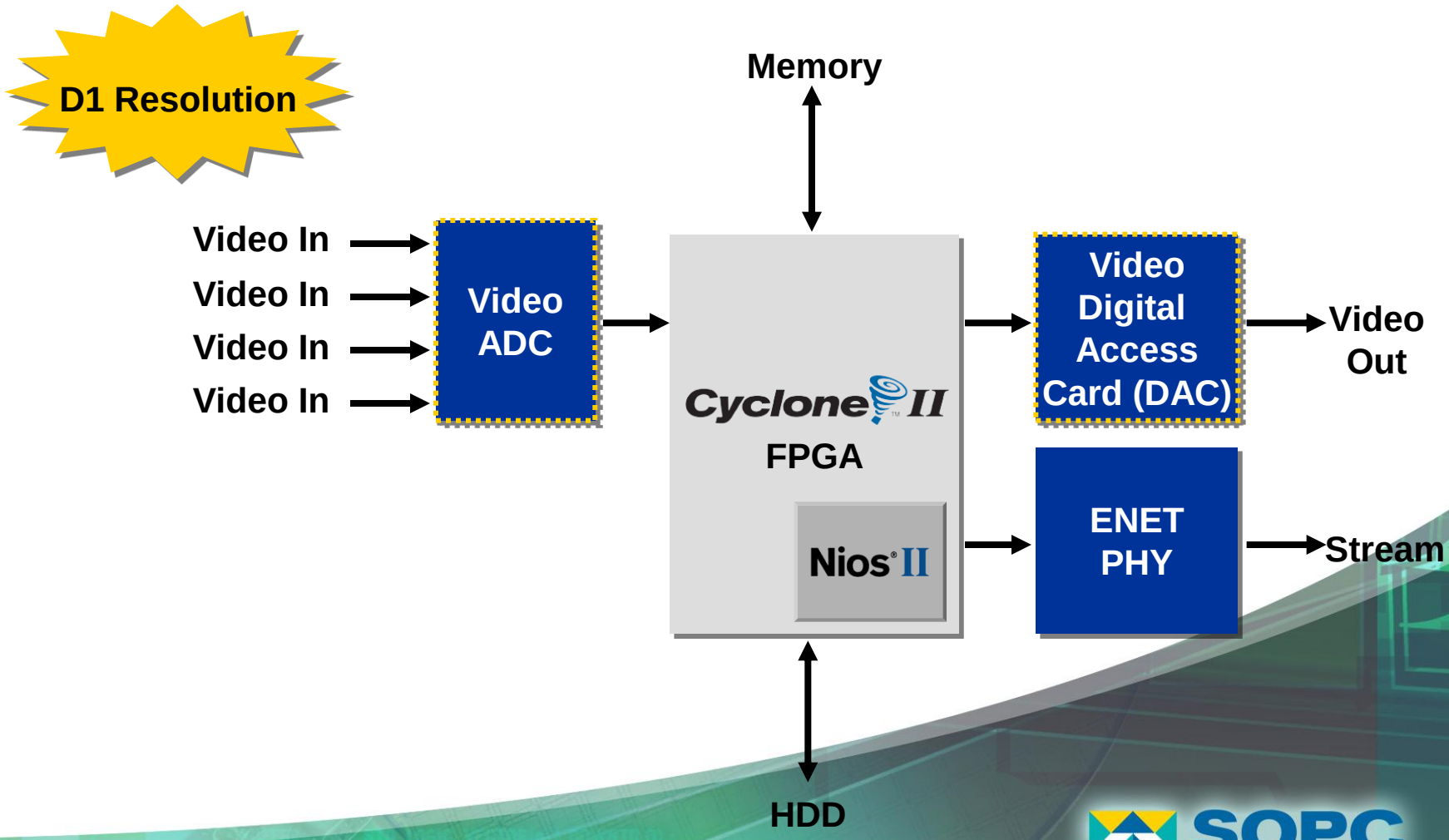
Case Study: Video Surveillance Using Cyclone® II FPGAs



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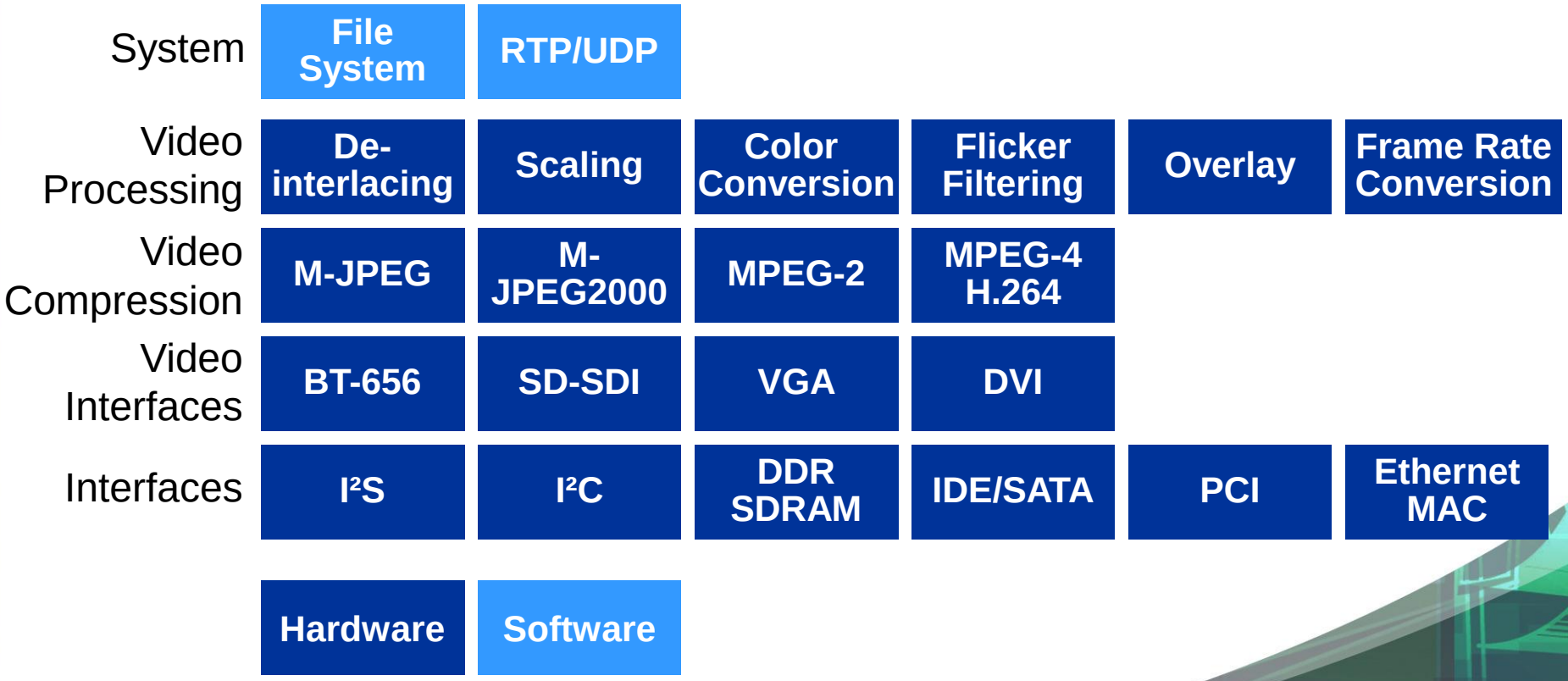
Video Surveillance Building Blocks



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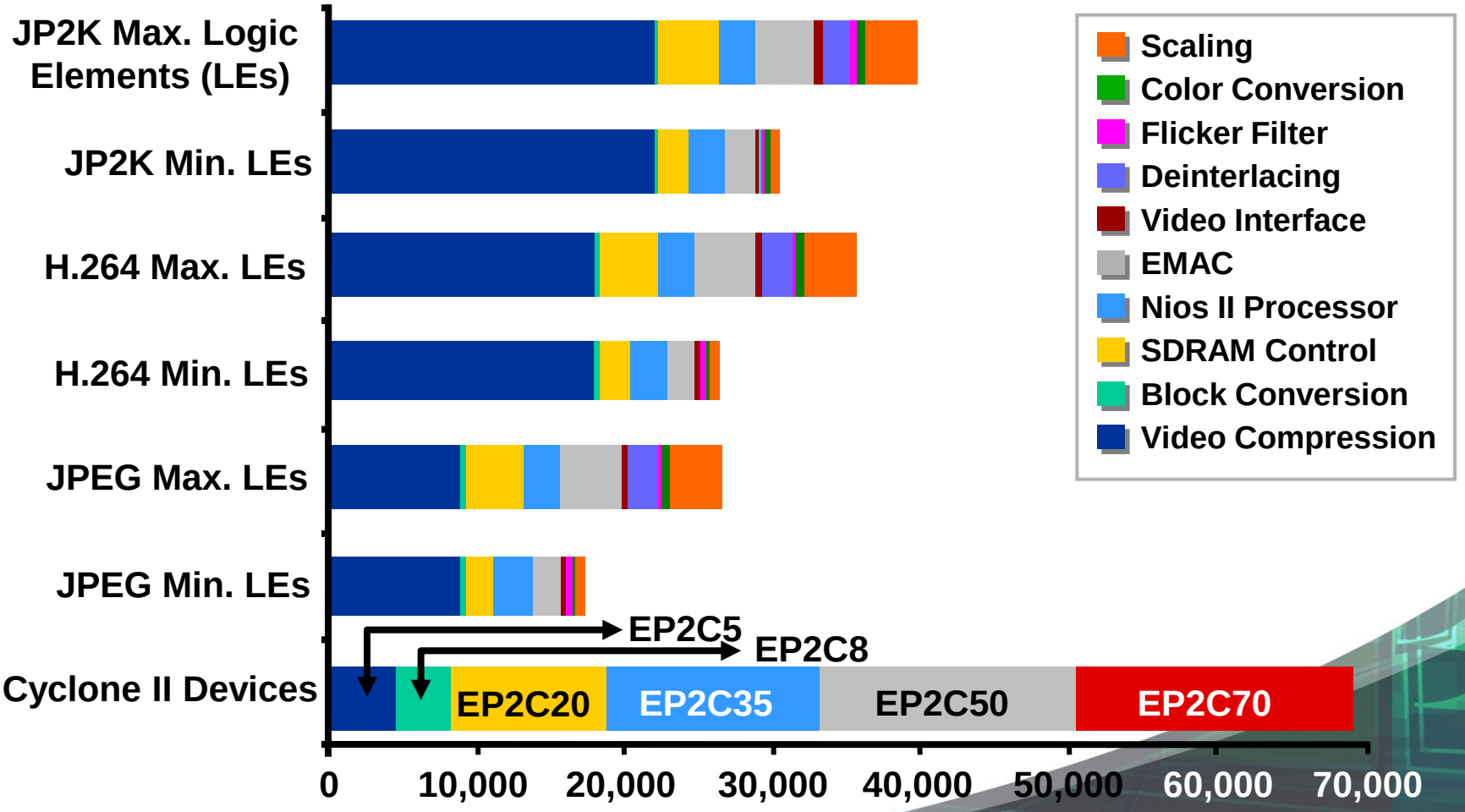
Complexity Analysis: Logic



Applicable for real-time full D1 processing

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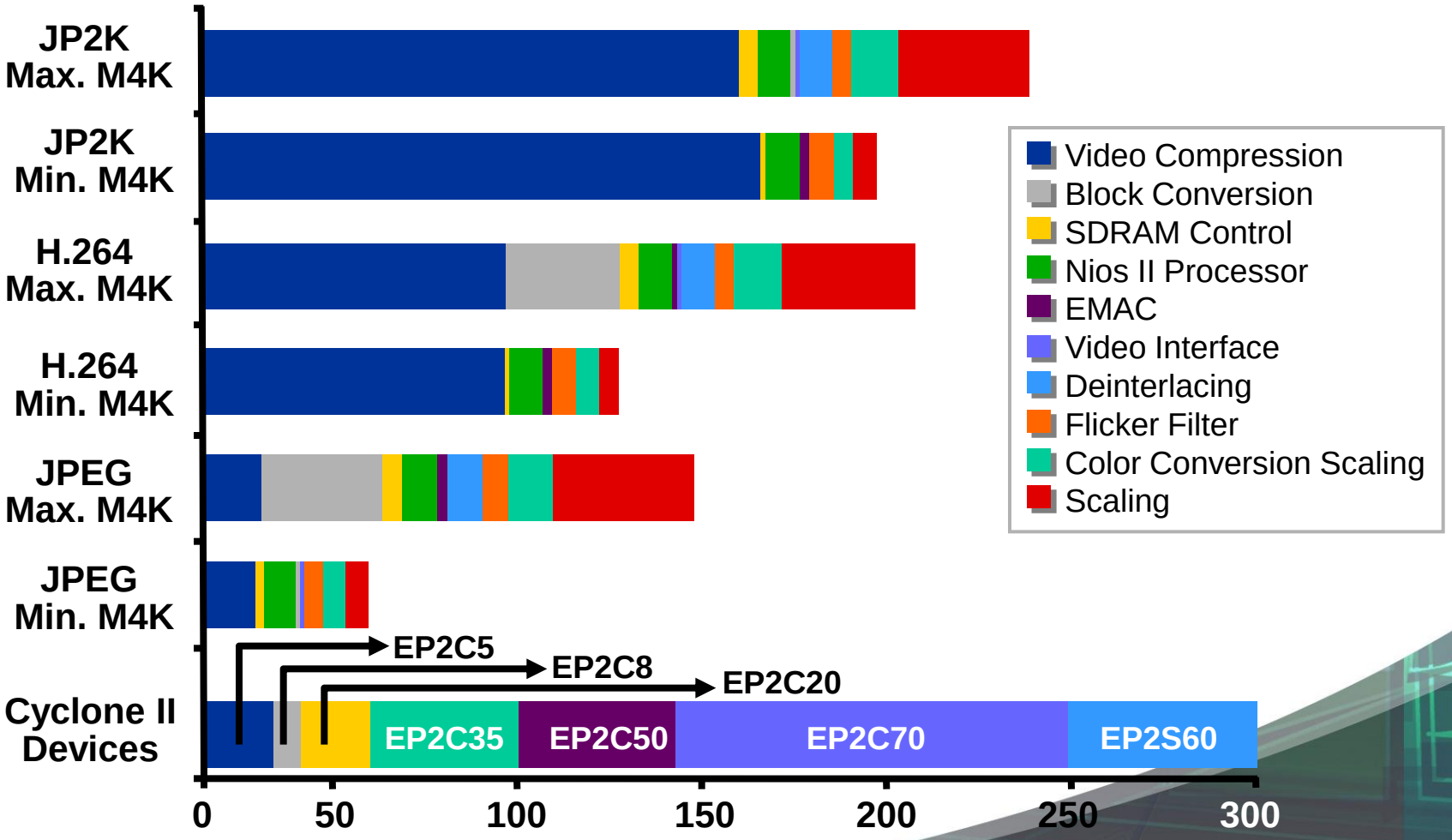
Complexity Analysis: Memory



Applicable for real-time full D1 processing

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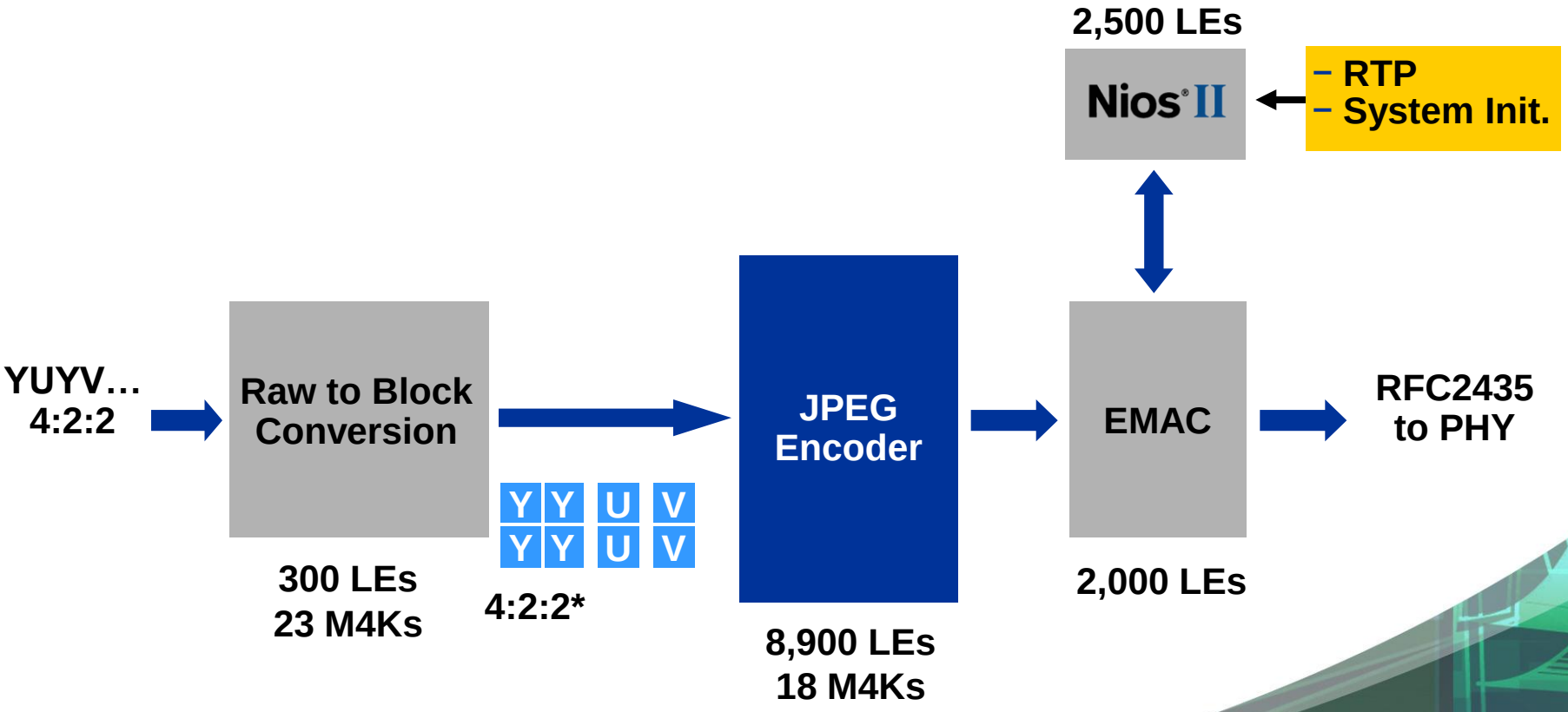
M-JPEG System



* 4:2:0 is also possible.

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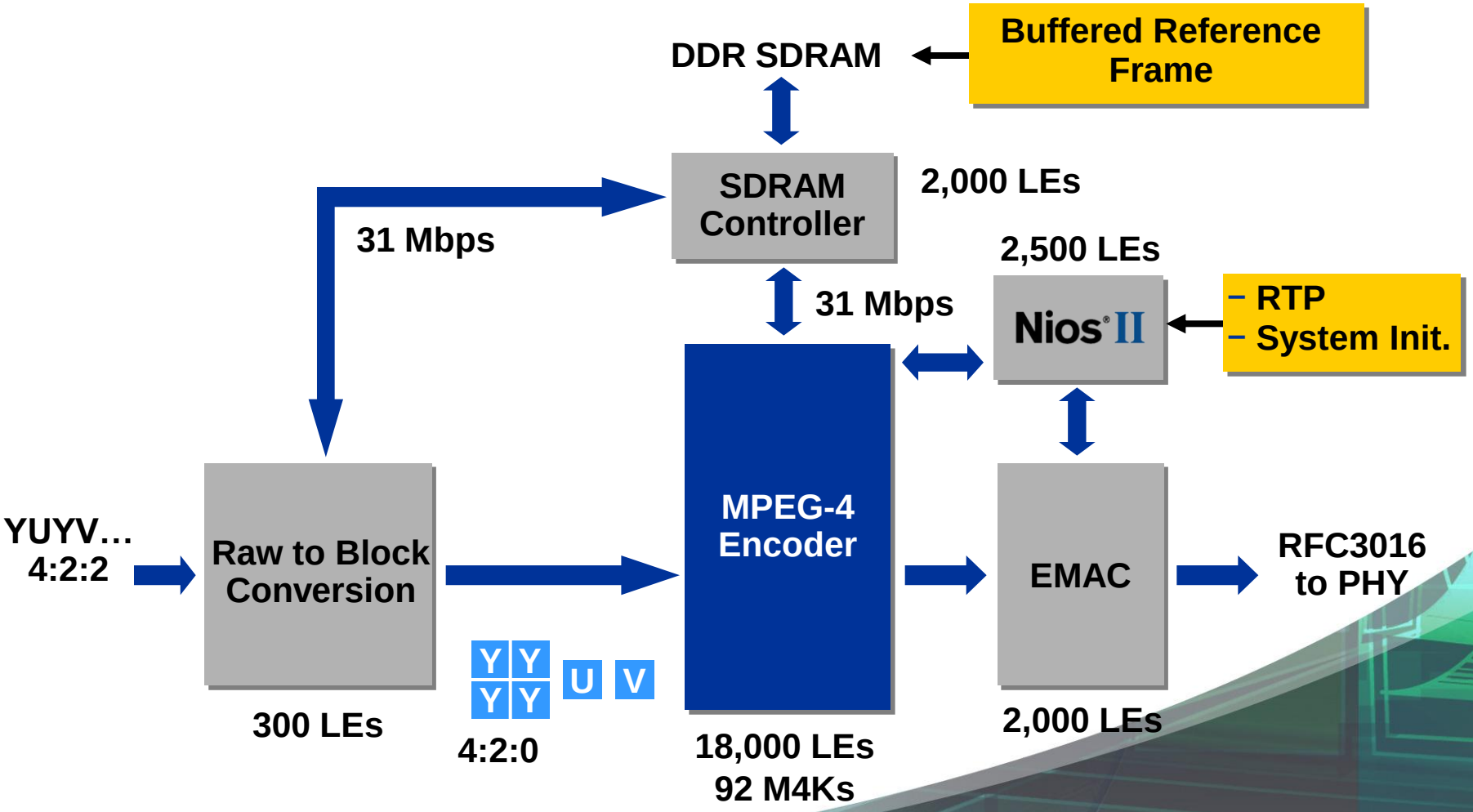
MPEG-4 Simple Profile System



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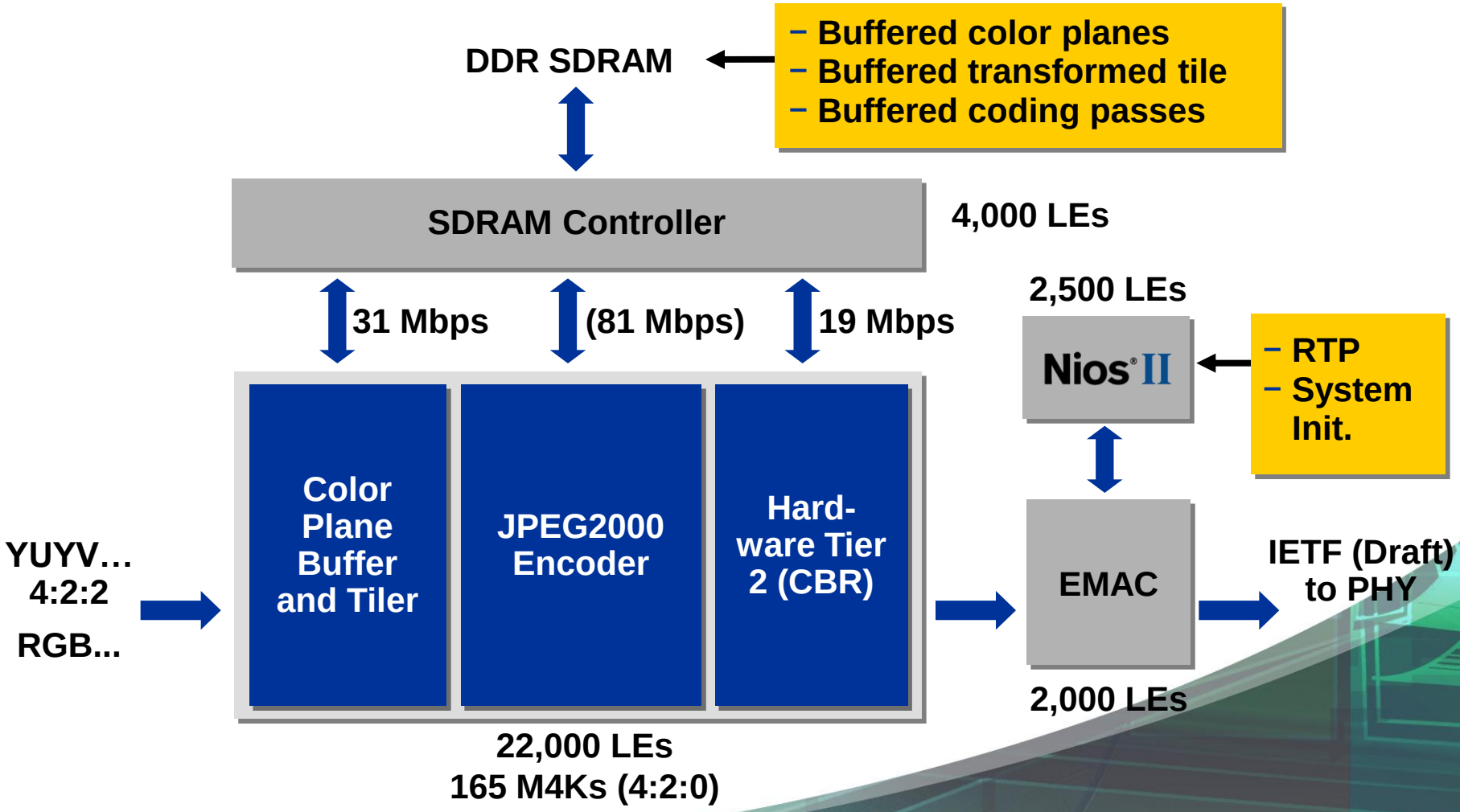
M-JPEG2000 System



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Case Study Summary

Requirement	M-JPEG	MPEG-4 SP	M-JPEG2000
Components:			
– Raw to Block	Yes	Yes	No
– Encoder	Yes	Yes	Yes
– SDRAM Controller	No	Yes	Yes
– Ethernet MAC	Yes	Yes	Yes
– Nios II Processor	Yes	Yes	Yes
LEs	14,000	23,000	32,500
M4Ks	52	105	183
SDRAM Bandwidth	0	62 Mbps*	131 Mbps
Cyclone II	EP2C20C8	EP2C35C8**	EP2C70C8
Frequency	16 MHz	100 MHz	80 MHz

- **Reducing the Bandwidth Is Possible by Using M4Ks for Raw to Block Conversion**

**** $25 Volume Price**

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H.264 Video Encoding

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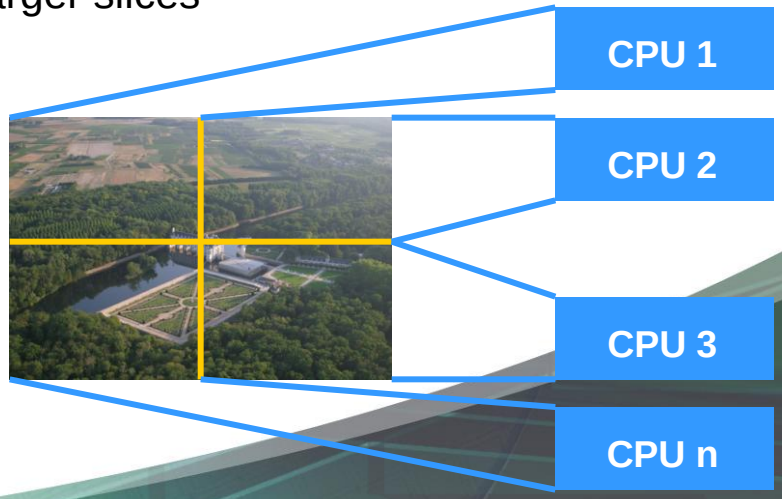
H.264 Video Compression

- JPEG, JPEG2000, MPEG-2, H.263, MPEG-4 part 2, MPEG-4 part 10/H.264 AVC all used in security/surveillance industry
- H.264 compression rates = 2x faster than competing standards at comparable quality
- Penalty is that H.264 encoding is extremely computationally intensive

FPGAs Are Ideal for H.264

- MPEG4-AVC is heavily computing-hungry
  - Processor limited by internal architecture (with 8 internal multipliers, can perform 8 multiplications per cycle)
    - TI DM6446 DSP requires 1-GHz clock for standard definition (SD) 30-fps encode
  - FPGA is highly scalable, supports 100 multiplications per cycle
- Tasks parallelization is mandatory
  - Several processors needed to process picture slices, easier to compute
  - FPGA can process bulk picture or larger slices



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H.264 Solution #1

- Primary lead provider: CAST
  - Right performance level for VS
    - Baseline, SD/D1 at 30 fps
  - Available today
    - Encoder, decoder, multi-channel encoder
  - Efficient implementation
    - ~20K LEs
  - Existing Altera customer engagements

H.264 Solution #2

- New partner: 4i2i
  - Right performance level for VS
    - Baseline, reference design = 3x [SD + common intermediate format (CIF)] at 30 fps
  - Available today
    - CODEC, multi-channel
  - Efficient implementation
  - DVR reference design in debug

Altera Video IP Functions

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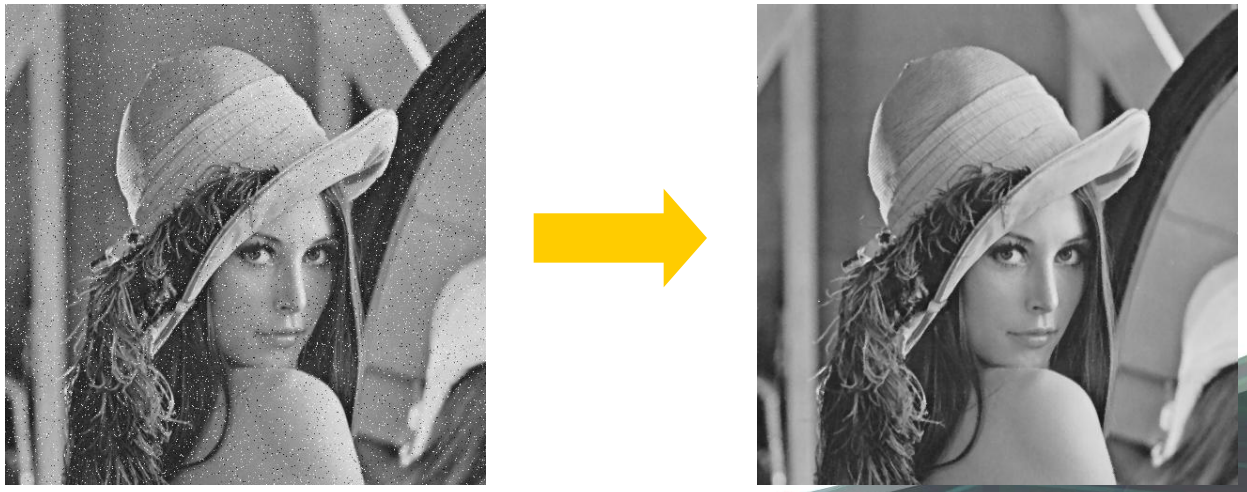
Altera Video and Imaging IP Library Suite

- Library of common video and image processing functions
  - Baseline set of IP with standard interfaces and protocols that allow users and third parties to easily add their own proprietary algorithms
  - Works with any design flow
    - RTL, model-based design, or C-based design
  - Reference design and development kit available
- IP cores optimized for Altera FPGAs
  - 2D digital filters: finite impulse response (FIR), median
  - Color space conversion
  - Image mixing/blending
  - Scalar (vertical/horizontal)
  - Deinterlacer
  - 2D fast Fourier transform (FFT)
  - Video buffer compiler

Altera Ordering Code: IPS-VIDEO

2D FIR Filter and 2D Median Filter

- Support 3x3 pixel, 5x5, and 7x7 kernel sizes
  - Support 9x9, 11x11, 13x13 in future releases
- Support 8-bit,10-bit, and 16-bit pixel input data
- Configurable support for handling image edges
- Optimized for FPGA architecture



Color Space Converter

- Color spaces supported:
  - RGB (computer and studio formats)
  - YIQ/YUV (NTSC, PAL, SECAM)
  - YCbCr (4:4:4, 4:2:2, 4:2:0) with chroma resampling
    - Support pixel replication/decimation
    - Support bilinear interpolation
    - Support bicubic interpolation
  - CMYK (document imaging)
  - Bayer conversion (CCD/CMOS sensor format) demosaic
- Supports gamma correction

Image Blending and Picture-in-Picture Mixing

- Supports 8-bit and 10-bit pixel data
- Supports OpenGL texturing standards, i.e., RGBA2, RGBA4
- Alpha blending on pixel-by-pixel basis
- Multiple color plane mixing (2 to 8 layers)
- Run-time control of picture-in-picture location
- Supports full-screen high-definition (HD) graphics

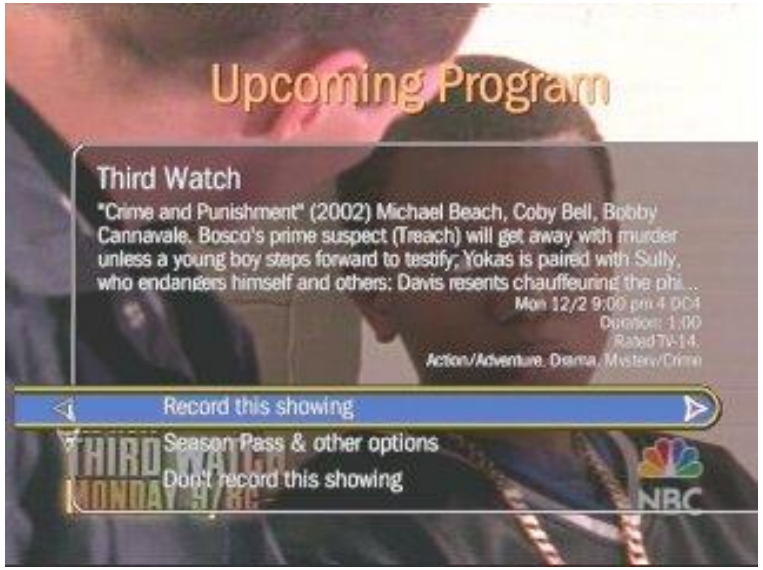


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Image Scaling

D1/SDTV: 720x480

HDTV 1080p: 1920x1080

- Independent scaling for vertical/horizontal with arbitrary scaling ratios
- Choice of filtering techniques
  - Linear (2-tap, 8-phase polyphase filter per dimension implementation)
  - Higher order interpolation (8-tap, 32-phase polyphase filter per dimension)
- Support 8-bit and 10-bit pixel input data and image clipping

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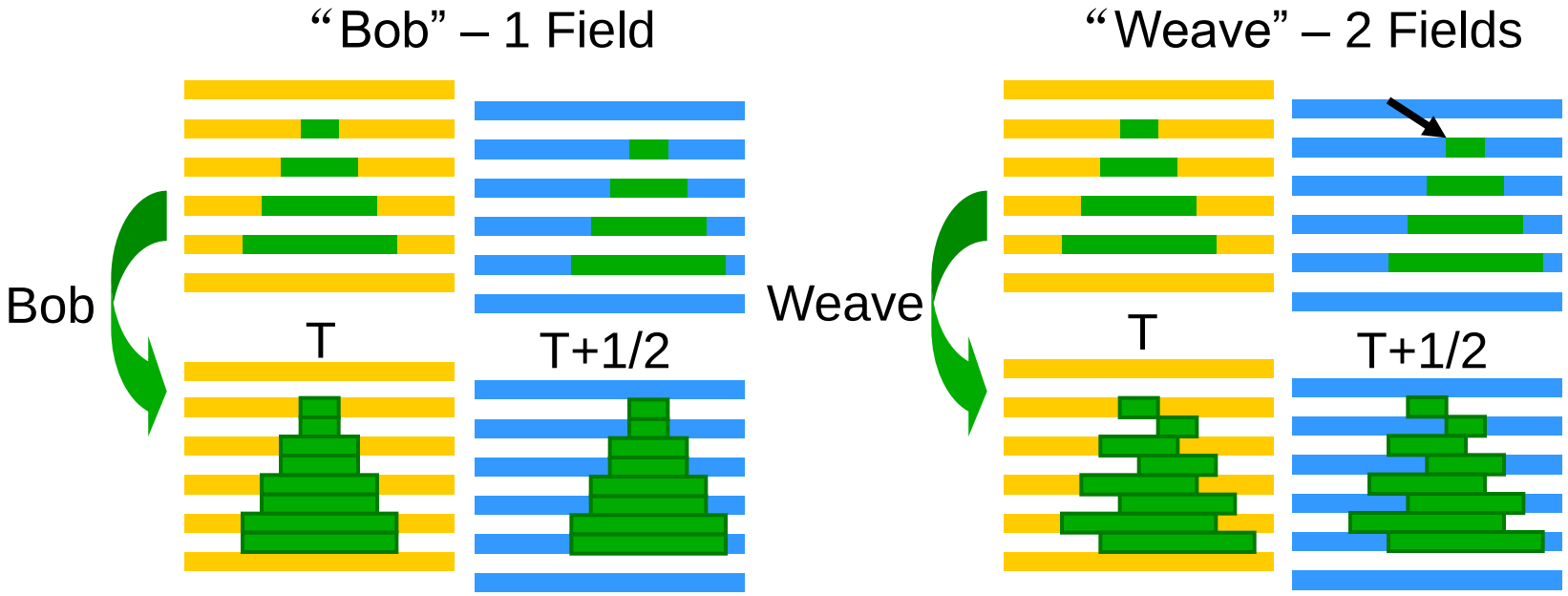
Deinterlacing Options



- **Bob and weave techniques: available in first release**
- **Motion adaptive deinterlacing: available in first release**
  - **"Weave" for still areas of the picture, "bob" for areas of motion**
- **Motion compensated deinterlacing: available in future release**

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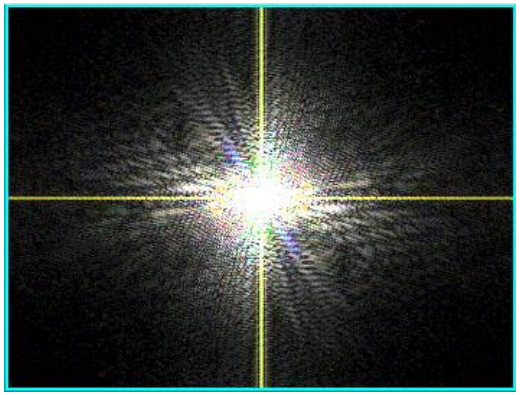
2D Fast Fourier Transform (FFT)



- Supports discrete set of transform sizes
  - 64x64, 256x256, 1024x1024
- Supports both fixed point and floating point
- Supports up to 16-bit pixel input data

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Video Buffer Compiler

- Allows efficient use of FPGA internal memories to store line buffers
- Optimized for typical SD and HD resolutions
- Supports Stratix® II and Cyclone II memory architectures
- Supports 8-bit and 10-bit pixel input data

Altera Memory Controller and Bus Interface Solutions

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PCI/PCI-Express in DVR System

- More than 70% DVR systems based on PCI and PCI Express interface
- Next-generation system will be based on PCI Express
  - Standard configuration for PC
  - PCI bandwidth limitation for multi-channel video
- Altera offers complete solution for PCI and PCI Express interfaces

Altera PCI Express Solutions

- Complete, easy-to-use PCI Express solutions
  - x1, x4 & x8 endpoints
  - Industry-leading design flow with Altera MegaCore® IP
  - Stratix II GX, Cyclone II, Stratix II, HardCopy® II and Stratix GX device support
- Low-risk, hardware-verified solutions
  - PCI-SIG-compliant and device characterization
  - 2 generations of FPGAs with embedded transceivers
    - Stratix GX passed PCI-SIG compliance
    - Stratix II GX targeting PCI-SIG compliance May 2006
  - Development/demonstration boards

Fastest Time-to-Market with a Reliable PCI Express Endpoint Solution

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FPGAs and Options Supported

Feature	x1	x4	x8
Device Family Support	■ Stratix II GX ■ Stratix II ■ Cyclone II ■ Stratix GX	■ Stratix II GX ■ Stratix II ■ Cyclone II ■ Stratix GX	■ Stratix II GX ■ Stratix II
Virtual Channels	1 to 4	1 to 4	1 or 2
Advanced Error Reporting (AER)	✓	✓	✓
End-to-End Cyclical Redundancy Check (ECRC)	✓	✓	✓
Data Path Width	64 bits	64 bits	64 bits
Frequency of Operation (f_{MAX})	62.5 MHz, 125 MHz	125 MHz	250 MHz

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Other IP Cores Available

- Ethernet MAC, I^2C, SATA
- Various memory controllers
  - DDR, DDR2, RLDRAM II

Altera and TI Solution

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Cost Challenge

3 D1 Channels + 3 CIF Channels + Analytics + Video Streaming

	DSP-Only Solution	FPGA+DSP Solution
FPGA	None	2C50
DSP	6 DM6446	DM642 (Analytics)
Memory	3 DDR2 SDRAM	1 DDR2 SDRAM
Total Silicon Cost	$195	$60

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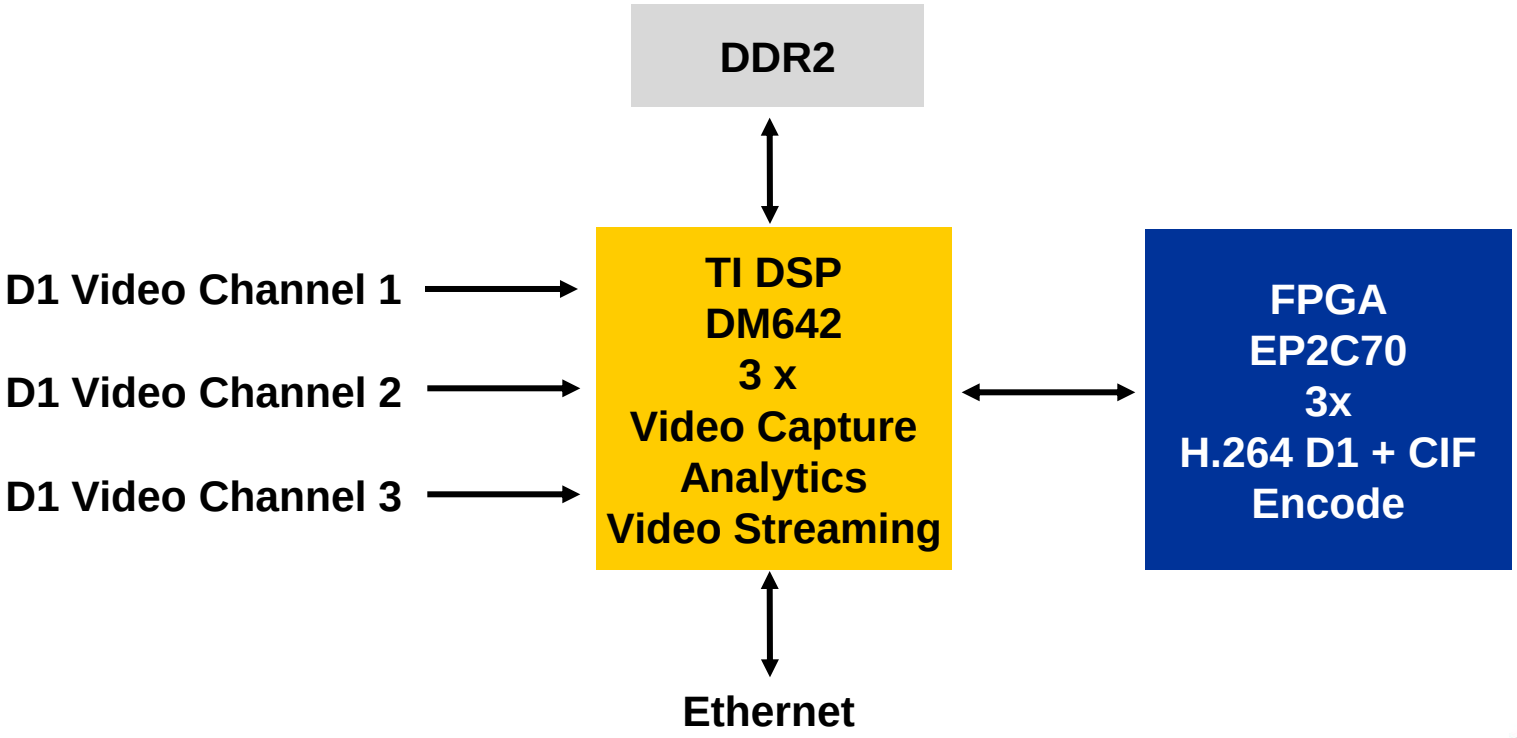
Why Use FPGAs and DSPs

- DSPs yield quick implementation of core processing
- FPGAs add specialized parallel-processing optimizations where serial instruction sets of DSPs fail
- Migrate suitable algorithms from DSP to FPGA coprocessor over time

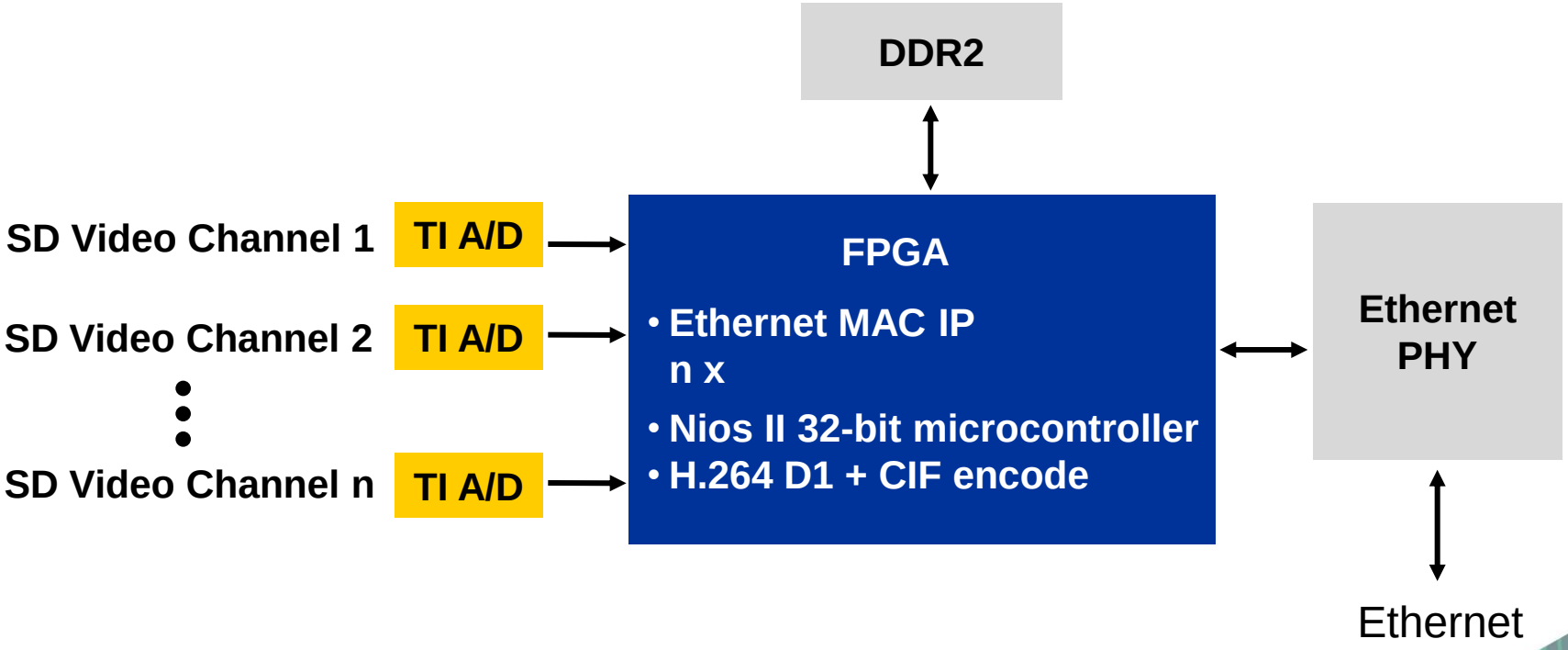
DVR Architecture Proposal #1



Advantages:
Front-end analytics
Streaming capability

Disadvantages:
Cost
2-chip solution

DVR Architecture Proposal #2



Advantages:
Cost
Scalable to *n* channels

Disadvantages:
Limited analytics
Multi-chip solution

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Development Kits

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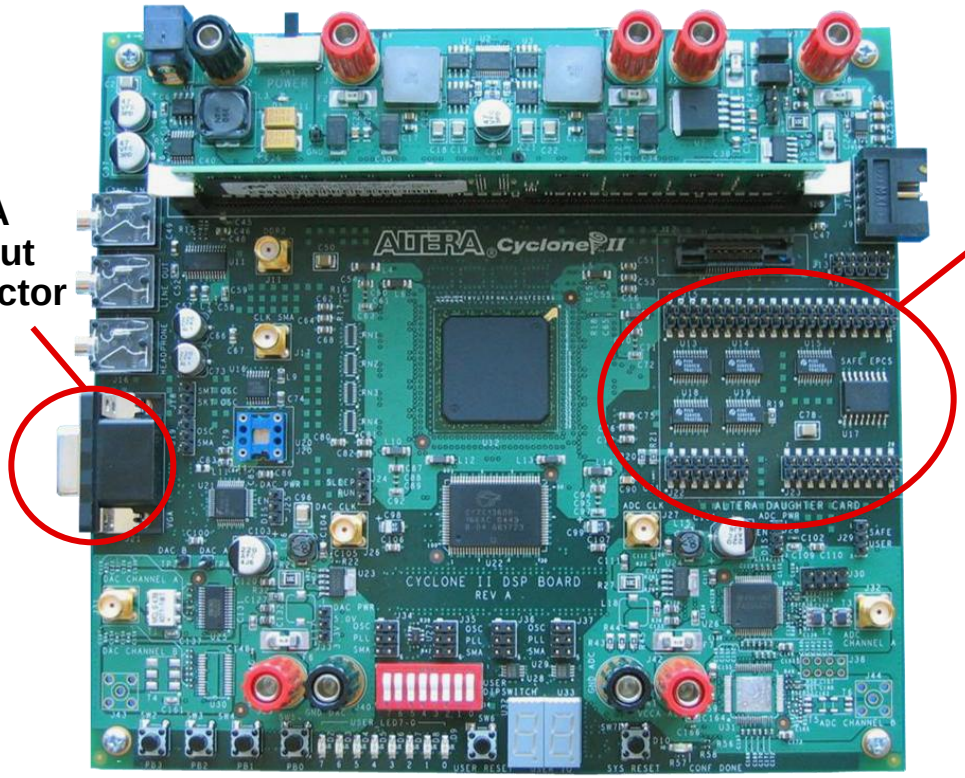
Cyclone II Video Development Kit



- FPGA density
  - EP2C35 to EP2C70
  - EMIF connector to TI DSP kits
- Video capture/input daughter card
  - Dual inputs
    Composite video (NTSC/PAL)
  - *Also compatible with Stratix II DSP Kits*
- Bundled software
  - Quartus® II (FPGA design)
  - DSP Builder (DSP design)
  - Matlab/Simulink evaluation
  - VIP Suite evaluation
    IP cores

Altera eStore On-Line Ordering Code = DK-VIDEO-2C70N (shown above) or DSP-DEVKIT-2C35 + DC-VIDEO-TVP5146N

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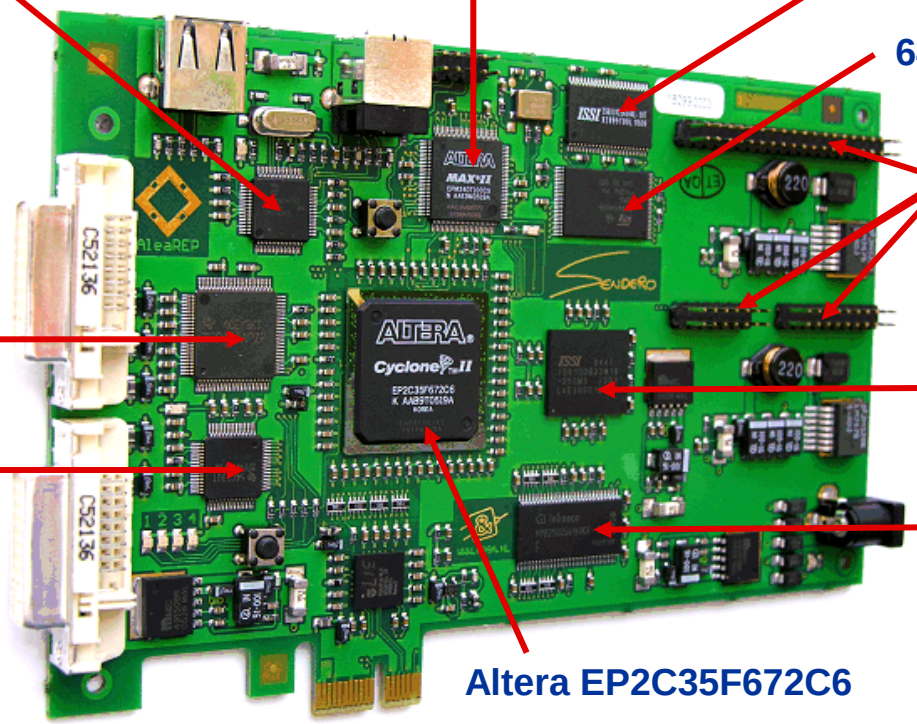
Sendero Board PCI Express



Ordering Information:

http://www.fpga.nl/index.html?sendero.html

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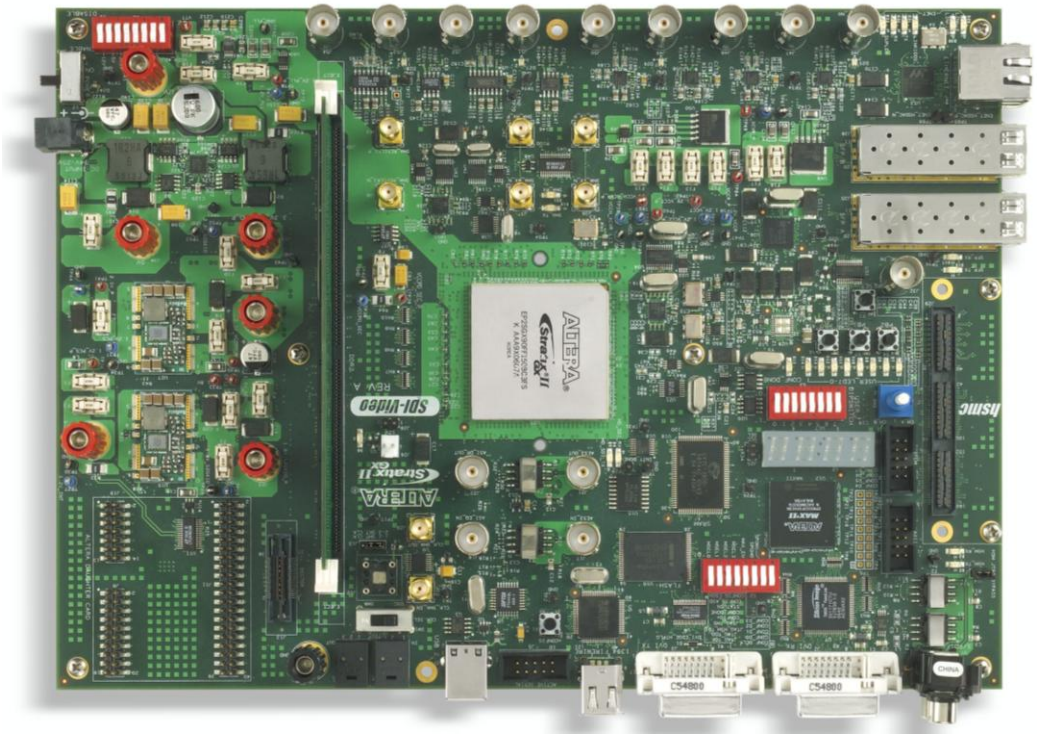
Stratix II GX Audio/Video Development Kit



- FPGA density
  - EP2SGX90
- Video
  - Digital video interface (DVI) inputs/outputs
  - Four SD HD SDI inputs/outputs, including dual-link SDI support
  - Asynchronous Serial Interface (ASI) inputs/outputs
- Audio
  - AES3
  - Sony/Phillips digital interface (S/PDIF)
- Bundled software
  - Quartus II (FPGA design)
  - DSP Builder (DSP design)
  - Matlab/Simulink Evaluation
  - SDI reference design
  - VIP suite evaluation IP cores

Altera eStore On-Line Ordering Code = DK-VIDEO-2SGX90N (shown above)

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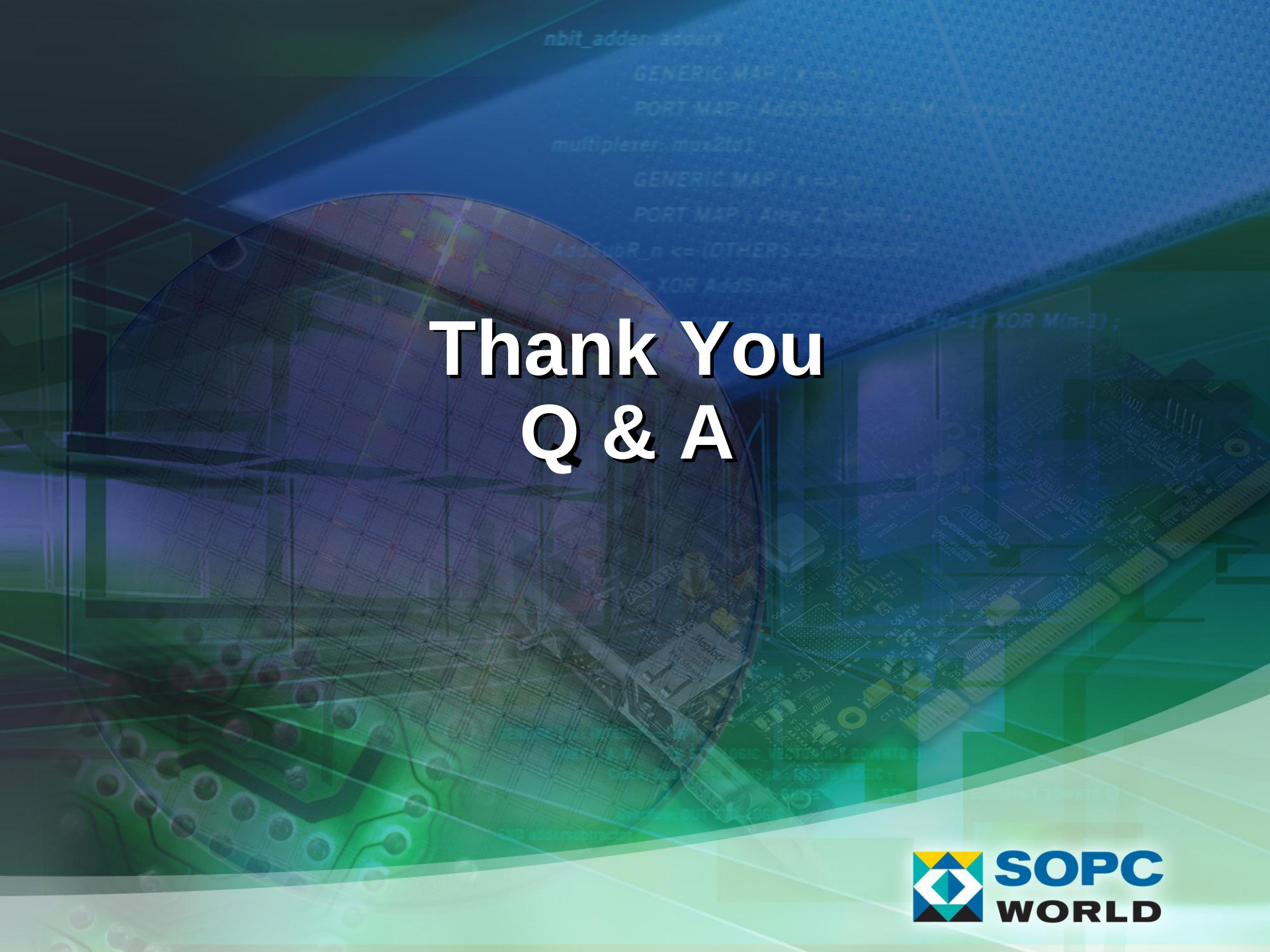
Other Development Kit Options

- Other video daughter cards:
  - ASI/SDI with 2C5 daughter card
  - Audio IO daughter card
- Cyclone III FPGA video development kit
  - In planning phase (contact Altera for schedule)
  - Will cover various applications, from video surveillance to consumer AV


Thank You
Q & A
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