Reduce Your System Power Consumption with Altera FPGAs

Agenda

- Benefits of lower power in systems
- Stratix® III power technology
- Cyclone® III power
- Quartus® II power optimization and estimation tools
- Summary

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Benefits of Lower Power

- Stay within a fixed power budget
  - Chassis limits (heat, space, current)
  - Battery life considerations
  - Outside power budget → not an option
- Reduce system cost
  - Fewer/smaller heat sinks and fans
  - Smaller power supplies
- Increase reliability
  - No fans → no moving parts
  - Lower system temperature
- Reduce design time and effort to meet power and thermal constraints
- Reduce ongoing operating costs

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Altera Power Strategy at 65 nm and Beyond

- Innovative architecture and advanced process technologies
- Best-in-class FPGA power modeling
- Lowest power solution in the industry

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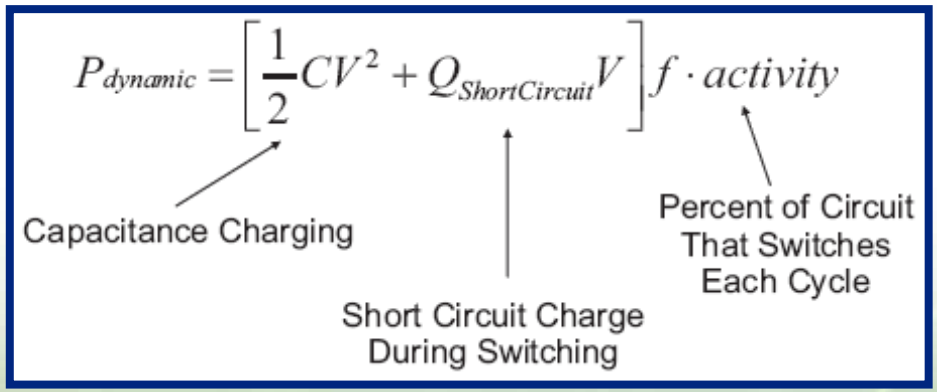
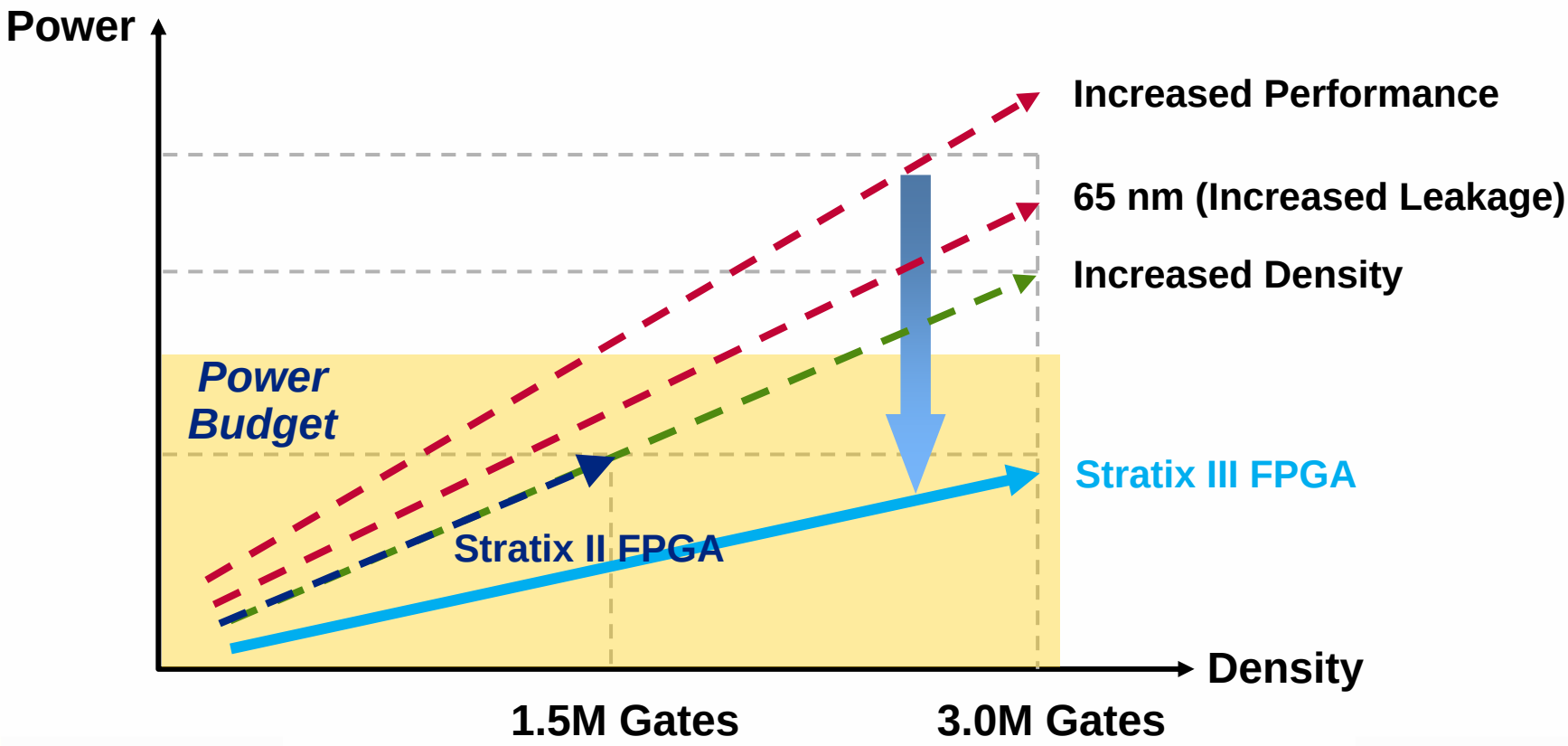
Power Components and Terminology

- Core static power
  - Power consumed even when there are no clocks active; power due to leakage currents
  - Static power is function of device selected and junction temperature
- Dynamic power
  - I/O power
    - Charging and discharging external load capacitance connected to device pins, I/O drivers, and external termination network (if present)
  - Block power
    - Power for individual device resources such as the logic elements (LEs), phase-locked loops (PLLs), or memory blocks
- Total power = core static power + dynamic power (I/O + block)



Stratix III Power Technology

Meeting the Power Challenge



Stratix III FPGAs Cut Power by 50% vs. 90 nm

Lowest Power FPGA in the Industry

Stratix III FPGA Power Reduction Technique	Lower Static Power	Lower Dynamic Power
Silicon Process Optimizations	✓	✓
Selectable Core Voltage (0.9 V or 1.1 V)	✓	✓
Programmable Power Technology	✓	✓
Power Optimized DDR Memory Interface	✓	✓
Quartus II Software PowerPlay Power Analysis and Optimization	✓	✓

Leading Edge Process Technology
Increased Performance, Reduced Power

- Advanced 65-nm process
  - 15% capacitance reduction → reduces dynamic power 15%
  - Lower voltage → reduces dynamic power another 16%
- Multiple-gate oxide thicknesses (triple oxide)
  - Trade-off static power vs. speed per transistor
- Multiple-threshold voltages
  - Trade-off static power vs. speed per transistor
- Low-k inter-metal dielectric
  - Reduces dynamic power, increases performance
- Strained silicon
  - Increased performance
- Copper interconnect
  - Increased performance, reduced IR drop

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Selectable Core Voltage

Selectable Core Voltage

- Customer selects the FPGA core voltage
  - 1.1 V for maximum performance
  - 0.9 V for minimum power
- I/O and PLL voltages unaffected
  - Still get maximum I/O interface speed
  - Crucial, since I/O bandwidth limits many systems

Nominal Voltage	Min. Regulator V_{OUT}	Max. Regulator V_{OUT}	Slow Timing Model	Fast Timing Model	Power Model
1.1 V	1.05 V	1.15 V	✓	✓	✓
0.9 V	0.86 V	0.94 V	✓	✓	✓

Power and Timing Impact

Core Voltage	Dynamic Power Reduction From Stratix II FPGAs	Static Power Reduction From Stratix II FPGAs	Performance Gain Over Stratix II FPGAs
1.1 V (1)	33%	52%	35%
0.9 V (2)	55%	64%	8%

Notes:
(1) Fastest vs. fastest speed grade comparison
(2) Slowest vs. slowest speed grade comparison

More Choice to Meet Your Power and Performance Budgets

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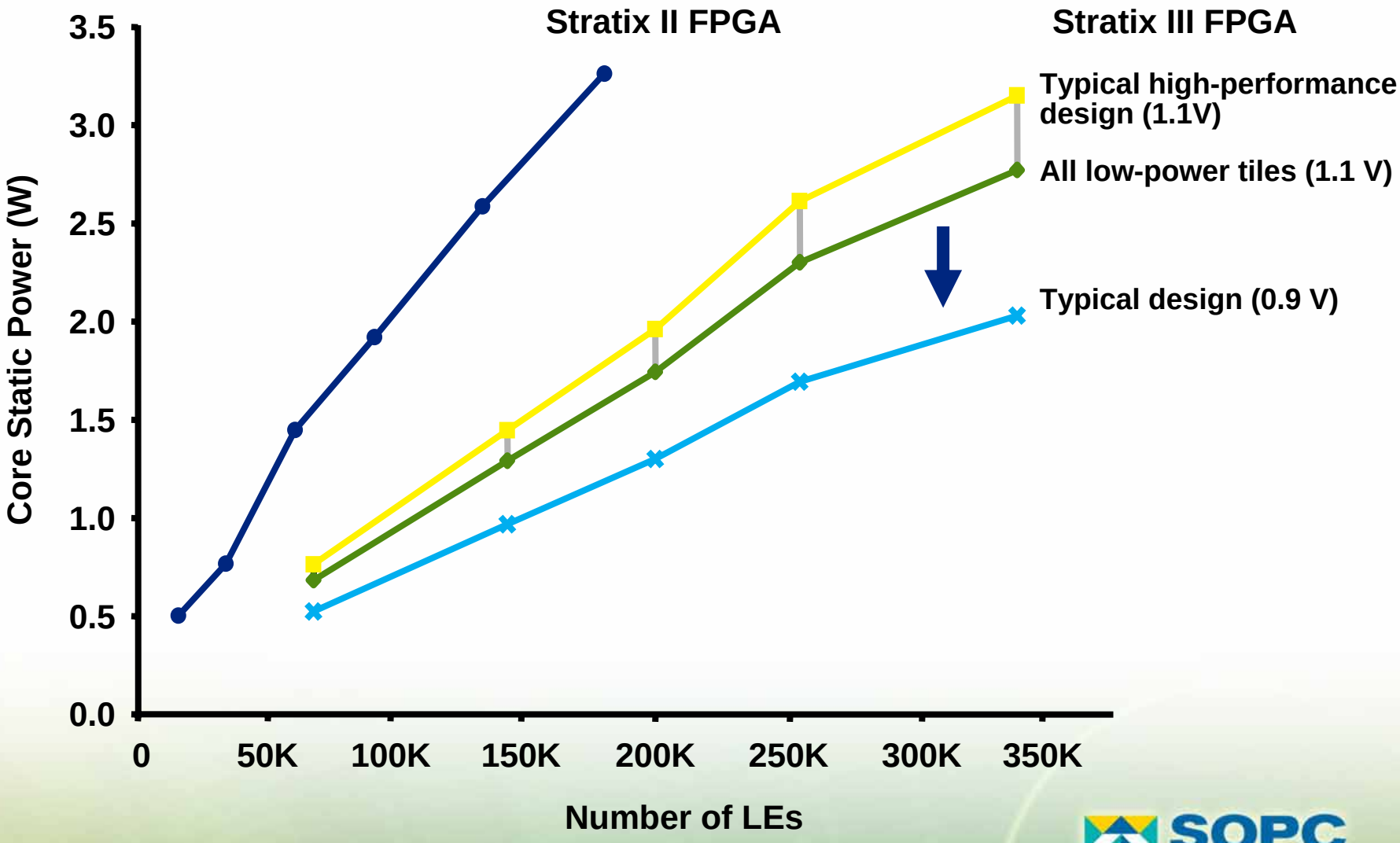
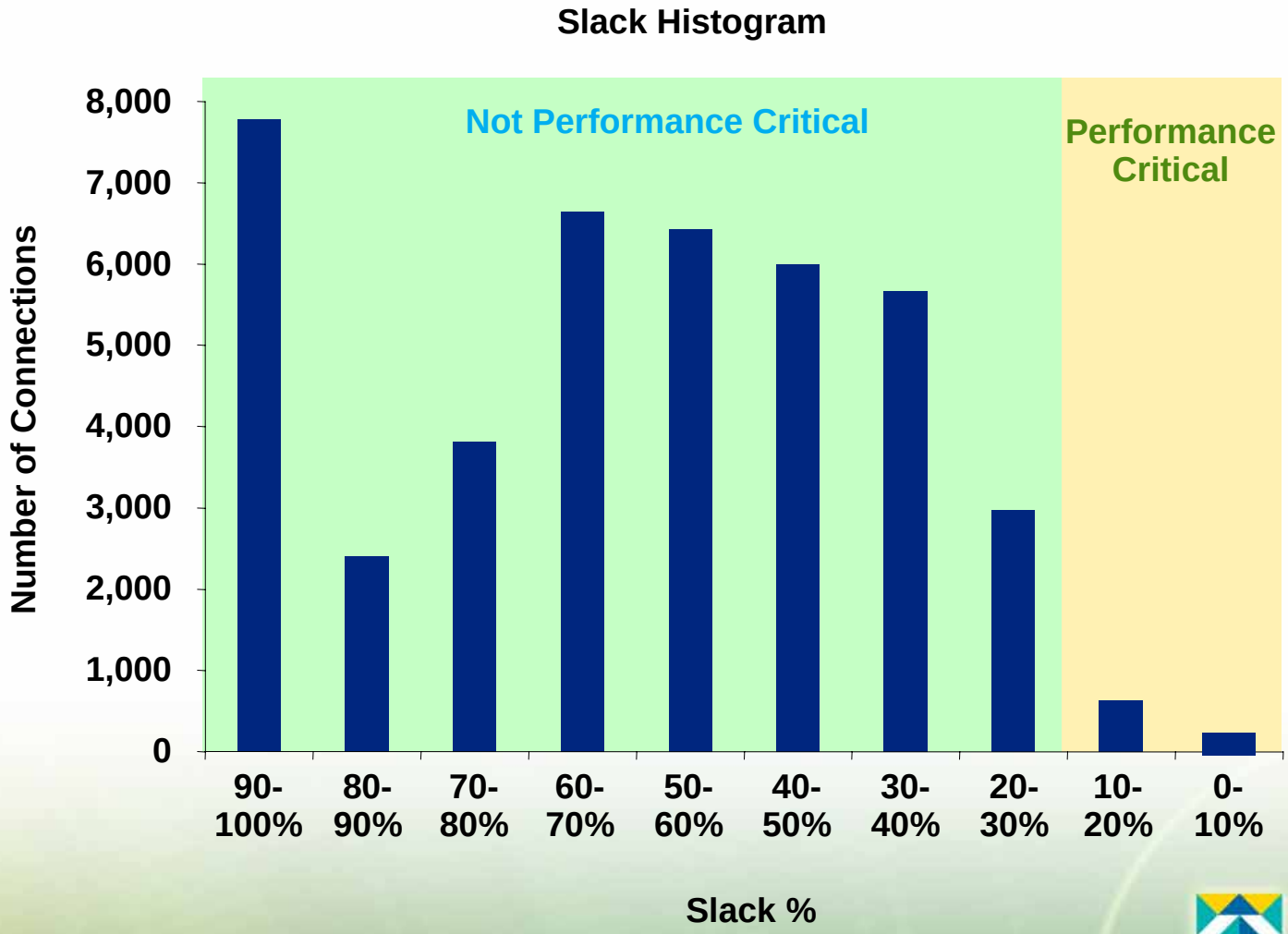
60% Lower Static Power (85˚C)



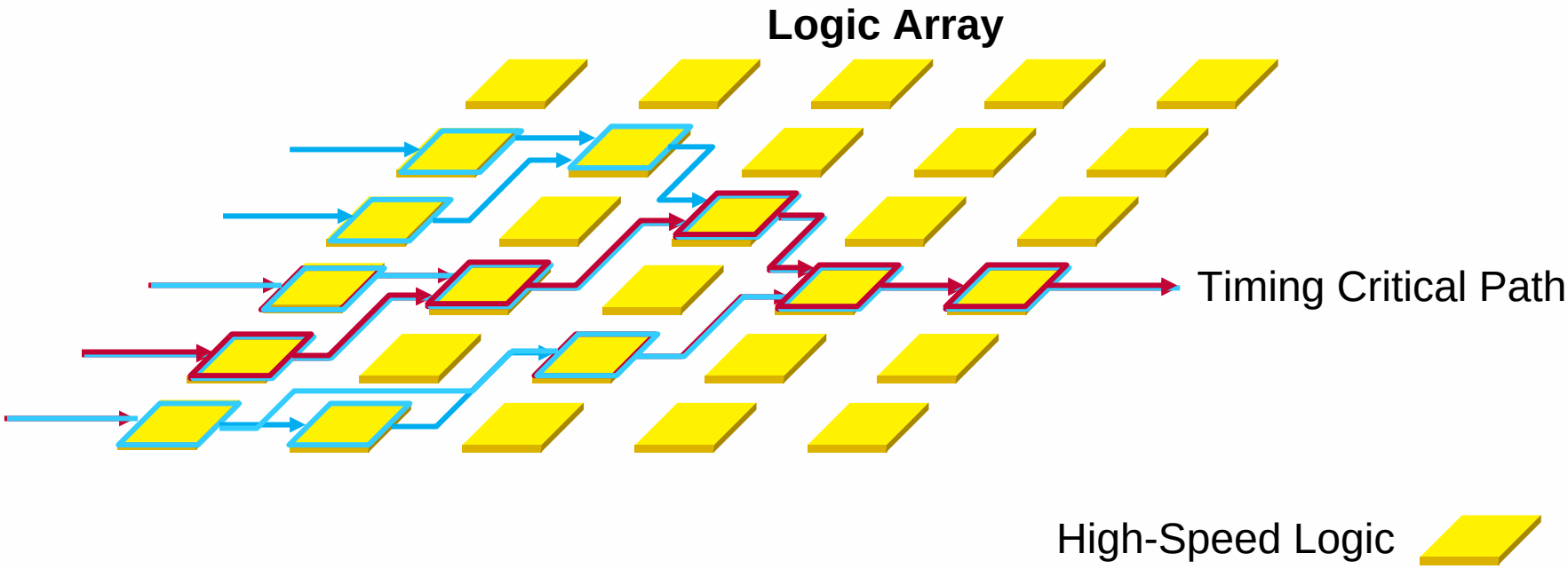
Programmable Power Technology

Design-Specific Power Optimization

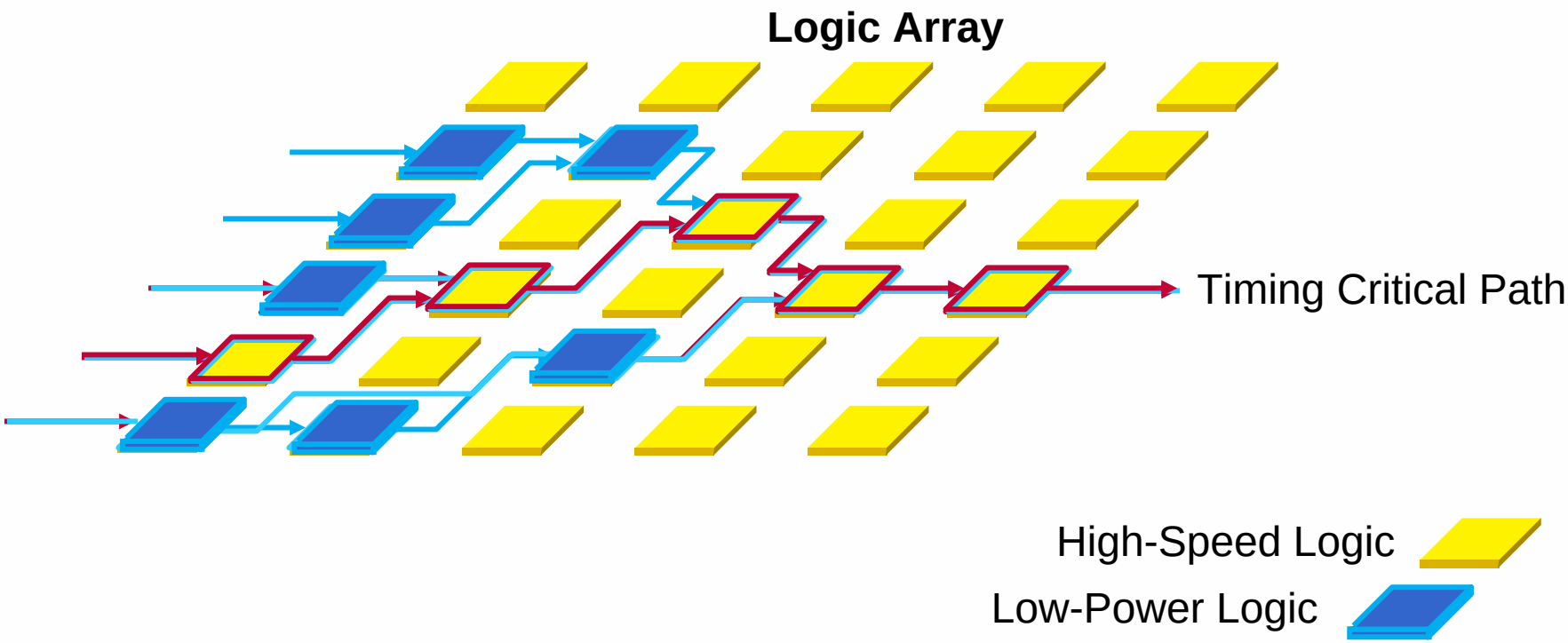
- Only a small fraction of logic is performance critical



Programmable Power Technology



Programmable Power Technology



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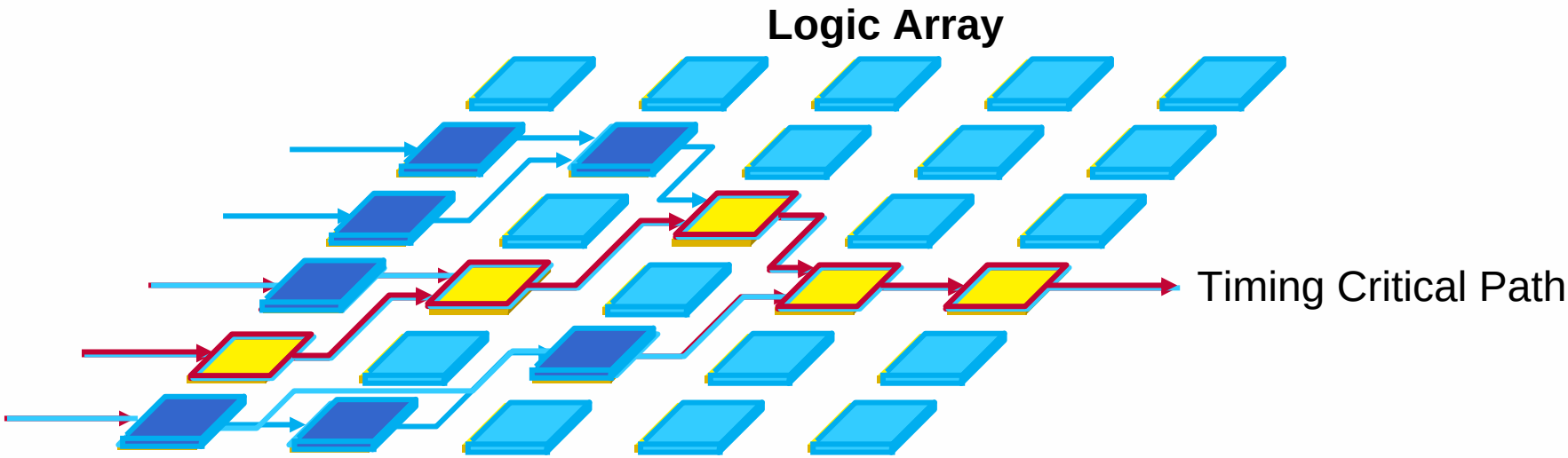
Programmable Power Technology



*** Power mapping fully automated by Quartus II software based on timing constraints**

High-Speed Logic

Low-Power Logic

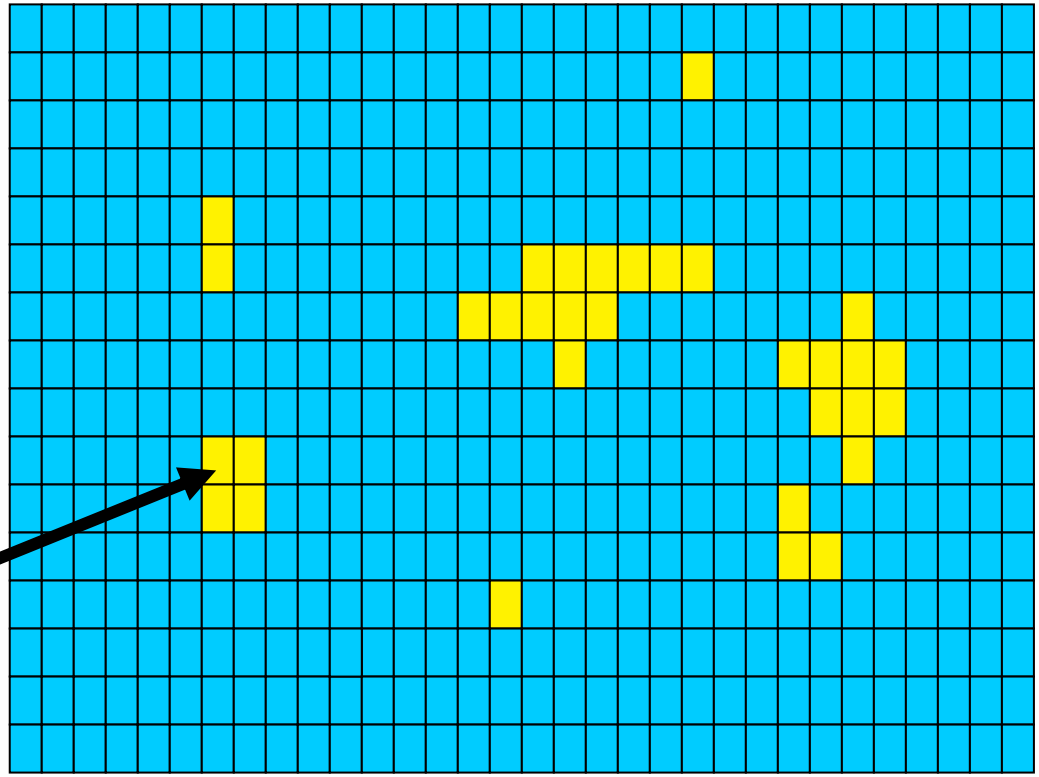
Unused Low-Power Logic

High Performance Where You Need It, Lowest Power Everywhere Else

High-Resolution Power Control

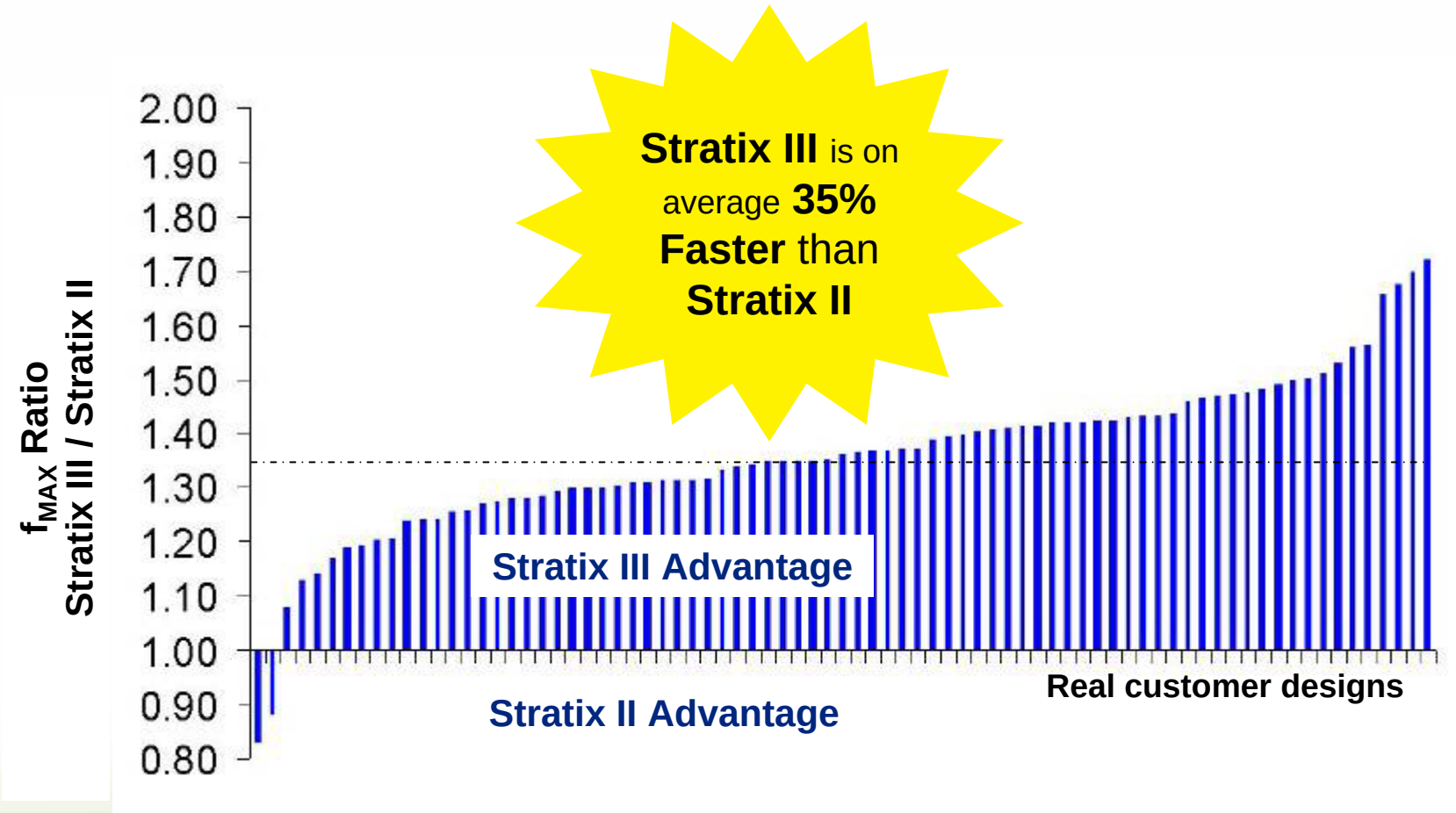
Stratix III FPGA (EP3SL340) has **8,050 tiles** for very high-resolution power/performance optimization

Only a small percentage of high-speed tiles required to maintain design performance



Speed of the Fastest LABs, Power of the Slowest

Stratix III: Highest Performance



Note: Benchmarking data is based on comparing an Altera device to an equivalent Xilinx device using Quartus II V7.2 and ISE 9.2iSP1 software

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Quartus 7.2 will be available in October of 2007

Using Programmable Power

- Circuit board requirements: none!
  - Stratix III FPGAs create low-power tiles using on-chip circuitry
  - No extra power supplies, no extra board components
- Design changes: none!
  - Quartus II software automatically uses high-speed tiles where needed for timing
  - All unused tiles set to low power
  - All tiles with timing margin set to low power
  - Failed timing constraints: all tiles not on critical paths set to low power

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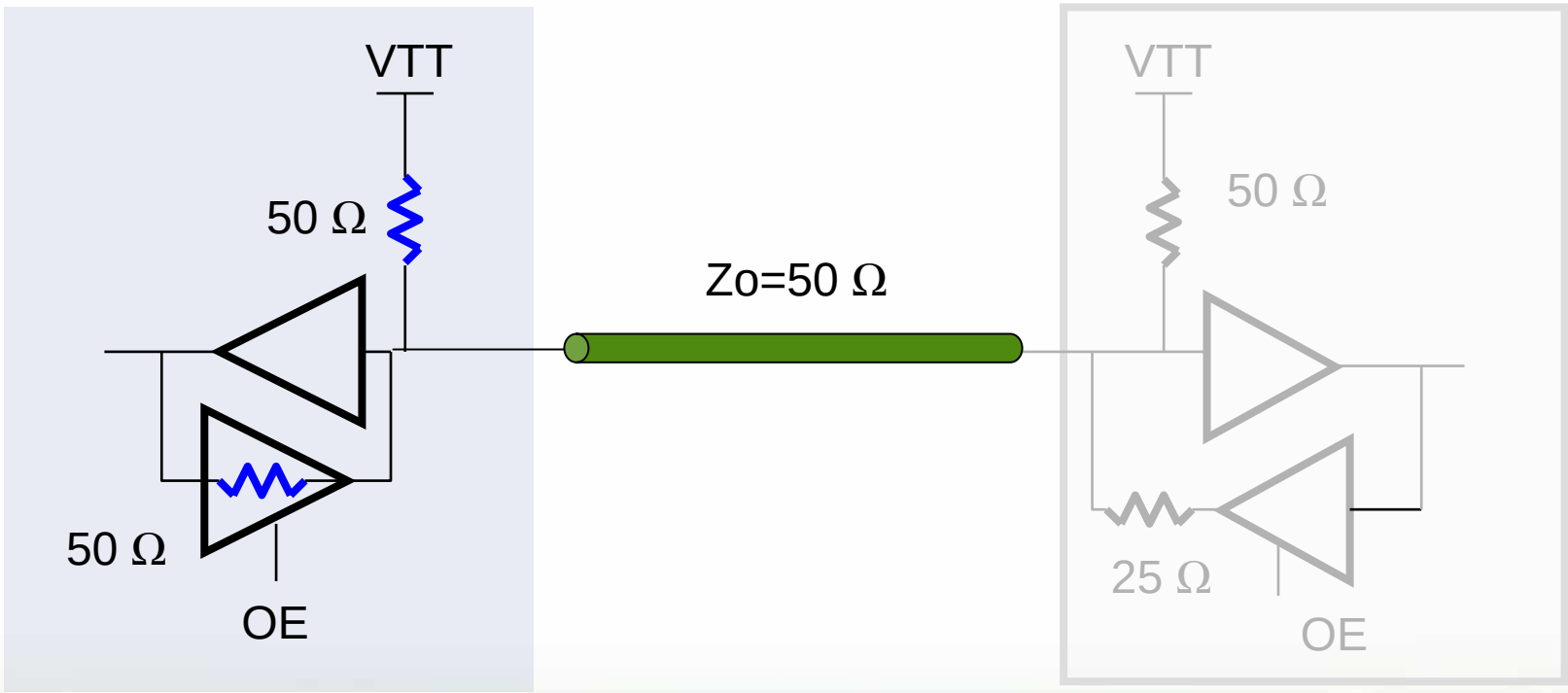
Power-Optimized DDR Memory Interface

Stratix III On-Chip Termination (OCT)

- Both parallel (Rt=50Ω) and series (Rs=50Ω) termination



(*) DDR 1/2/3, RLDRAMII, QDR II/II+ support

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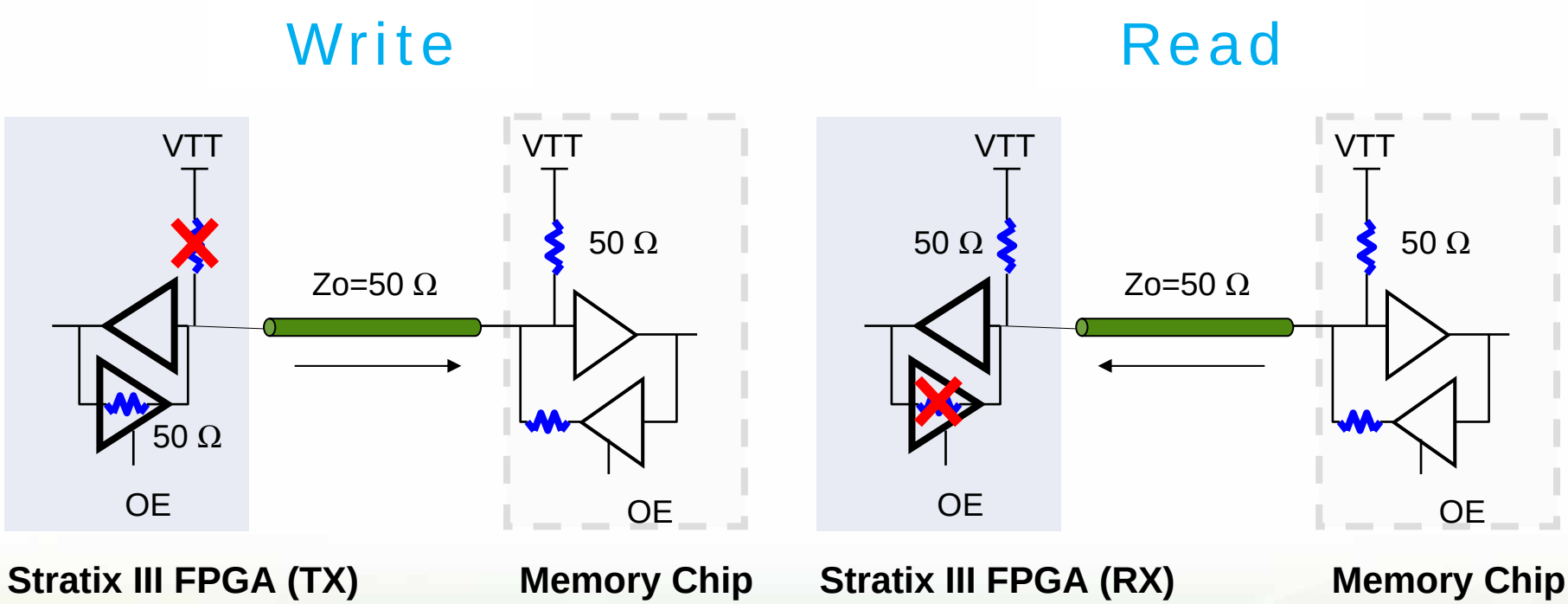
Stratix III FPGA Dynamic OCT

- Write: Rs on, Rt off → Matching line impedance
- Read: Rs off, Rt on → Terminating far end



Saves 1.6 W of DC Power on 72-Bit DDR2 Bus

Benefits of Dynamic OCT

1. Power significantly reduced vs. traditional parallel OCT
   - Saves **1.6 W** of DC power on 72-bit DDR2 bus
2. Proper line termination and impedance matching on bidirectional busses
   - Enhanced signal integrity
3. No need for on-board termination resistors

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Stratix III FPGAs Support DDR3

- Stratix III FPGA: the only FPGA that supports DDR3
- DDR3 consumes **30% lower power** than DDR2
  - DDR2: 1.8 V
  - DDR3: 1.5 V
- Example system:
  - 72-pin, 200-MHz memory interface, with on-chip termination
    - Conventional FPGA DDR2 power: 3.9 W
    - Stratix III (dynamic OCT) DDR2 power: 2.3W
    - Stratix III (dynamic OCT) DDR3 power: 1.6W
  - **Total savings of 2.3 W**

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Cyclone III Power Advantages

Cyclone III Silicon Design Strategy

- Maintain performance while reducing power
- Utilize latest process technology and features available for low-power design

Process or Technology	Benefit
Multi-threshold transistors	**Balance need for performance and low power consumption**
Variable gate-length transistors	**Balance need for performance and low power consumption**
TSMC 65-nm low-power (LP) process	**Reduced FPGA power consumption using the same low-power process technology employed for mobile phone chip sets**

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Cyclone III Power Consumption Advantage

Power Component	Cyclone III Devices Power Reduction Over Cyclone II Devices (1)
Typical Static Power	Up to 54%
Core Dynamic Power	Up to 24%
I/O Power	Comparable

Notes:

(1) Based on Cyclone III EPE v7.0 beta and Cyclone II EPE v.6.1

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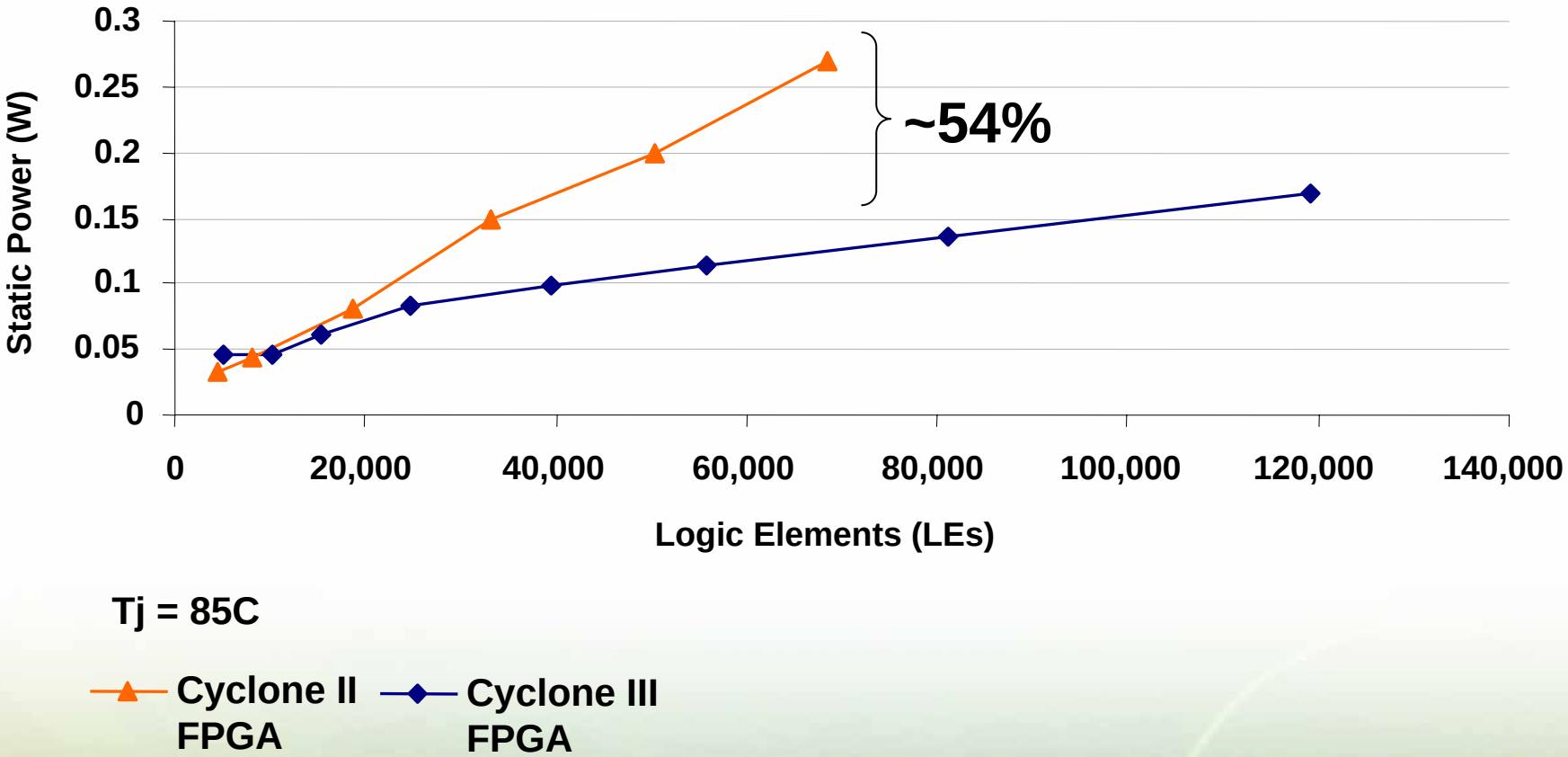
Core Static Power Comparison (85C Tj)

- Cyclone III FPGA benefits grow as Tj and density increase



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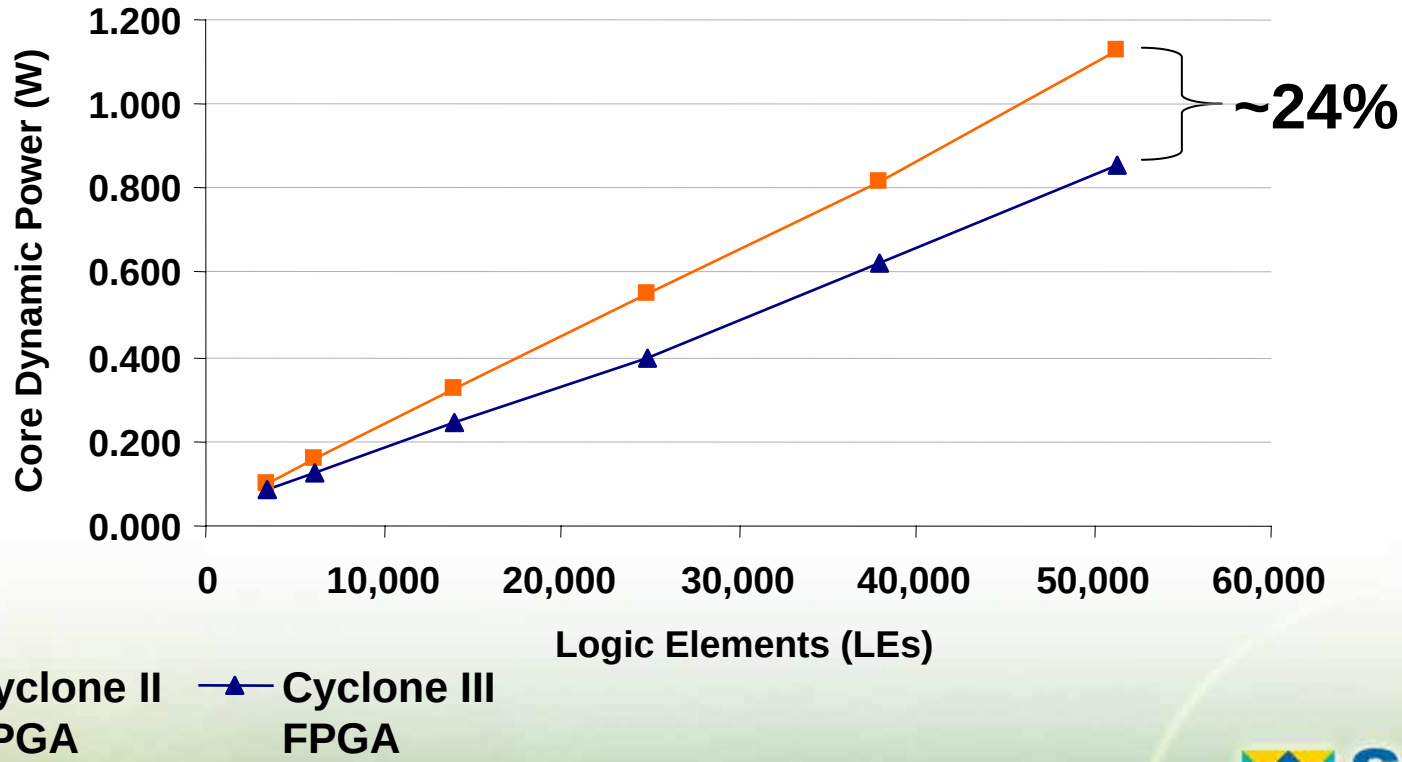
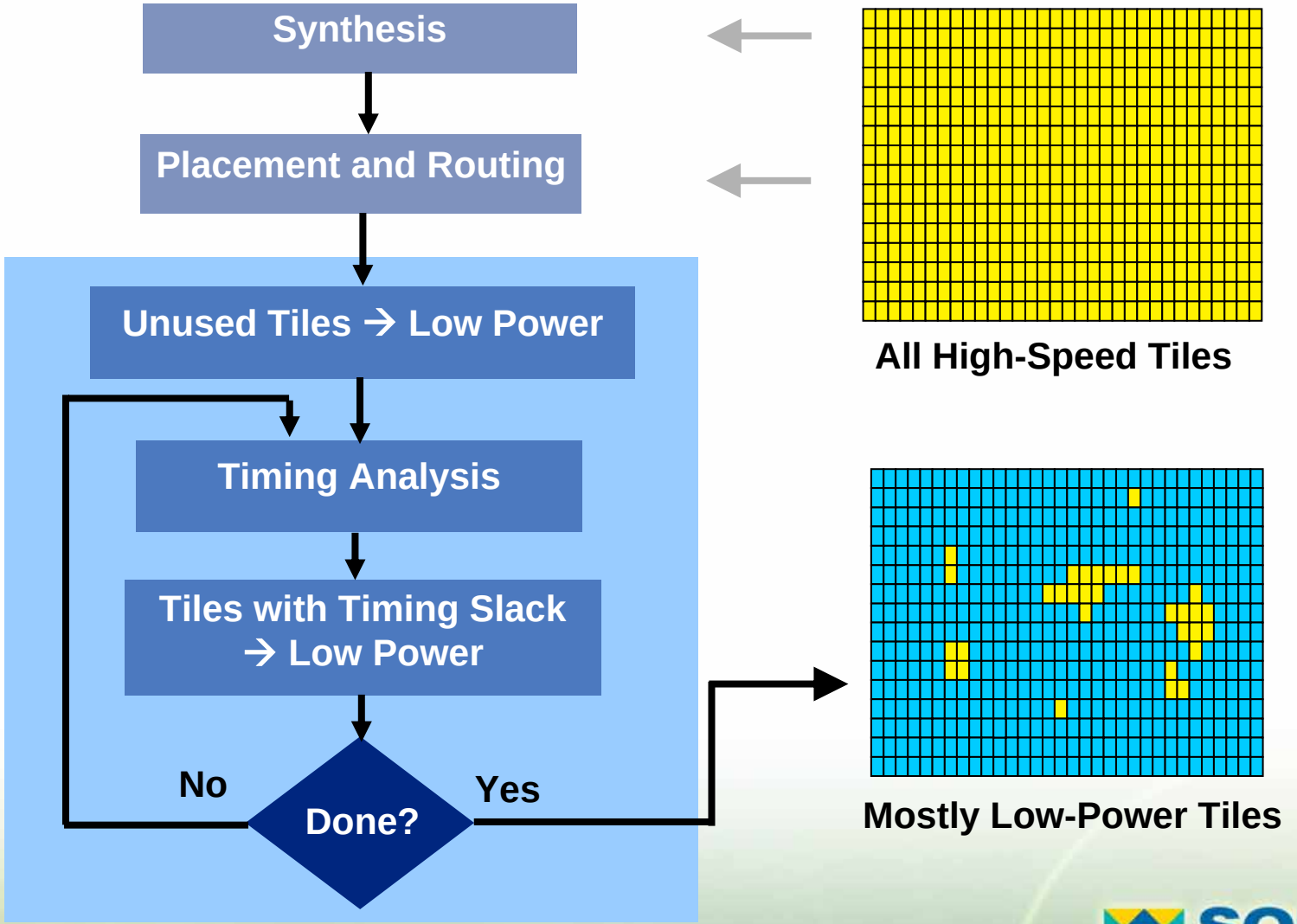
Core Dynamic Power

- Does not vary with temperature
- Function of frequency, number of circuits switching, and capacitance
- All of the Cyclone III device blocks consume less dynamic power than Cyclone II device blocks except for the PLL blocks

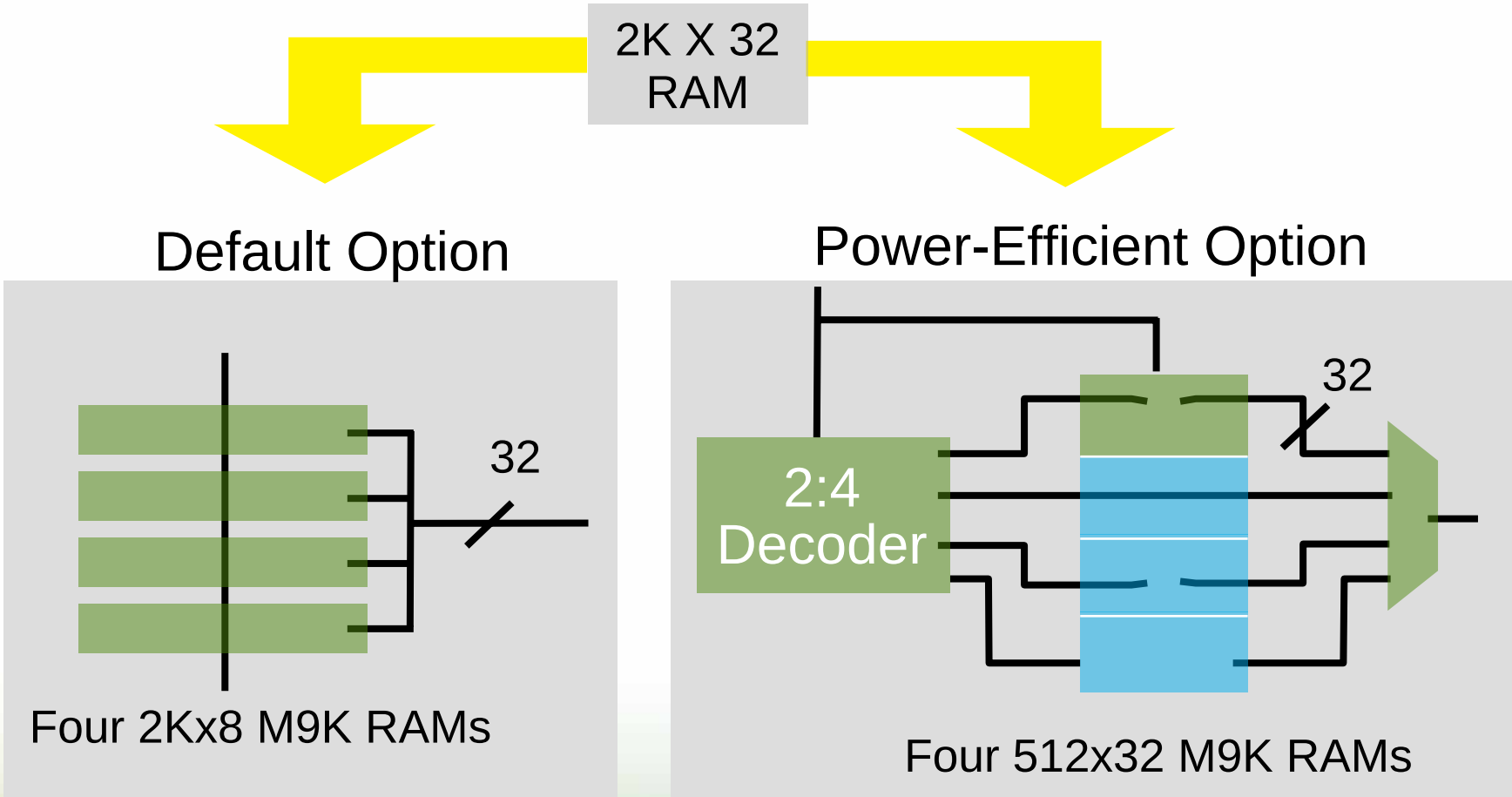


Quartus II Power Optimization and Estimation Tools

Automatic Programmable Power

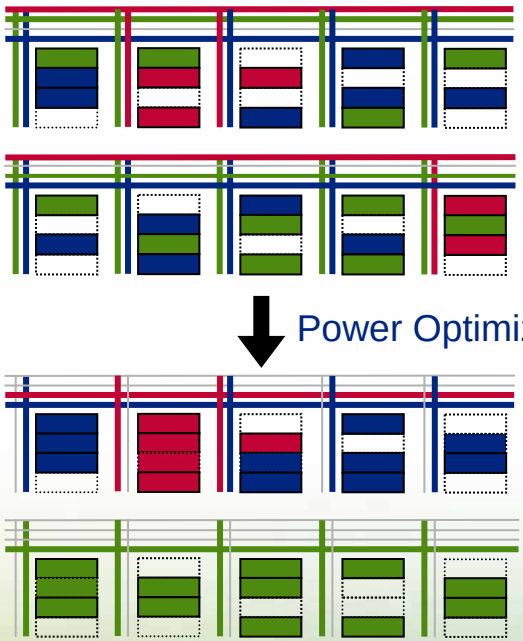


Example: Power-Optimized RAM Mapping

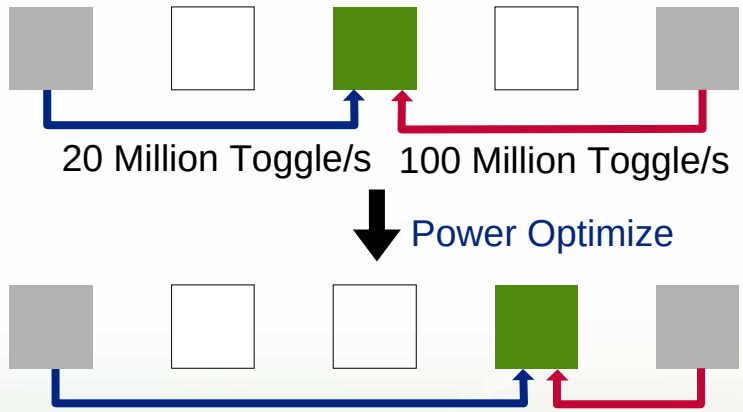


Logic and Clock Power Optimization

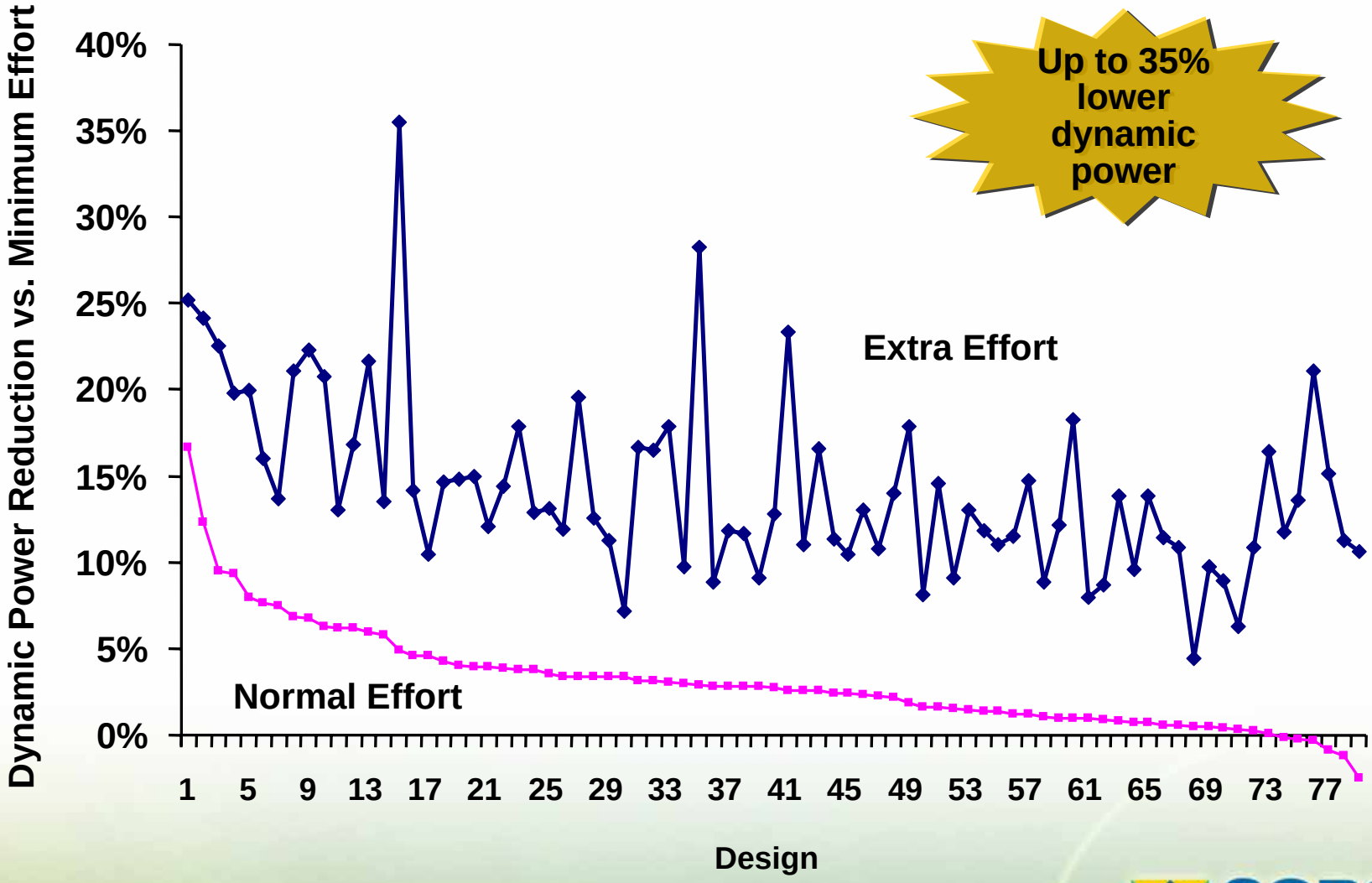
- Clock power reduction
  - Stratix III hardware can shut down clock at 3 levels of tree
  - Automatic placement to reduce clock power



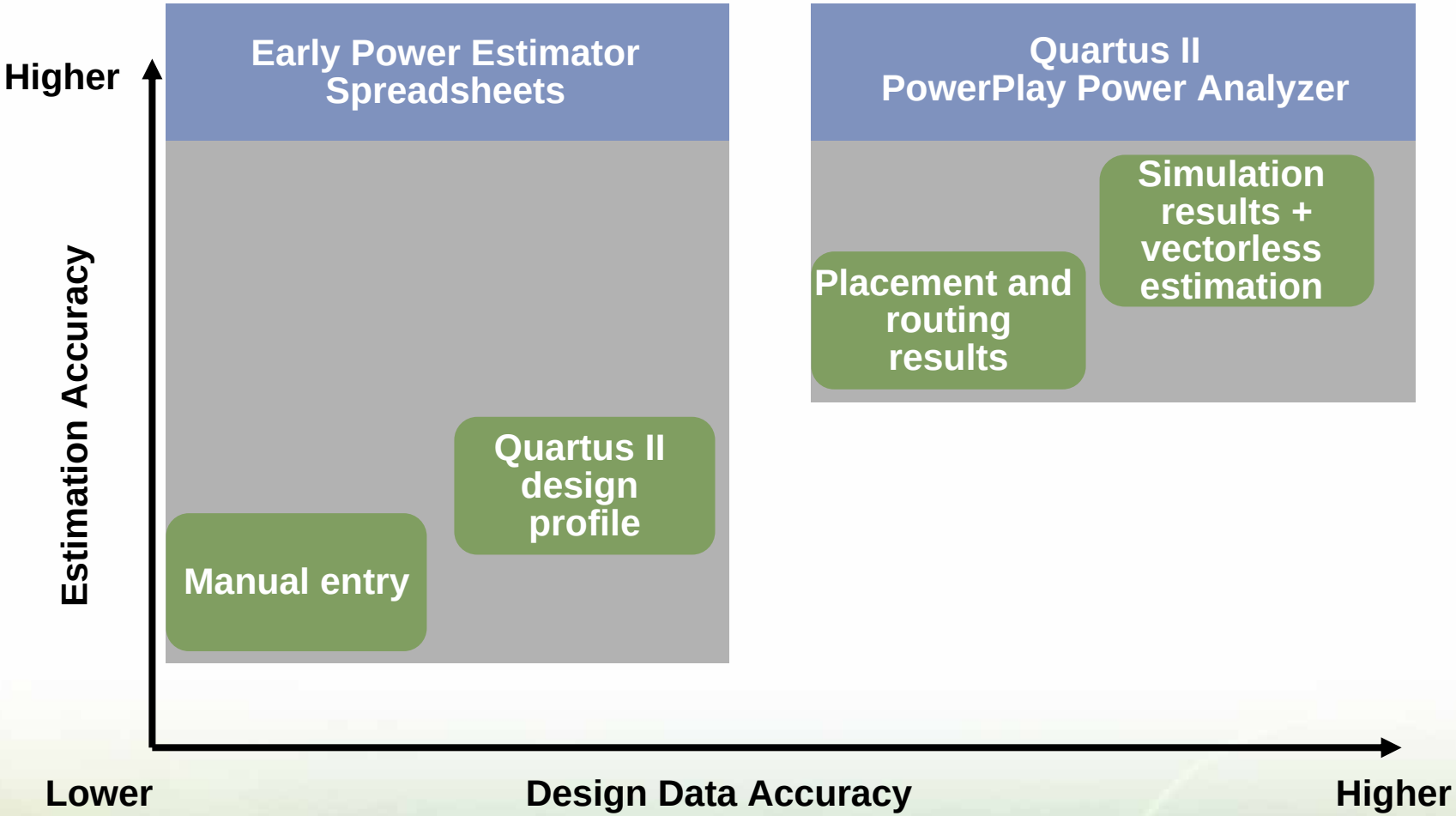
- Power-driven placement and routing
  - Minimize capacitance of high-toggling signals
  - Without violating timing constraints



Dynamic Power Optimization



Design Data Accuracy vs. Estimation Accuracy



Early Power Estimator Spreadsheets

- Enter in design data manually if design files are not available
- Quartus II software automatically generates design data inputs
- Supports quick “what-if” analysis
- Download from Altera® website

Input
Number of Registers
Transition Rates
Clocks and Frequency
I/O and Memory
DSP and PLLs
Temp, Air Flow, Heat Sinking

→

Early Power Estimator

→

Reports
By Resource
By Supply
Thermal Analysis

Estimate Power Before Design Files Available

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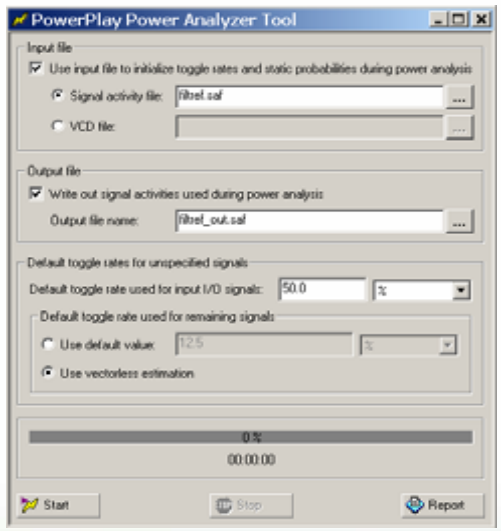
Quartus II Power Analyzer

- Provides highest estimation accuracy by taking advantage of Quartus II software design data and simulation stimuli
- Vectorless estimation technology improves accuracy by plugging in holes not covered by test bench stimuli

Input
Number of Registers
Transition Rates
Clocks and Frequency
I/O and Memory
DSP and PLLs
Temp, Airflow, Heat Sinking
Simulation Results
Place-and-Route Results
Node Activity

Power Analyzer



Reports
By Resource
By Supply
Thermal Analysis
Design Hierarchy Power
Confidence Metrics
Signal Activity Data

Available in All Versions of Quartus II Software

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How Good Are Estimation Results?

- Altera's rigorous modeling methodology
  - Use detailed circuit HSPICE models
    - Logic element, routing, I/Os, clocks
    - Around 9000 simulation elements
  - All models tested and calibrated against FPGA
  - Customer designs tested as final check of quality
- Quality of user inputs and assumptions affects estimation accuracy
  - Are the toggle rate assumptions accurate?
  - Are the simulations reflective of real-world stimuli?
  - How far off is LE count from the final design?

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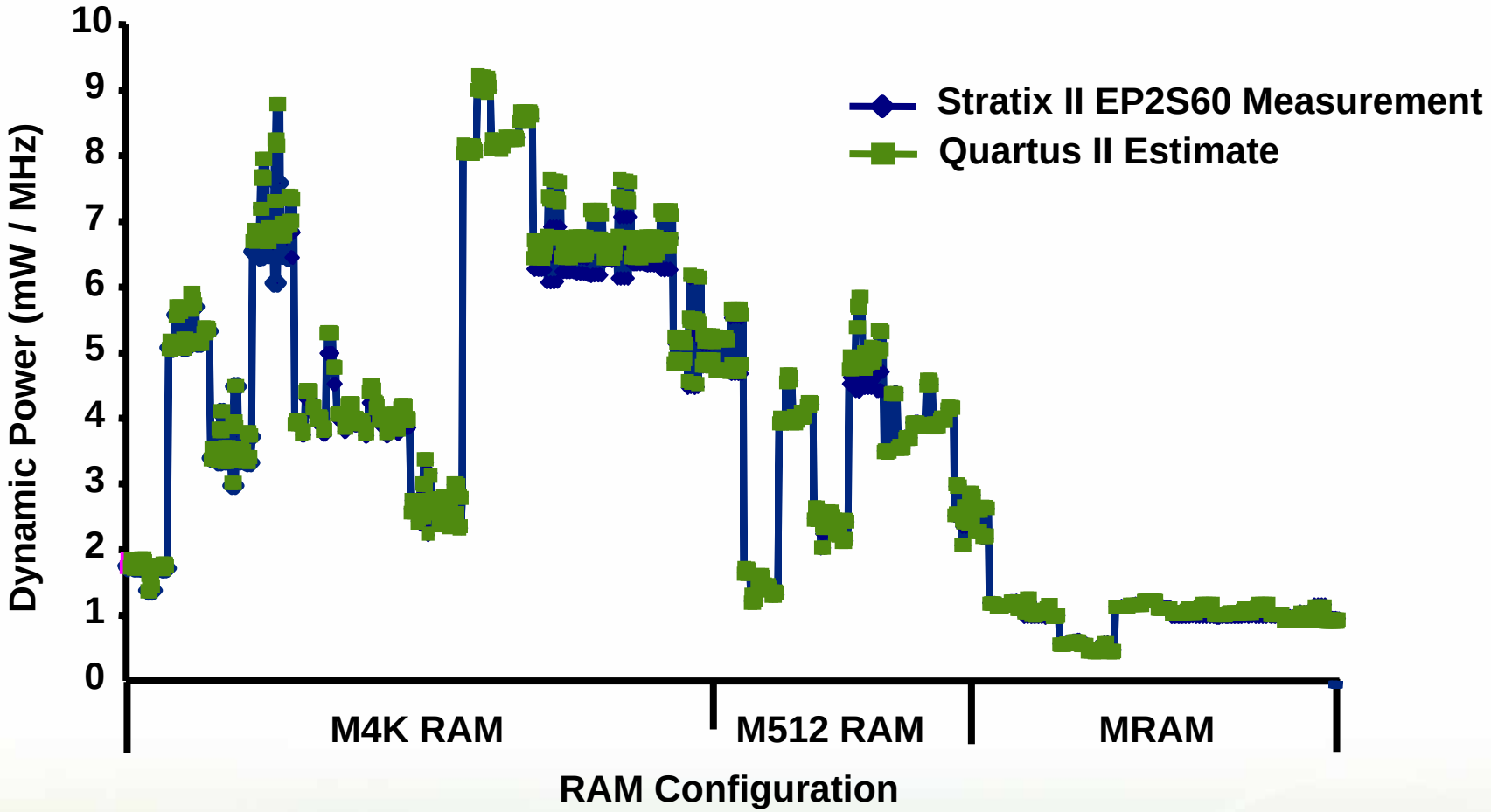
Model Correlation Example: RAM



8700+ Designs Covering All FPGA Elements

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Altera 65-nm Power Advantage

- Innovative architecture and advanced process technologies
  - Programmable Power Technology and selectable core voltage
  - Stratix III FPGA consumes less than half the total power of Stratix II FPGA
  - Cyclone III FPGA consumes less than half the static power of Cyclone II FPGA
- Best-in-class FPGA power modeling
  - Allows power optimization
  - Accurate power estimator
- Lowest power solution in the industry
  - Stratix III FPGA consumes 45% lower power than Virtex-5
  - Cyclone III FPGA consumes up to 80% lower power than Spartan-3

Thank You!