Display and DVR Application

Agenda

- Digital video recorder (DVR) market and display technical overview
- Key system diagrams
- Altera® solutions for DVR and display application
  - Reference designs and intellectual property (IP) cores
  - Tools and development kits
  - Devices
- Live demo
- Conclusion

Video Processing Trends

- Higher image capture and display resolutions
  - Increased consumer demand for digital content
  - Government conversion requirements
- Evolving compression techniques
  - M-JPEG → MPEG4 → H.264
- Needs for advanced system intelligence

Today's Displays

CRT

Rear / Front Projection:

CRT
LCD
DLP
LCOS

Thick

Thin

LCD

PDP
LCD

DLP
F-LCOS

< 40”

> 40”

Trends in LCD TVs

- Larger (>50”)
- Higher resolution (1920 x 1080)
- >1 billion colors

W-XGA+ 16:9
28”- 65”

W-XGA 15:9
17”- 32”

VGA 4:3
15”- 20”

- Flexibility for future features
- Competes with plasma and projection
- Goal: home theatre experience

Changing System Requirements...

A/D or PHY → DSP Device → D/A or PHY

Resolution increase

1280p x 720p

800p X 600p

Processing requirements increase

1. Over 2X more pixels need to be processed for each frame at 30 frames per second
2. Changes in encoding/decoding formats

Standard definition (SD) to high definition (HD) format

...Impacts to System Design

A/D or PHY

DSP Device

DSP Device

DSP Device

D/A or PHY

Resolution increase

1280p x 720p

800p X 600p

SD to HD format

Key System Diagrams

Display System Diagram

Composite
DVD
Digital SD/HD
Memory stick
Digital video interface
…

Video Board

Scaler

Resolution control,
contrast enhancement,
edge enhancement,
color enhancement,
color compensation, …

LVDS

Driver Board

TCON

Driver IC
Control signal
generation

Panel Int'f

LVDS
RSDS
Mini-LVDS

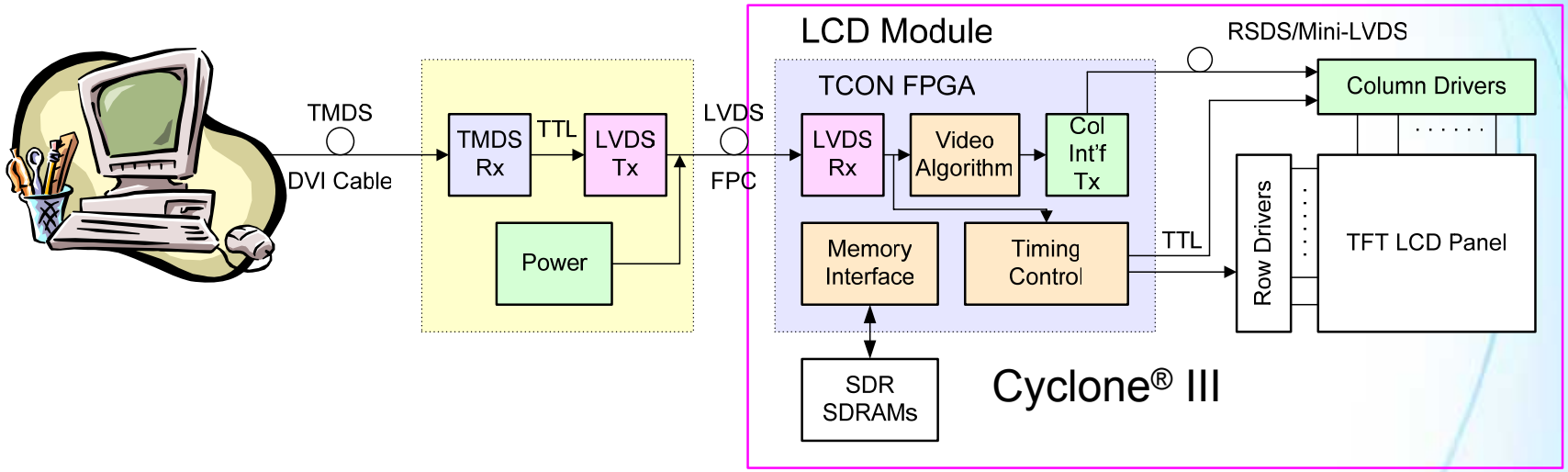
CRT

Rear
Projection

LCD

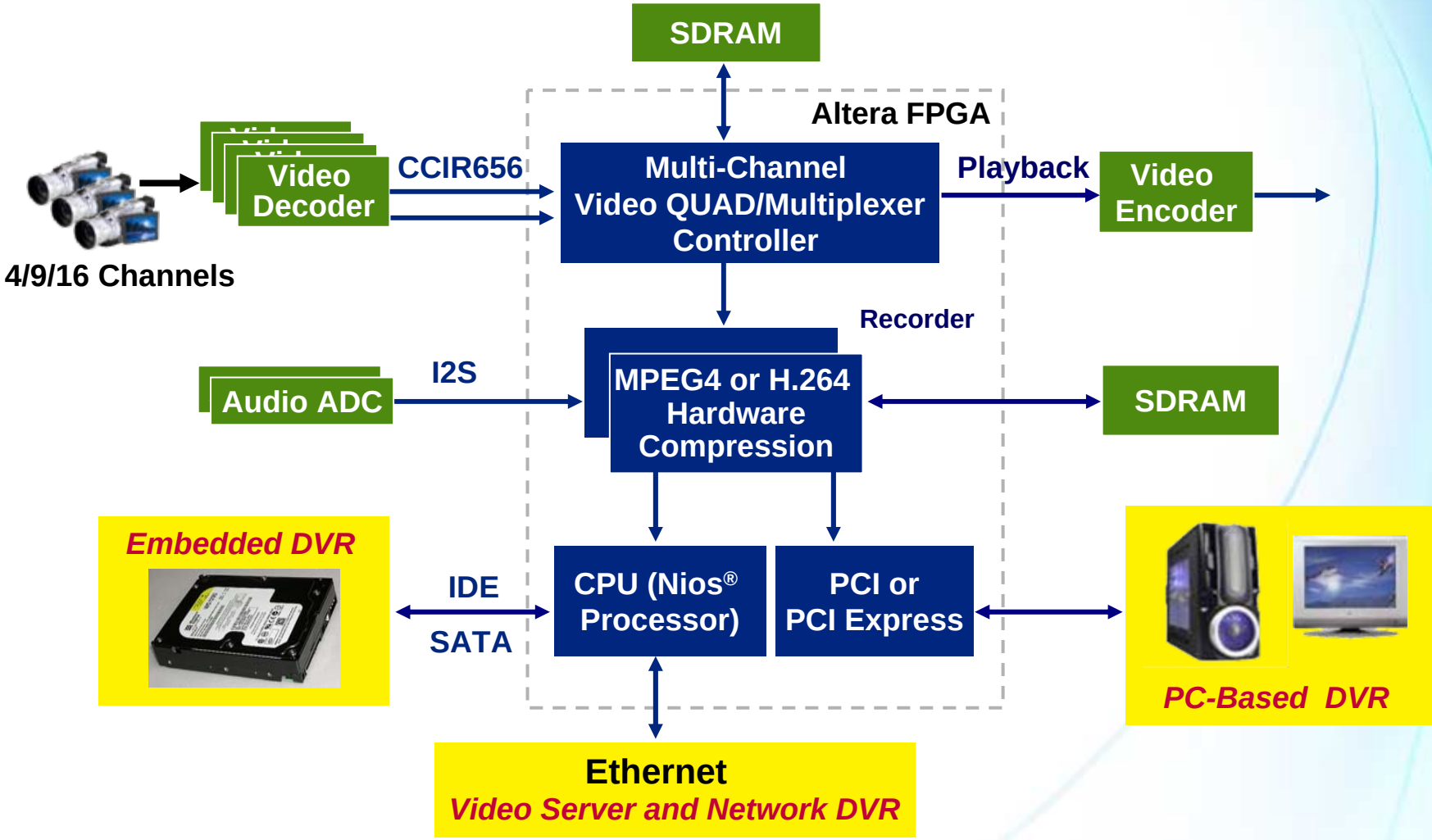
PDP

Digital Display Interfaces

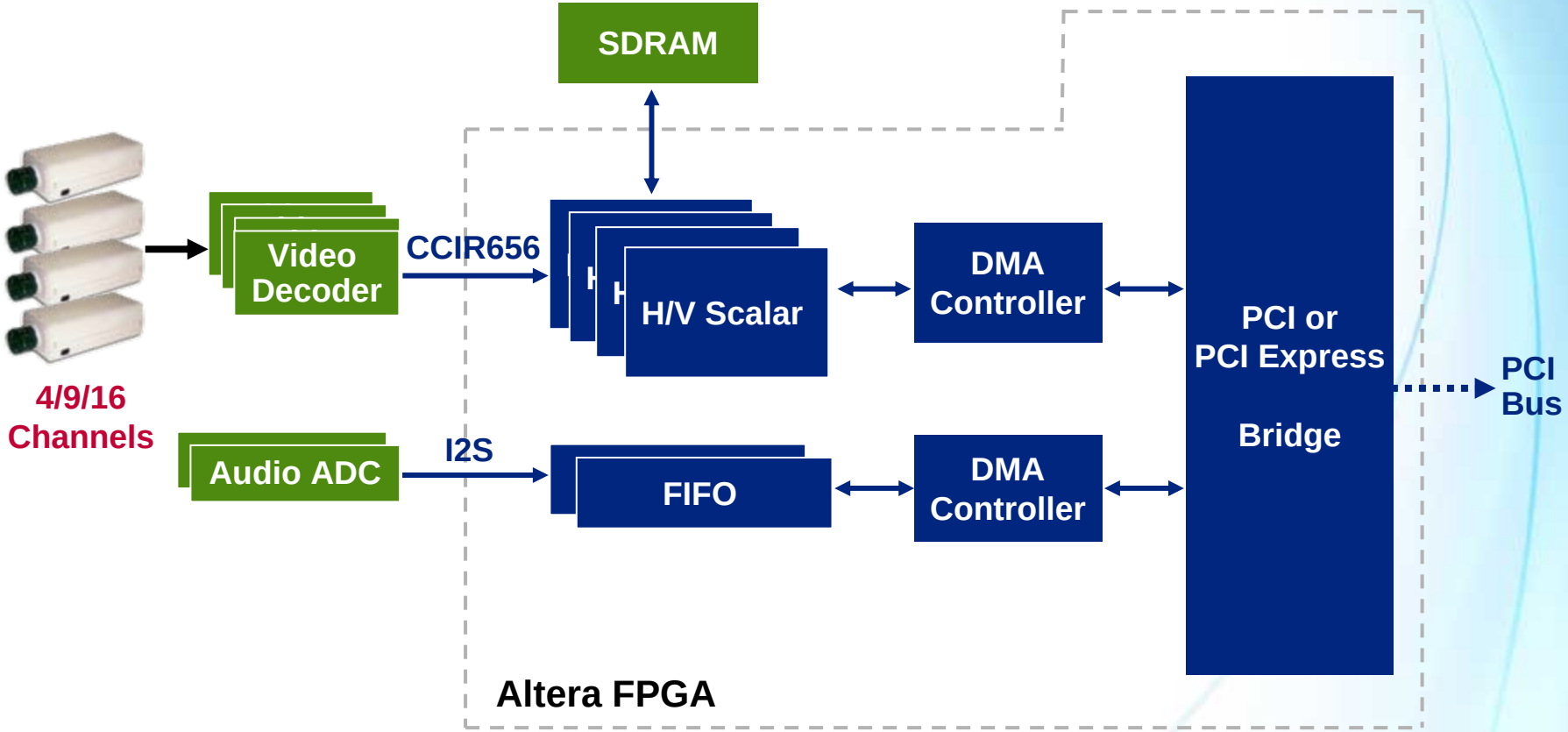


- Transition minimized differential signaling (TMDS): Connection between PC and buffer board with DVI cable
- LVDS: Connection between buffer board and TCON board with FPC
- Reduced swing differential signaling (RSDS)/mini-LVDS : Connection between TCON board and column driver board with FPC

DVR System: Hardware Compression



PCI-Based DVR: PC Software Compression



Reference Designs and IP Cores

IP Examples – Video

I/O and system

- PCI Express
- Serial RapidI/O™ standard
- Electro-magnetic interference filter (EMIF) interface
- Asynchronous Serial Interface (ASI)
- Serial digital interface (SDI)
- ATA HDD (Nuvation)
- MPEG-2 transport
- 10/100/1000 Ethernet
- DDR/DDR2 controller

Pre-/post-processing

- Scaler
- Deinterlacer
- 2D finite impulse response (FIR) filter
- 2D median filter
- Color space converter
- Chroma resampler
- Gamma corrector
- Alpha blender
- Highest quality HDTV upconversion (Let It Wave)
- Advanced encryption standard (AES)/data encryption standard (DES)/Sha-1 Encryption (CAST)

Video and Image Processing Suite

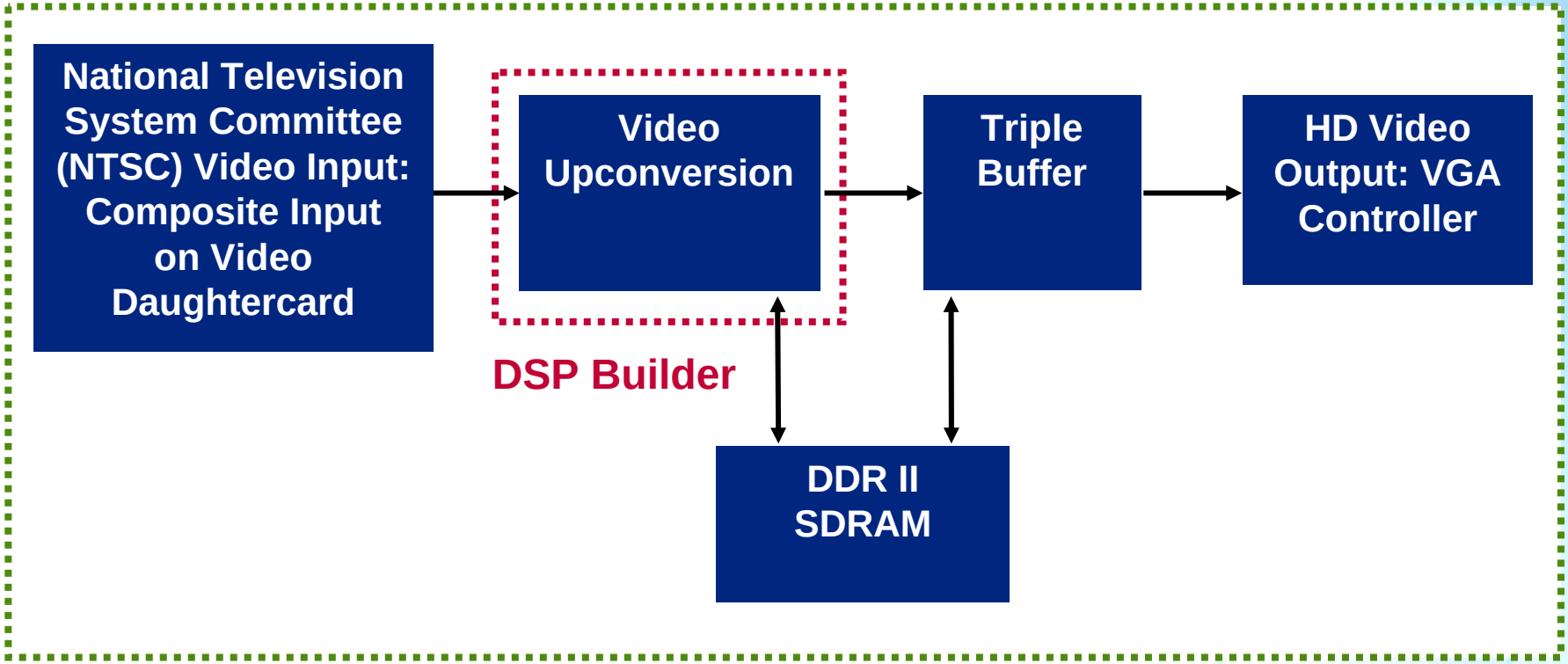
Compression

- H.264 MP, HP (ATEME)
- H.264 BP (4i2i, CAST, W&W)
- H.264 CABAC/CAVLC (ATEME)
- H.264 Loop Filter (ATEME)
- MPEG-4 SP/ASP (CAST, Barco)
- JPEG (CAST, Barco)
- JPEG2000 (CAST, Barco, BroadMotion)

Video and Image Processing Suite

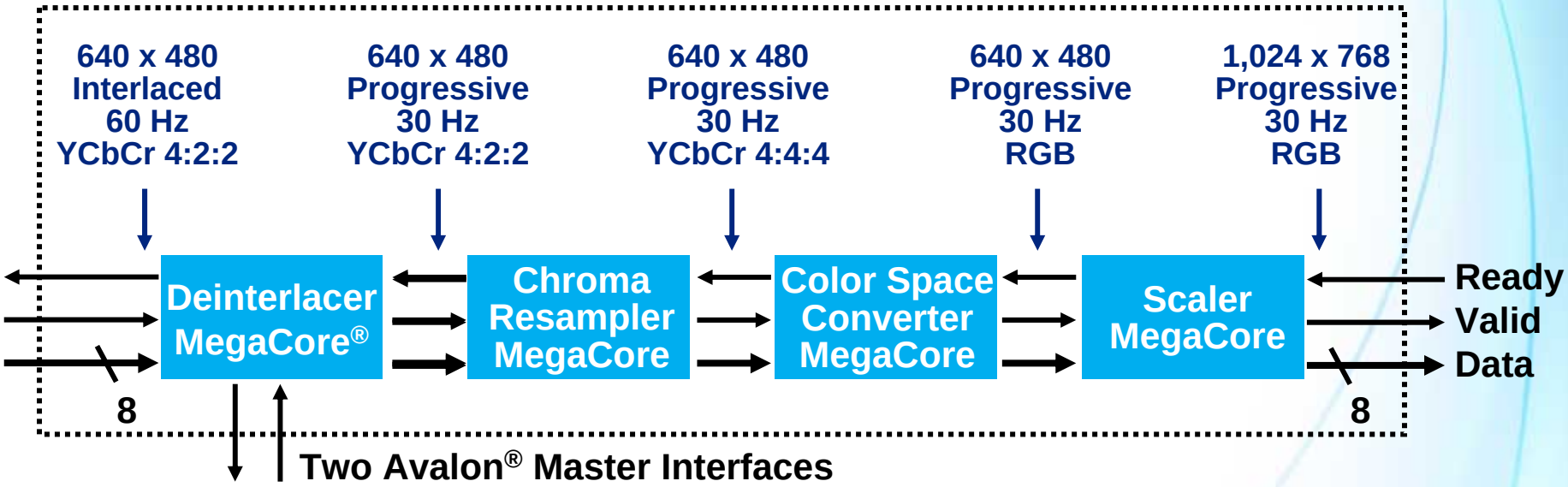
Core	Function
Deinterlacer	Converts interlaced video formats to progressive video format
Color space converter	Converts image data between a variety of different color spaces
Scaler	Resizes and clips image frames
Gamma corrector	Performs gamma correction on a color space
Alpha blending mixer	Mixes and blends multiple image streams, including picture-in-picture (PIP)
Chroma resampler	Changes the sampling rate of the chroma data for image frames
2D filter	Implements a 3x3, 5x5, or 7x7 FIR filter on an image data stream to smooth or sharpen images
2D median filter	Implements a 3x3, 5x5, or 7x7 filter that removes noise in an image by replacing each pixel value with the median of neighboring pixel values
Line buffer compiler	Efficiently maps image line buffers to Altera on-chip memory

VIP Upconversion System



Video Upconversion Datapath

- Entire datapath is assembled in DSP Builder



Display Application Resources

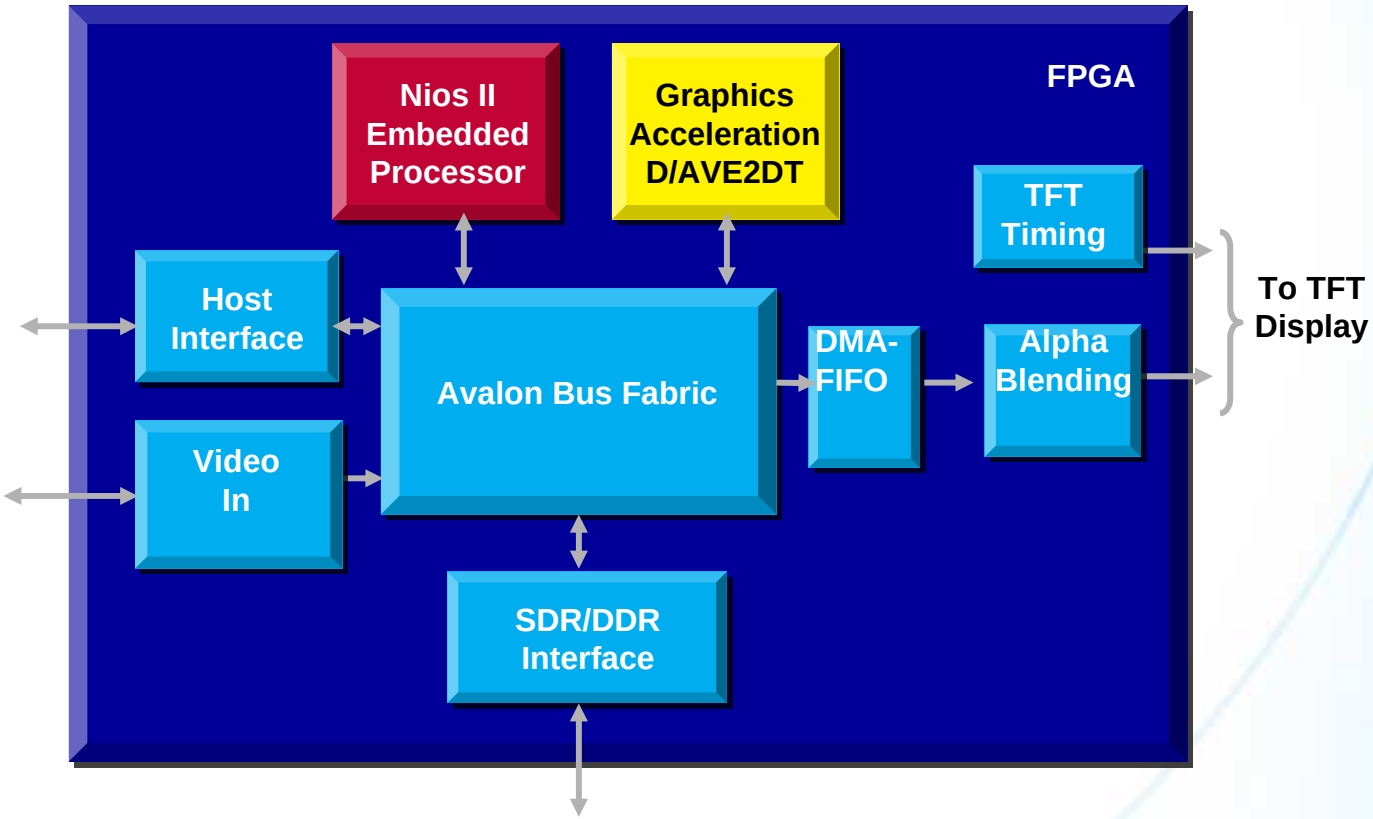
- Video and Image Processing Suite
  - Library of nine common video and image processing functions optimized for Altera FPGAs
- Video processing reference design
- Low-Cost FPGA Starter Kit, Cyclone III Edition
- Microtronix ViClaro II HD Video Enhancement Development Platform
- *Develop a Display System Using Low-Cost Cyclone III FPGAs* QuickCast
- White papers
  - *Cyclone III FPGAs Enable a New Class of LCD HDTVs*
  - *A Flexible Architecture to Drive Sharp Two-Way Viewing Angle and Standard LCDs*
  - *Satisfy the Demand for Rapid Feature Enhancement in Consumer Display Products*

www.altera.com/cyclone3-markets

Video and Image Processing Resources

- Video and image processing IP
  - Library of nine common video and image processing functions from Altera
  - Compression IP available from Altera partners such as ATEME, Barco, 4i2i, and CAST
- Video processing reference design
- Video training course
  - Advanced DSP design: using FPGAs to architect and optimize a video and image processing system
- Low-cost FPGA Starter Kit, Cyclone III Edition
- Video daugtercard
- Design Video and Image Processing Systems with Low-Cost Cyclone III FPGAs QuickCast
- White papers
  - *Video and Image Processing Design Using FPGAs*
  - *Video Surveillance Implementation Using FPGAs*
  - *Medical Imaging Implementation Using FPGAs*

Graphics Processor Platform



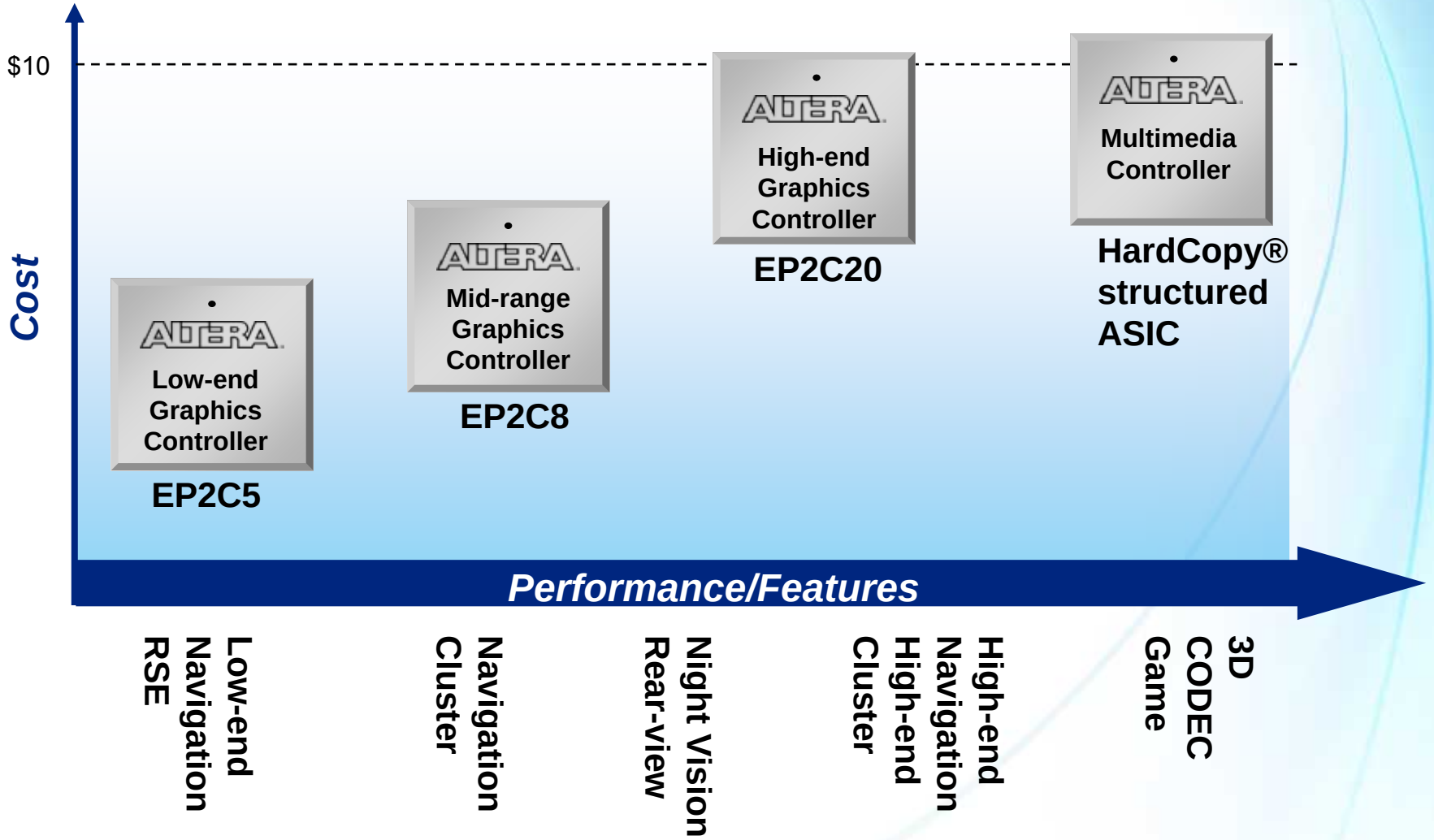
Graphics Solutions Selector Guide

Altera Graphics Solutions	Lowest cost	Low-end	Mid-range	High-end	SOC
Applications	RSE Rear-view camera	RSE Cluster Rear-view Night vision Low-cost Navi	High-end Cluster Navigation	High-end Navigation Game Console additional functions	Multimedia Controller High-end graphics Audio Codec and other functions
	Supported in				
Target Device	EP1C3T100 EP2C5T144	EP2C5F256	EP2C8F256	EP2C20F256	HC210W
Graphics Feature List					
Layering	-	Yes	Yes	Yes	Yes
Alpha Blending (layer alpha, pixel alpha)	-	Yes	Yes	Yes	Yes
Clipping / Resizing	Yes	Yes	Yes	Yes	Yes
Video input	Yes	Yes	Yes	Yes	Yes
Picture-in-Picture	-	Yes	Yes	Yes	Yes
Colour Depth	-	Yes	Yes	Yes	Yes
Anti-aliasing	-	on Host Micro	Yes	Yes	Yes
Line Drawing	-	on Host Micro	Yes	Yes	Yes
Polygon Drawing	-	on Host Micro	Yes	Yes	Yes
Circles & Ellipses	-	on Host Micro	Yes	Yes	Yes
Quadratic and Cubic Bézier	-	on Host Micro	Yes	Yes	Yes
Bitmap BLIT	-	on Host Micro	Yes	Yes	Yes
Multiple render-attributes	-	on Host Micro	Yes	Yes	Yes
Multiple Bitmap Formats	-	on Host Micro	Yes	Yes	Yes
HW Support for Matrix Computation	-	-	Yes	Yes	Yes
Graphics Library & OpenGL Compliance	-	on Host Micro	on Host Micro	Yes	Yes
3D Graphic rendering engine	-	-	-	-	Yes
RGB Digital Output	Yes	Yes	Yes	Yes	Yes
LVDS Output	Yes	Yes	Yes	Yes	Yes
Memory Interfaces (SDR, DDR, Flash)	-	Yes	Yes	Yes	Yes
Flexible Host Interfaces	-	Yes	Yes	Yes	Yes

Graphics Hardware Acceleration

- D/AVE (Display Controller and Accelerated Vector Engine)
  - Provided by TES (former ThalesEE)
  - A specialized graphics acceleration hardware
  - Innovative, vector-based rendering engine
  - High render quality (sub-pixel and anti-aliasing)
  - Low resource consumption
  - Flexible design, easy to parallelize, easy to add new functionality
  - Low memory bandwidth consumption
  - Key features:
    - Blit operation in D/AVE 2DT-S (direct blit, stretch blit, transparency, bilinear filtering, per pixel alpha, coloring, antialiasing)
    - Lines (arbitrary width, round endpoints, truncated endpoints, alpha gradients, soft edges (blurring))
    - Polygons (triangles and quadrangles, alpha gradients, soft edges (blurring), per edge controls for anti aliasing)
    - Circles and ellipses (all conic sections, filled or with arbitrary width, arcs of 0° -360° , soft edges, alpha gradients)
    - Quadratic and cubic Bézier (approximate by circle arcs, arbitrary width, round or truncated endpoints, outlines blurring, alpha gradients)
    - Render-attribute: color, pattern, texture
    - Supported bitmap formats: Alpha8 (8Bit), Alpha8In32 (8Bit), RGB 555 (16Bit), RGB 565 (16Bit), ARGB 4444 (16Bit), RGB 888 (32Bit), ARGB 8888 (32Bit)

Multimedia Solutions Roadmap



Devices

The Significance of Power

- Challenges
  - Thermal management
  - Fixed power budgets
  - Battery life
- Cyclone III FPGAs allow you to do more with less power

Application Examples

Portable and Small Form Factor Products

Pico-cell Communication

Increase functionality while reducing power

Display Application Challenges

Display application examples

- LCD and plasma displays and projectors
- DVD player/recorder
- Automotive/navigation displays
- Medical and industrial imaging

High Functionality

- Higher video-rate processing for standard-definition (SD) to high-definition (HD) conversion
- Larger display panels require image enhancement to reduce/eliminate digital video noise artifacts
- Demand for upgrade path to next-generation features (e.g. video, 3D rendering, picture-in-picture, enhanced on-screen display (OSD))
- Single graphics controller solution to address range of display sizes, external memory types, feature sets

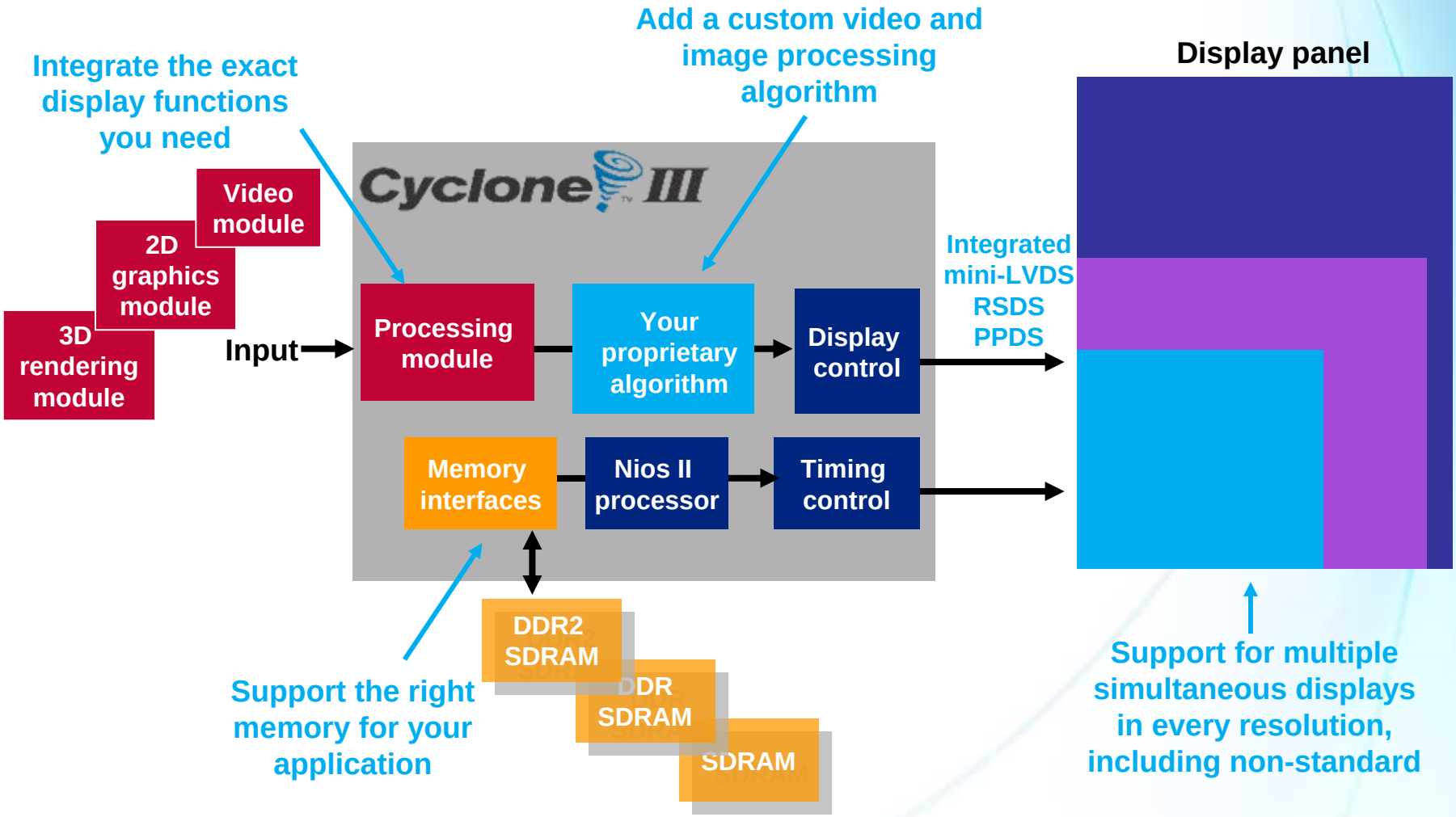
Low Cost

- Declining profit margins over product lifecycle
- ASIC design cycles do not meet time-to-market requirements

Low Power

- Battery life for portable applications

Universal, Flexible, and Scalable Display Controller



Video and Image Processing Challenges

Video and imaging application examples

- Video surveillance
- Video conferencing
- Medical/industrial/military imaging
- Automotive infotainment

High Functionality

- Video standards continue to evolve, driving higher data rates (e.g. H.264)
- Processing requirements are outpacing digital signal processing (DSP) performance

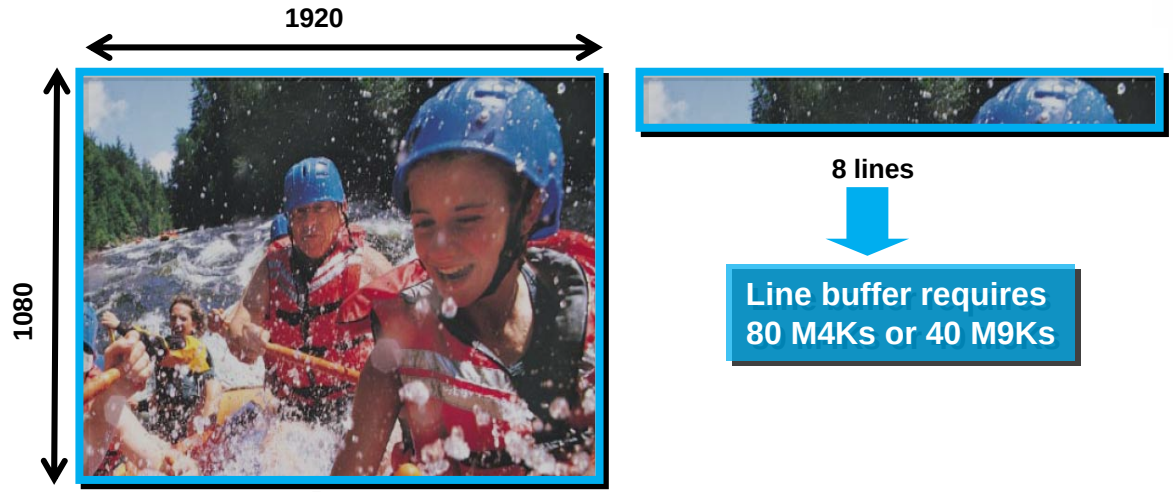
Low Cost

- Expensive or multiple DSP processors required for HD class video
- ASIC design cycles do not meet time-to-market requirements

Low Power

- Thermal dissipation can interfere with sensitive charge-coupled device (CCD) image capture devices

Video Line Buffering Application

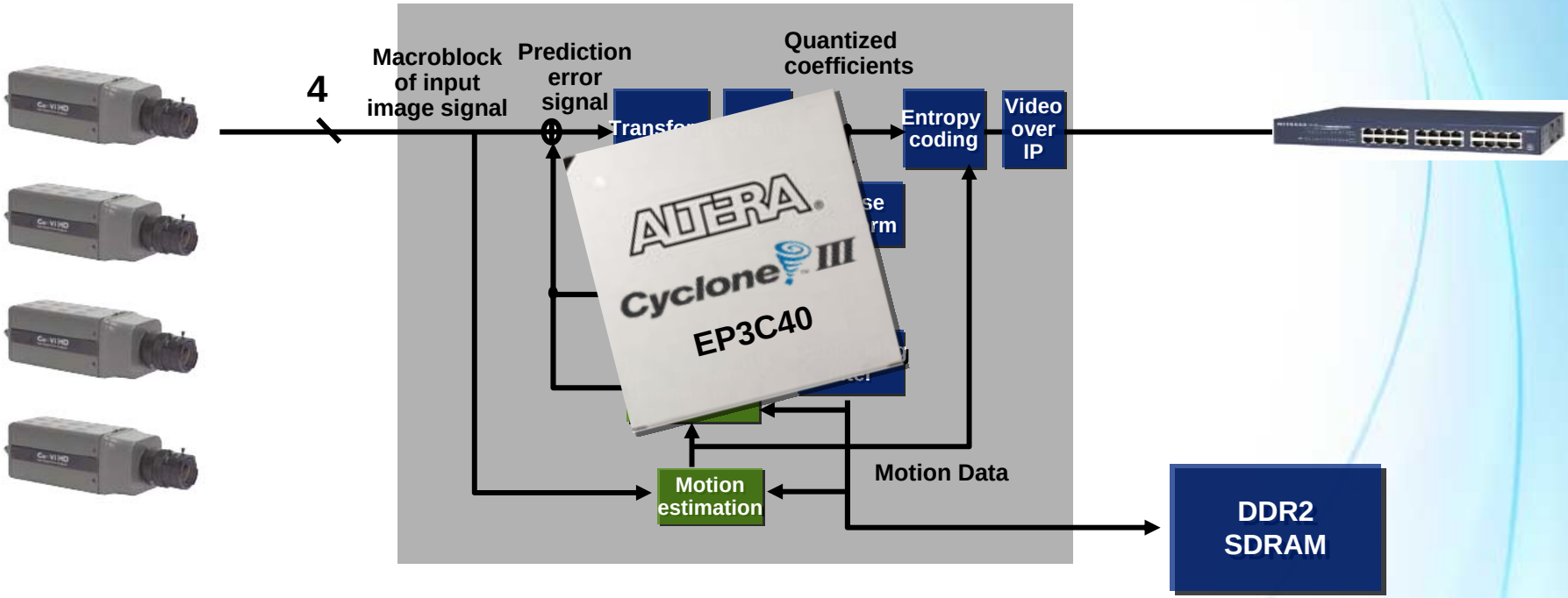


Buffer eight lines of video in a mid-range Cyclone II device

Buffer eight lines of video in the smallest Cyclone III device

	Cyclone II device – EP2C35	Cyclone III device – EP3C5
Volume price	$18.00	$4.00

Enable Low-Cost H.264 Encoding



Processing intensive blocks

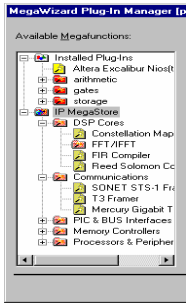
Implement SD H.264 Encoder in a Single Device for Under ¼ W and $5 per Channel

Tools and Development Kits

System Integration Solution

Create Design Blocks

IP



Model-Based Design

'C'-Based Design

HDL Entry

```
entity par_fir is
 port (
   io0_gpo : out std_logic_vector(15 downto 0);
   io0_gpi : in std_logic_vector(15 downto 0);
   clock : in std_logic;
   reset : in std_logic
     );
end entity;
```

Embedded Software Development

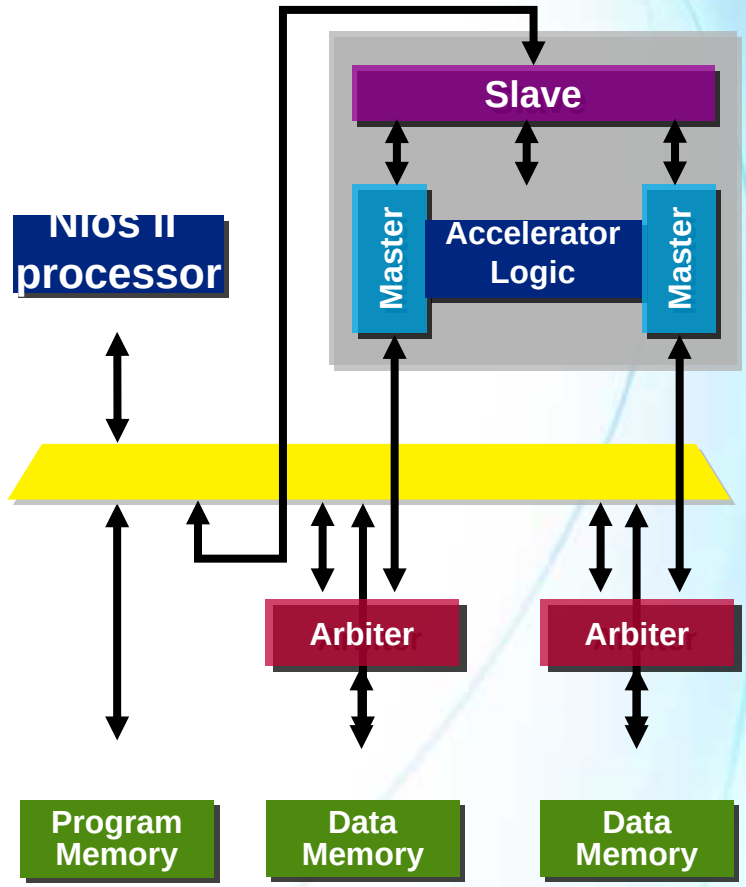
Integrate System

Including

ALTERA®

Nios II C-to-Hardware (C2H) Compiler

- Another tool that extends FPGA design to higher abstraction level
- Brings software productivity to hardware design
- Accelerates time-critical C code
  - Converts ANSI C subroutines to hardware accelerators
  - **Automatically** adds accelerators to a Nios II system
- Tightly integrated into Nios II embedded processor design environment



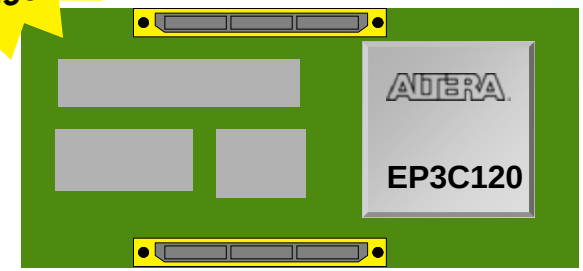
Cyclone III Base Kits

Available April 2007 $199

Cyclone III FPGA Starter Kit

- EP3C25F324
- HSMC connector
  - Allows daughtercard expansion
- On-board memories:
  - 256-Mbit DDR
  - 1-Mbyte sync SRAM
  - 16-Mbyte flash

Available October 2007 $695

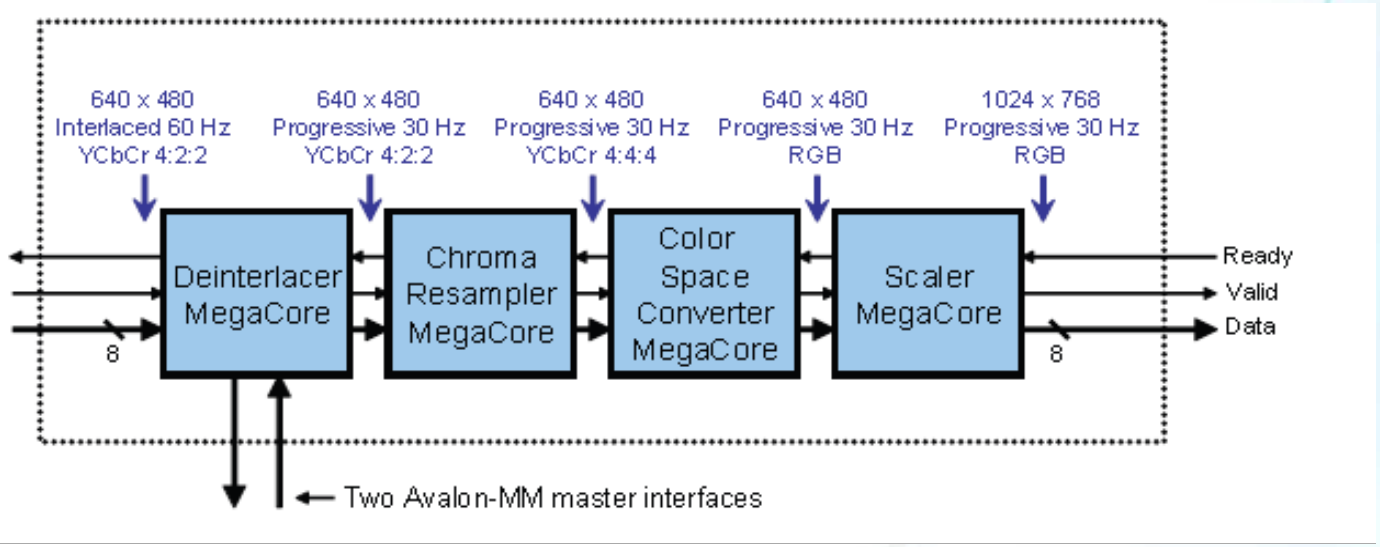


Cyclone III Dev Kit

- EP3C120F780
- 2x HSMC connectors
  - Allows daughtercard expansion
- 10/100/1000 Ethernet
- On-board memories:
  - 256-Mbit DDR2
  - 8-Mbyte sync SRAM
  - 64-Mbyte flash

Live Demo

- Video Image Processing Suite reference design:
  - Video and image processing upconversion example design demonstrates upconversion from a SD video stream in National Television System Committee (NTSC) format to a HD output resolution (1024 × 768).
  - Reference: http://www.altera.com/support/refdesigns/sys-sol/broadcast/ref-post-processing.html
  - Literature: http://www.altera.com/literature/an/an427.pdf



Conclusion

Conclusion

- Cyclone III devices deliver low power, high performance, and low cost to enable customer innovation
- DSP Builder, Quartus® II design software, and development kits improve productivity
- Display and video image processing application resources facilitate customers' design