Accelerating WiMAX DUC & DDC System Designs

January 2007, Version 2.1

Application Note 421

Introduction

The worldwide interoperability for microwave access (WiMAX) standard is an emerging technology with significant potential that is poised to revolutionize the broadband wireless internet access market. The diverse hardware requirements for these systems including processing speed, flexibility, integration and time-to-market necessitate an FPGA based implementation platform. Altera® high-density FPGA devices provide WiMAX OEMs with significant competitive advantages by minimizing development time and resources, maximizing first-time success, and accelerating time-to-market.

This application note describes how system architects and hardware designers can accelerate the design of digital up conversion (DUC) and digital down conversion (DDC) functions for WiMAX basestations using Altera devices, tools, intellectual property (IP) and reference designs. The system design challenges associated with WiMAX DUC and DDC designs are illustrated and the companion reference designs act as a demonstration of how to overcome these challenges using while achieving an optimized and cost effective hardware implementation.

Key Features of the Reference Designs

The DUC and DDC reference design has the following key features:

- DSP Builder based design methodology to significantly reduce the development time
- Multi-channel filter design techniques to achieve cost effective solutions
- Highly parameterizable IP MegaCore® functions to further reduce development time
- Support for multiple transmit and receive antenna configurations
- Easily modifiable to support scalable channel bandwidths
- Compliant to the draft WiMAX standard (*IEEE 802.16*) [1]

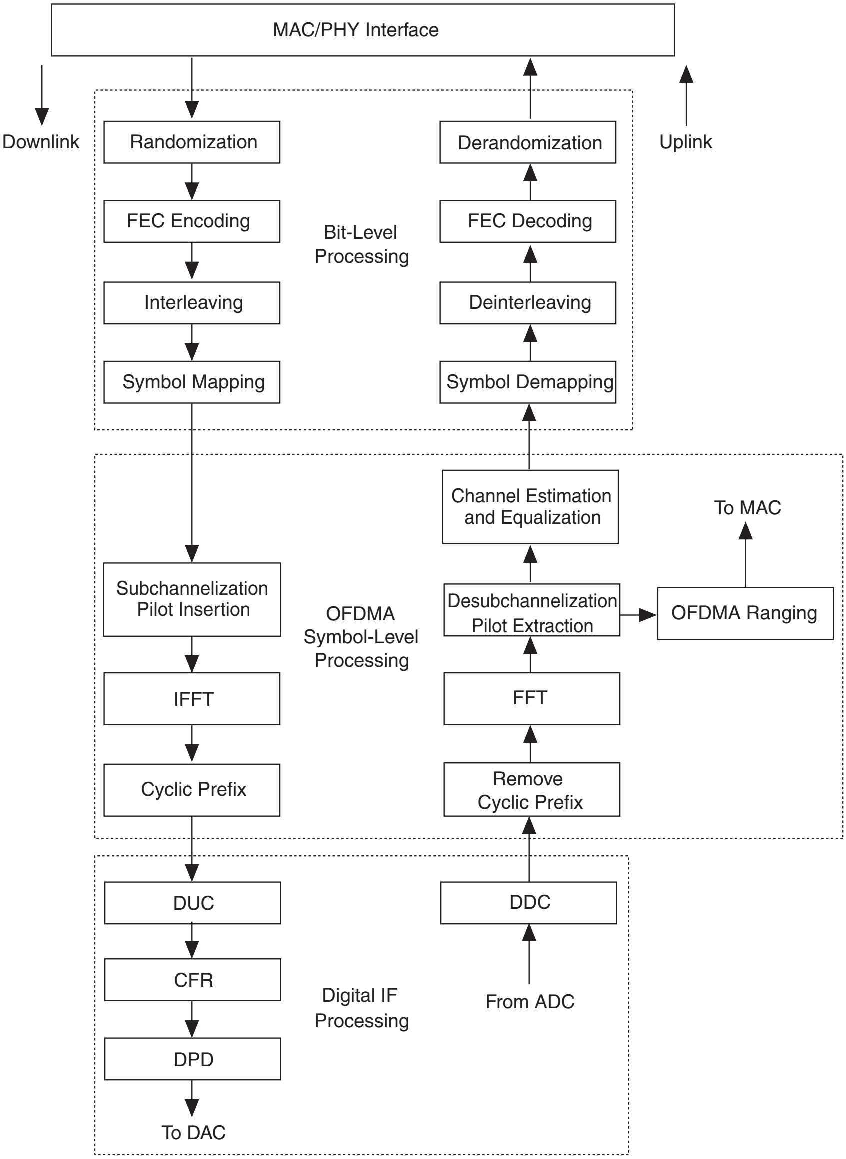
☞ Please contact your local **Altera sales representative** for a copy of the reference design.

For more information on *IEEE 802.16*, refer to the *IEEE Standard for Local and Metropolitan Area Networks, Part 16: Air Interface for Fixed Broadband Wireless Access Systems*, IEEE P802.16-REVd/D5-2004, May 2004.

WiMAX Physical Layer

Figure 1 shows an overview of the *IEEE 802.16e-2005* scalable orthogonal frequency-division multiple access (OFDMA) physical layer (PHY) for WiMAX basestations.

Figure 1. WiMAX Physical Layer Implementation



Altera's WiMAX building blocks include bit-level, OFDMA symbol-level, and digital intermediate frequency (IF) processing blocks. For bit-level processing, Altera provides symbol mapping/demapping reference designs and support for forward error correction (FEC) using the Reed-Solomon and Viterbi MegaCore® functions.

The OFDMA symbol-level processing blocks include reference designs that demonstrate subchannelization and desubchannelization with cyclic prefix insertion supported by the fast Fourier transform (FFT), and inverse fast Fourier transform (IFFT) MegaCore functions. Other OFDMA symbol-level reference designs illustrate ranging, channel estimation, and channel equalization.

The digital IF processing blocks include single antenna and multi-antenna digital up converter (DUC) and digital down converter (DDC) reference designs, and advanced crest-factor reduction (CFR) and digital predistortion (DPD).

This application note illustrates the functionality and implementation of the DUC and DDC functions.

For more information on Altera WiMAX solutions, refer to the following application notes:

- *AN 412: A Scalable OFDMA Engine for Mobile WiMAX*
- *AN 430: WiMAX OFDMA Ranging*
- *AN 434: Channel Estimation & Equalization for Mobile WiMAX Basestations*
- *AN 439 Constellation Mapper and Demapper for WiMAX*

System Design Requirements

This section outlines some of the system design aspects that must be considered when implementing a WiMAX digital up or down converter.

The WiMAX standard specifies various operating modes. This particular reference design has been designed to support scalable orthogonal frequency-division multiple access (OFDMA) modulation with a Fast Fourier Transform (FFT) size of 1024. The operating bandwidth is 10MHz.

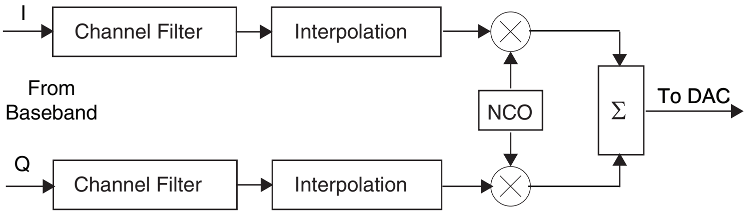
Digital Up Converter

A digital up converter (DUC) provides the link between the digital baseband and analog RF front end and is required on the transmitter of a generic transceiver. The sampling frequency of the baseband data stream is increased before it is modulated onto a high frequency carrier.

The algorithm consists of three stages shown in Figure 2:

1. Channel Filter – Applies pulse shaping to ensure that the spectral mask and restrictions imposed by the regulatory body are not violated.
2. Interpolation – The sampling frequency of the baseband samples are increased. Filtering is required to mask spectral images that appear as part of the interpolation process.
3. Mixer/Combiner – A numerically controlled oscillator (NCO) generates two orthogonal sinusoids at the carrier frequency and these are mixed with the I and Q streams. Finally the outputs of the mixers are added together before being passed on to the digital-to-analog converter (DAC).

Figure 2. Digital Up Converter Block Diagram



For this DUC reference design, the sampling rate specifications are:

Baseband:	11.424 million samples per second (MSPS)
IF:	91.392 MSPS

Hence there is a total interpolation factor of 8.

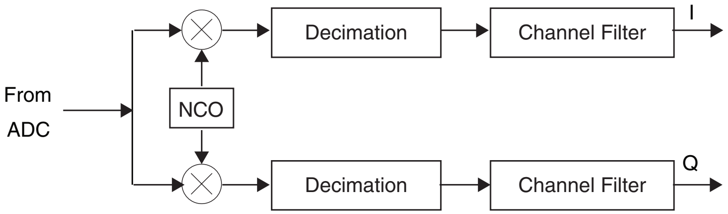
Digital Down Converter

A digital down converter (DDC) provides the link between the analog RF front end and the digital baseband of a receiver. The data is demodulated from the high frequency carrier and subsequently the sampling frequency of the data stream is reduced. The data stream is then compatible with the baseband modem.

The algorithm consists of three stages shown in Figure 3:

1. Mixer – A numerically controlled oscillator (NCO) generates two orthogonal sinusoids at the carrier frequency and these are mixed with the input stream from the analog-digital-converter (ADC).
2. Decimation – The sampling frequency of the intermediate frequency (IF) samples is decreased. Filtering is required to guard against aliasing in the decimation process.
3. Channel Filter – Applies pulse shaping to attenuate any out of band energy in the baseband data.

Figure 3. Digital Down Converter Block Diagram



For this DDC reference design, the sampling rate specifications are given by:

IF:	91.392 MSPS
Baseband:	11.424 MSPS

Hence there is total decimation factor of 8.

Data Path Quantization

Each signal bus within a digital signal procession (DSP) design is represented by a finite number of bits. This finite representation often leads to a loss in precision in the numbers that introduces quantization noise. It is up to the system designer to decide what quantization noise is acceptable and architect the data path accordingly.

The number of bits required to represent data often scales throughout a design. This is because a good design will prevent overflow caused by operations such as multiplication and addition.

Subsequently, the required bit width at the output of full precision finite impulse response (FIR) filters, such as those used in the reference designs, is significantly greater than the input data width. It is necessary to scale this output data to a satisfactory length that trades off performance, total logic area, power and ultimately total cost per channel.

One advantage of using Altera FPGAs for this type of design is the flexibility of the device architecture. Data widths can be adjusted throughout the design by the system architect to achieve exactly the precision and overflow protection required, at the same time as achieving the selectivity and attenuation desired in the filters. This flexibility is not possible using an application specific standard part (ASSP).

In addition, the dedicated high speed multiplier logic that is part of the Stratix® II and Cyclone™ II device families have several configurations that make it possible to tradeoff between resource utilization and multiplier width.

The most basic method for reducing the bit width of the filter output is truncation. This can be achieved by simply discarding a number of the least significant bits. This method requires no additional hardware complexity, but it does lead to an error that is always negative. This error adds a DC bias to the data. To minimize this, you can utilize additional logic that rounds the resulting data to the nearest integer (under the assumption that the discarded bits represent the fractional parts).

The method of rounding “away from zero” will introduce a bias for midpoint values: for example, 1.5 will be rounded to 2, 2.5 to 3, and so on. Thus, this technique always rounds “up” and this also leads to a DC bias. “Convergent” rounding eliminates the possibility of bias, since rounding to the nearest even number in the case of mid-point values has a 50% probability of rounding up and 50% probability of rounding down: for example, 1.5 is rounded to 2, 2.5 to 2, and so on. Thus, half the time it rounds up and the other half it rounds down.

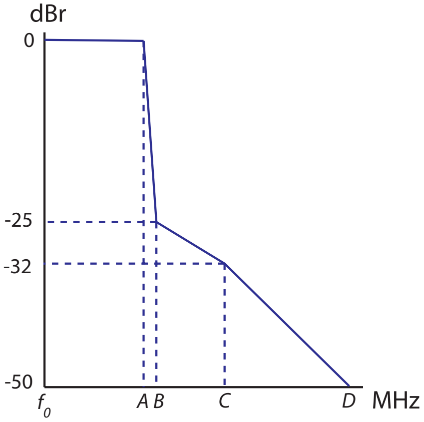
A parameterizable library block is provided to achieve convergence rounding to 16 bits in the DUC/DDC data paths.

Spectral Mask

Equipment manufacturers of WiMAX systems are required to ensure their systems comply with spectral regulations to prevent interference with other telecommunication devices and WiMAX channels.

This leads to the requirement that filters and power amplifiers must be designed such that there is no spectral radiation beyond the allowed channel bandwidth. The WiMAX standard [2] states that the transmitted spectral density of the signal should fall within the spectral mask given by Figure 4.

Figure 4. Transmit Spectral Mask (10MHz Channelization)



	A	B	C	D
Frequency (MHz)	4.75	5.45	9.75	14.75

FIR Filter Design

Detailed FIR filter design techniques are beyond the scope of this document but this section provides an overview of the tradeoffs necessary when defining the filters in the data path. Commonly, filter design may be achieved using computer aided design tools such as the FIR compiler coefficient generator or the MATLAB filter design toolkit.

Physically realizable filters have non-ideal frequency response because the filter taps are derived by truncating the ideal impulse response of the filter. Truncation of the impulse response compromises the transition width between the pass band and stop band, and so the number of taps must be traded off with the necessary sharpness of the transition.

Truncation of the impulse response also leads to ripples in the frequency response because of the discontinuity at the edges. Since only a small ripple may be tolerated, a tapered window function is used to smooth the edges of the impulse response. Although this achieves less ringing in the response, the stop band attenuation is reduced.

Hence filter design requires tradeoffs between the number of taps, the pass band ripple and the stop band attenuation. Ultimately a good filter design meets the required spectral specifications whilst minimizing the necessary hardware complexity.

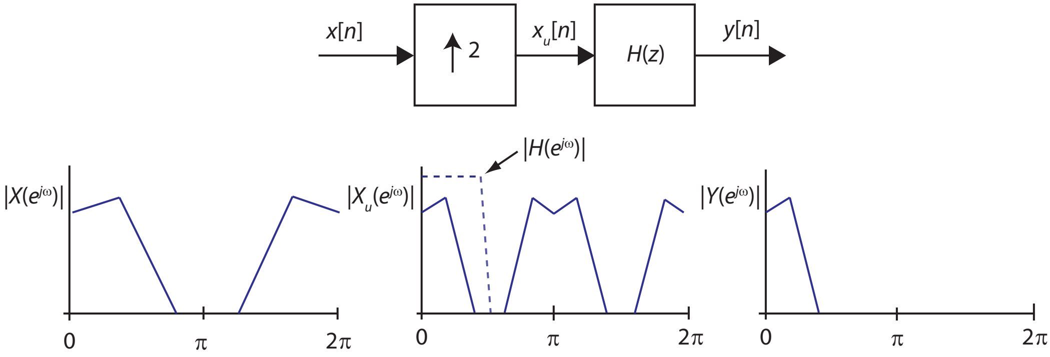
Multirate Filter Design

Digital up and down converters are required to increase/decrease the sampling frequency of the data stream. This can be achieved using interpolators and decimators respectively. Since the mathematics are beyond the scope of this document, only an overview of interpolation and decimation is given before considering how to achieve good hardware efficiency by cascading interpolation and decimation stages.

In the time domain, an increase in the sampling rate by a factor L is achieved by inserting $L-1$ equidistant zero-valued samples between two consecutive samples of the input sequence. In the frequency domain, the Fourier transform is compressed by a factor of L, and so the spectrum has spectral images introduced. It is necessary to remove these images using an appropriate low pass filter.

Figure 5 illustrates these principles and the associated spectra where the interpolation factor L=2.

Figure 5. Interpolation Block Diagram and Spectra for L=2

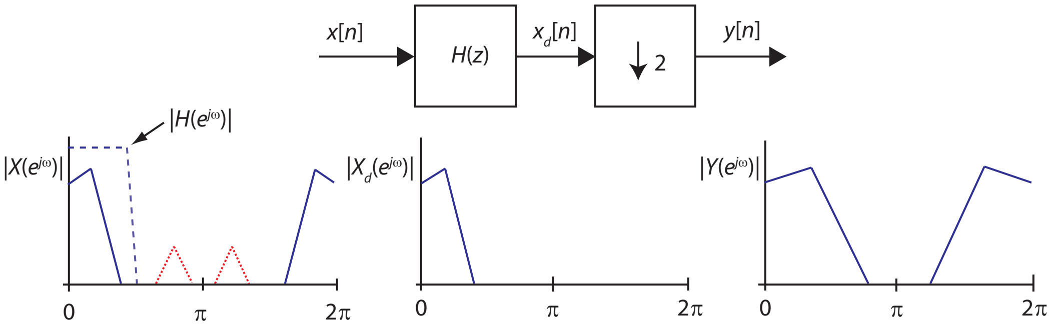


To decrease the sampling rate by a factor *L*, a decimation operation is required and is implemented by keeping every L^{th} sample of the input sequence and discarding the other *L-1* in-between samples.

In the frequency domain, this leads to aliasing if there are frequency components in the input sequence that are greater than half of the target sampling frequency. A low pass filter is therefore required before the decimation operation to ensure that out-of-band frequencies are attenuated. This low pass filter has the same specifications as the filter required for a interpolate by *L*.

Figure 6 shows the block diagram for decimation by 2 and the associated spectra. The dotted red components represent harmonics that can not be represented by the target sampling frequency, and are attenuated by the low pass filter to prevent aliasing.

Figure 6. Decimation Block Diagram and Spectra for L=2



In general, you can reduce the hardware complexity of a sample rate converter by cascading multiple interpolation/decimation stages [3]. This is because each stage can exploit the fact that the transition band does not have to be as sharp in the knowledge that certain regions of spectrum have already been attenuated by the previous filter. A shallower transition band leads to less taps, which in turn leads to a reduction in multiplier resources. "Multistage Partitioning" on page 18 describes how cascaded rate changes are exploited in the reference design.

Minimum Stop Band Attenuation

The target minimum stop band attenuation for the WiMAX DUC/DDC design should be less than -90dB. This will enable the filters to reject interference from or to adjacent and non adjacent channels.

Maximum Pass Band Ripple

The cascaded filter sections should have a pass band peak-to-peak ripple of no more than 0.05 dB. It is necessary to prevent distortion of the pilot and data carriers because this would lead to poor constellation and channel estimation recovery.

Oscillator Spectral Purity

Data samples are mixed with the channel carrier frequency at the IF interfaces in both the DUC and DDC designs. This carrier frequency is generated using a hardware block called a numerically controlled oscillator (NCO).

Since the NCO only generates an approximation of a sinusoid, the power of the desired spectral component relative to the highest level undesired harmonic component is known as the spurious-free dynamic range (SFDR). Undesired spectral components are a direct consequence of the finite precision and can lead to substantial intermodulation distortion.

For this type of design, a SFDR of at least -100dB is recommended.

DUC Specific Specifications

Relative Constellation Error (RCE)

Filtering and Quantization in the up conversion chain introduces noise onto the transmitted spectra. It is necessary to ensure that the signal-to-noise ratio at the receiver equipment is not degraded by greater than 0.5dB due to the additional noise introduced by the transmitter.

The specific algorithm [4] defined by the equation below quantifies the magnitude of the error of the transmitted constellation point relative to the desired constellation point.

$$\text{Error}_{RMS} = \frac{\displaystyle\sum_{i=1}^{N_f} \frac{\displaystyle\sum_{j=1}^{L_P}\left[\sum_{k=1}^{N_{FFT}}\left\{(I(i,j,k)-I_0(i,j,k))^2+(Q(i,j,k)-Q_0(i,j,k))^2\right\}\right]}{P_0\cdot L_P\cdot N_{FFT}}}{N_f}$$

where:

L_P is the length of the packet
N_f is the number of frames for the measurement
$(I_0(i,j,k), Q_0(i,j,k))$ denotes the ideal symbol point of the i^{th} frame, j^{th} OFDMA symbol of the frame, k^{th} subcarrier of the OFDMA symbol in the complex plane
$(I(i,j,k), Q(i,j,k))$ denotes the observed point of the i^{th} frame, jth OFDMA symbol of the frame
k^{th} is the subcarrier of the OFDMA symbol in the complex plane
P_0 is the average power of the constellation
N_{FFT} is the FFT size

The required performance is given by Table 1.

Table 1. Relative Constellation Error Specifications

Burst Type	Required RCE (dB)
QPSK $^1/_2$	-16.4
QPSK $^3/_4$	-18.2
16QAM $^1/_2$	-23.4
16QAM $^3/_4$	-25.2
64QAM $^2/_3$	-29.7
64QAM $^3/_4$	-31.4

Notes for Table 1:

(1) The burst type is expressed in terms of quadrature phase shift keying (QPSK) or quadrature amplitude modulation (QAM).

DDC Specific Specifications

Receiver Sensitivity

The receiver sensitivity is defined as the weakest received signal level that must result in a bit error rate (BER) performance of better than 10^{-6}.

The test should be applied to an entire modem design since there are several areas where distortion of the signal may occur. For instance, fixed point quantization in the FFT operation or the performance of the constellation demapper and Viterbi decoder modules could lead to failure of the receiver sensitivity test. It is still necessary to carry out this test to be sure that there is appropriate margin for distortion from the other modules.

The minimum receiver signal-to-noise ratios (SNR) required by the WiMAX standard [5] are given by Table 2.

Table 2. Minimum Receiver SNR Required to Achieve BER 10^{-6}

Modulation	E_b/N_0 (db)	Coding Rate	Receiver SNR (dB)
QPSK	10.5	1/2	9.4
		3/4	11.2
16-QAM	14.5	1/2	16.4
		3/4	18.2
64-QAM	19.0	2/3	22.7
		3/4	24.4

Adjacent Channel Rejection

In normal operating conditions, it is possible that multiple channels will be operating and it is necessary for the digital down converters to be able to attenuate the power that is outside of the desired channel.

The WiMAX standard [6] requires that a receiver operating at 3dB above the receiver sensitivity (outlined in the previous section) must be able to reject interfering signals at the power levels given by Table 3 whilst still achieving an error rate better than 10^{-6}.

Table 3. Adjacent and Nonadjacent Channel Rejection

Modulation/Coding	Adjacent Channel Rejection (dB)	Nonadjacent Channel Rejection (dB)
16-QAM-3/4	11	30
64-QAM-2/3	4	23

Altera DUC & DDC Design Methodology

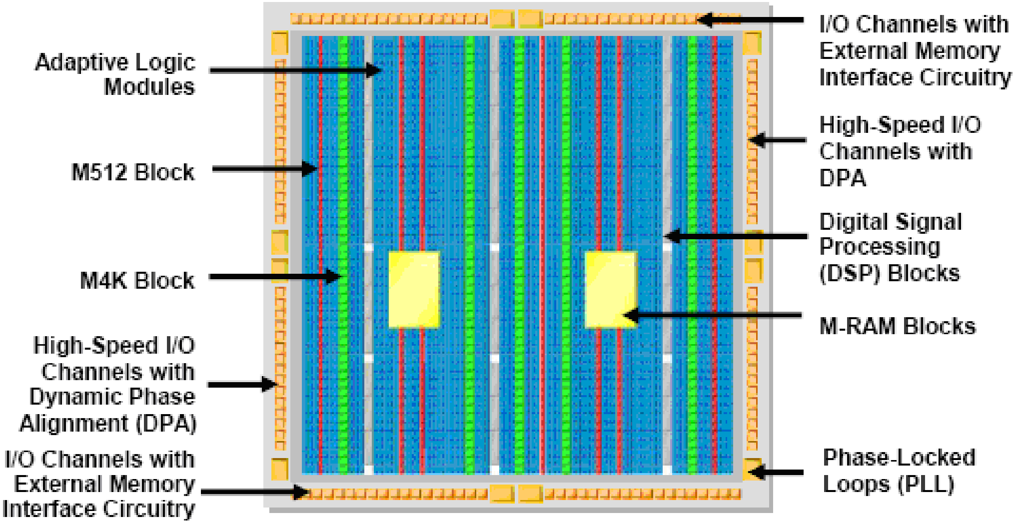
This section outlines the main advantages of the FPGA devices that make them an ideal platform for this type of design. In addition, it explains the tool flow and IP offerings that make it easy to exploit these features to achieve the lowest cost and fastest time to market solution.

Devices

Wireless technology such as WiMAX requires significant hardware processing capability. Some of the Stratix® II floorplan features (Figure 7) that are exploited in this reference design are illustrated as follows:

- The RF card alone requires considerable multiplication operations and Stratix II dedicated DSP blocks are utilized to achieve the high throughput required.
- Quartus® II synthesis exploits the adaptive logic module (ALM) structures to pack more logic into a smaller area which leads to faster performance.
- Dedicated arithmetic functionality is utilized to implement efficient adder trees in the filter structures.
- The parallel logic structure array leads to architectural flexibility and bit width quantization is varied throughout the design to achieve optimum precision.
- Fast internal memory structures are available in three block sizes (M-RAM, M4K, and M512) and are used for the storage required in the filter structures.
- Spectrum licensing regulations and WiMAX specifications are subject to change and so the programmable nature of the FPGA is important for altering the RF card functionality.

Figure 7. Stratix II Floorplan



DSP Builder

DSP Builder is a design entry methodology that enables rapid system design using the familiar MATLAB/Simulink environment. You can rapidly prototype algorithms using the Altera blockset and verify the functionality by building a testbench using other familiar Simulink components. When the design has been verified, DSP Builder provides a flow that generates HDL code for the system that may be synthesized to hardware using the Altera Quartus II software.

This reference design demonstrates how to integrate the Altera IP MegaCore functions and how to achieve a multiple channel design. The control logic required to achieve the design is abstracted away from the designer using custom library components that are provided as bus interfaces in between the various sections of the design.

IP MegaCore Function Portfolio

The Altera MegaCore® functions provide parameterizable hardware implementations of common DSP algorithms that are optimized for the Altera FPGA device families.

If MegaCore functions are utilized, you can explore a larger design space thanks to the architectural flexibility of the MegaCore functions and at the same time reduce development cost since resources are not necessary for development of the DSP function and verification of the implementation.

Many of the DSP IP MegaCore functions feature multiple channel capability, so that you can implement a multiple channel design easily from a single channel system level specification. In addition, it is often possible to achieve greater hardware efficiency by using these features, leading to a lower cost-per-channel for the design.

You can configure all Altera MegaCore functions using a consistent user interface and the generated hardware has a well defined interface that makes it easy to integrate the MegaCore functions using the DSP Builder methodology. In addition, you can integrate the behavior of MegaCore functions into existing bit-accurate system level simulations by utilizing the associated simulation models.

The following sections illustrate some of the features and configurations that are offered by the FIR Compiler and NCO Compiler MegaCore functions and how these can be best exploited by the system architect.

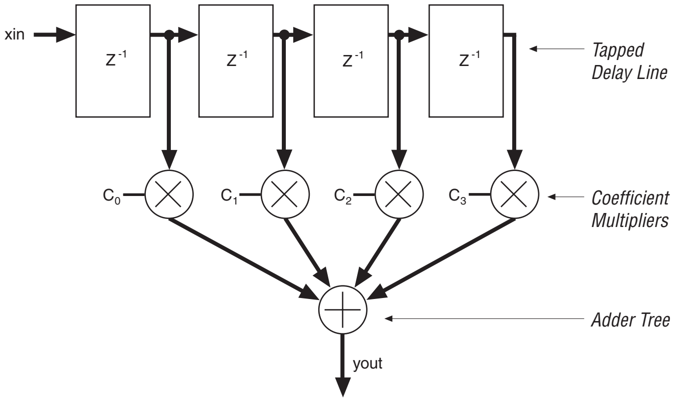
Finite Impulse Response (FIR) Compiler

The FIR Compiler MegaCore function implements hardware for single rate, interpolating and decimating filters. You can use the coefficient generator to achieve the desired frequency response. Alternatively, filter coefficients can be generated using a third party tool such as MATLAB and imported via a text file.

Filter Architectures

The simplest description of a FIR filter is a tapped delay line. There are many different filter architectures that can be used to achieve this. Each trades off a combination of performance and throughput, logic area, dedicated multiplier utilization, and memory usage.

Figure 8. Tapped Delay Line



In general, the highest frequency of operation can be achieved using the fully parallel architecture at the expense of the highest logic utilization. However, the multicycle variable architecture can achieve a more balanced implementation that makes use of dedicated multipliers, internal memory and logic.

This reference design exploits the balanced multicycle variable (MCV) architecture with the aim to fit the DUC/DDC designs into the smallest device possible.

Parameterization and Implementation

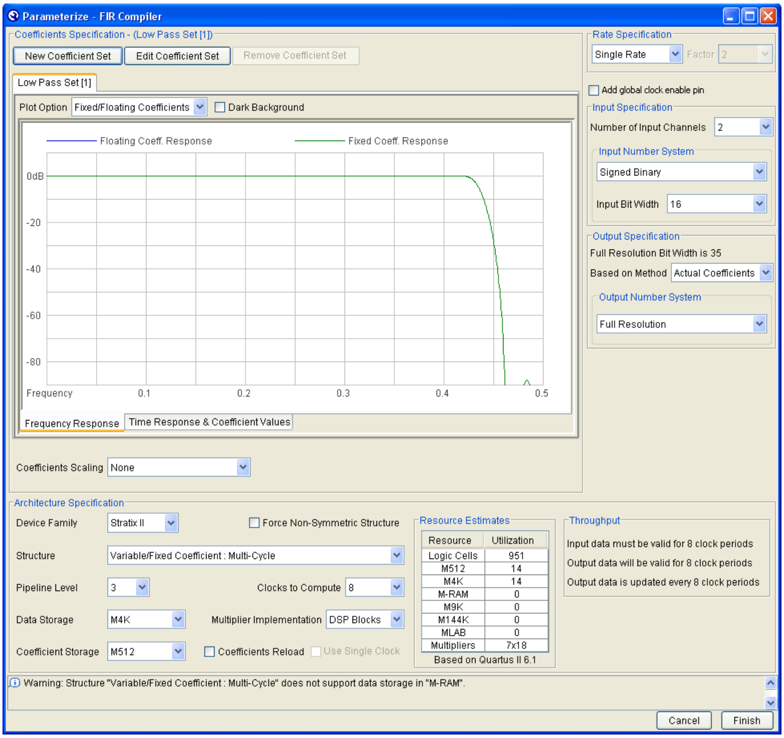
You must select the throughput required, with respect to the clock frequency chosen. The required throughput is a function of the data rate, the number of channels and the clock rate.

As a rule of thumb, the larger the number of clock cycles per input sample, the greater the degree of resource sharing within the filter. The MegaCore function takes care of the complex scheduling required to achieve the most efficient hardware architecture.

Polyphase decomposition is exploited in interpolation and decimation filters to achieve a reduction in hardware resources since zero-stuffed data does not need to be computed when interpolating and the discarded data when decimating also does not require any filter computation.

Pipelining options are available. There are three levels, and these apply register stages to the accumulator carry chains. Although Stratix II devices have fast dedicated carry chains, large adders can dominate the critical path because of the large logic delay through the adders. In general, the pipeline level of 2 is sufficient for most filters, but high throughput filters sometimes require the highest pipeline level. As a rule of thumb, more pipelining leads to additional performance but at the expense of greater latency and logic utilization.

Figure 9. FIR Compiler Parameterization Interface



Plot Option: Fixed/Floating Coefficients

☐ Dark Background

Coefficients Scaling: None

Single Rate — Factor: 2

☐ Add global clock enable pin

Number of Input Channels: 2

Signed Binary

Input Bit Width: 16

Full Resolution Bit Width is 35

Based on Method: Actual Coefficients

Full Resolution

Device Family: Stratix II

☐ Force Non-Symmetric Structure

Structure: Variable/Fixed Coefficient : Multi-Cycle

Pipeline Level: 3

Clocks to Compute: 8

Data Storage: M4K

Multiplier Implementation: DSP Blocks

Coefficient Storage: M512

☐ Coefficients Reload ☐ Use Single Clock

Resource	Utilization
Logic Cells	951
M512	14
M4K	14
M-RAM	0
M9K	0
M144K	0
MLAB	0
Multipliers	7x18

Based on Quartus II 6.1

Input data must be valid for 8 clock periods

Output data will be valid for 8 clock periods

Output data is updated every 8 clock periods

Warning: Structure "Variable/Fixed Coefficient : Multi-Cycle" does not support data storage in "M-RAM".

Finally, you can adjust the word length quantization of the internal buses within the filter. Coefficients with larger bus widths lead to a filter response that is closer to the ideal response, but at the expense of higher memory and logic utilization. Output truncation leads to additional quantization noise at the output and the danger of overflow. In the reference design, the coefficients are set to 18 bits, and the output precision is set to maximum.

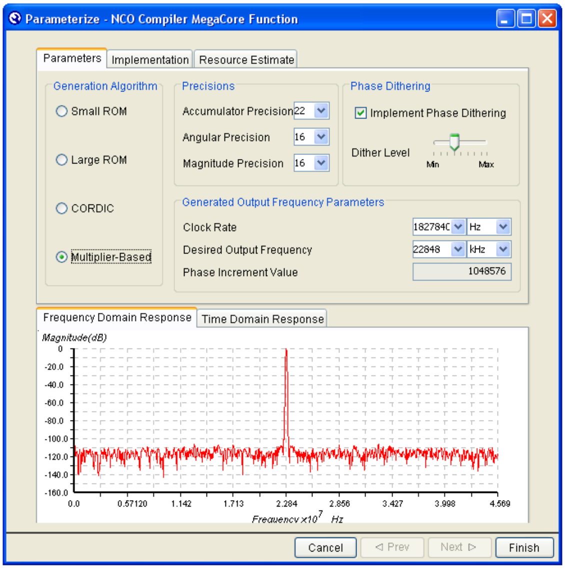
Numerically Controlled Oscillator (NCO) Compiler

The Altera NCO Compiler generates numerically controlled oscillators customized for Altera devices. This particular design uses the oscillators as quadrature carrier generators in the I-Q Mixer stage to modulate the I-Q channels onto orthogonal carriers.

Various NCO architectures may be parameterized using the IP Toolbench interface; such as ROM based, CORDIC-based, and multiplier-based. Each trades off spurious-free dynamic range and resource utilization (memory, multipliers or logic). You can visualize the frequency domain response of the parameterized NCO using IP Toolbench itself.

The multiplier architecture is chosen as it offers a good balance between logic utilization and dedicated memory/multiplier usage.

Figure 10. NCO Compiler Parameterization User Interface



Parameterize - NCO Compiler MegaCore Function

Generation Algorithm
○ Small ROM
○ Large ROM
○ CORDIC
● Multiplier-Based

Precisions
Accumulator Precision 22
Angular Precision 16
Magnitude Precision 16

Phase Dithering
☑ Implement Phase Dithering
Dither Level

Generated Output Frequency Parameters
Clock Rate 182784C Hz
Desired Output Frequency 22848 kHz
Phase Increment Value 1048576

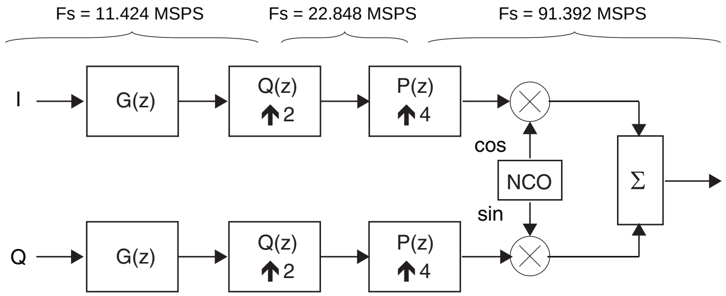
Reference Design Tutorial

Multistage Partitioning

Recall from "Multirate Filter Design" on page 8 that you can reduce the total required computational complexity by dividing the sampling rate conversion into a cascade of stages. For this application, a total rate change of 8 is required and this is decomposed into two stages; an interpolate by two stage, and an interpolate by four stage.

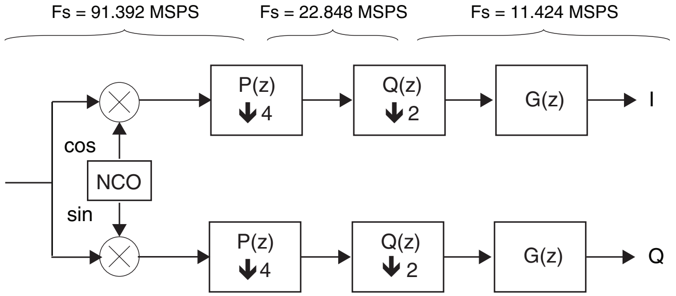
Figure 11 illustrates this architecture for the DUC.

Figure 11. Digital Up Converter Multistage Partitioning



Similarly, the DUC partitioning is decomposed into a decimate by two stage, and a decimate by four stage as shown in Figure 12.

Figure 12. Digital Down Converter Multistage Partitioning



The channel filter *G*(*z*) is used to attenuate spectral energy outside of the spectral mask. This filter requires the sharpest roll off and so has the most taps. Note that the spectral mask is exceeded by around 1dB at the start of the transition band. This is acceptable because the OFDMA carriers in this region are guard carriers; that is, the transmitter applies no energy to these frequencies. The output spectrum is therefore compliant with the spectral mask.

Filter *Q*(*z*) is associated with the rate change of stage 2. This filter attenuates spectral images of the baseband data in the DUC and applies band limiting in the DDC. A wider transition band is possible because the spectral gaps introduced by the channel filter may be exploited and subsequently only 79 taps are required.

Filter *P*(*z*) attenuates further spectral images and band limiting associated with the rate change of stage 4. Just like filter *Q*(*z*), you can exploit a wider transition band so only 39 taps are required to satisfy the attenuation requirements.

The relaxation of the transition band requirements for a cascaded rate change is shown in Figure 13. The filters are designed so that the stop band starts at the point that the spectral images of the lower sampling rate filters start.

Figure 13. Relaxed Transition Band Requirements

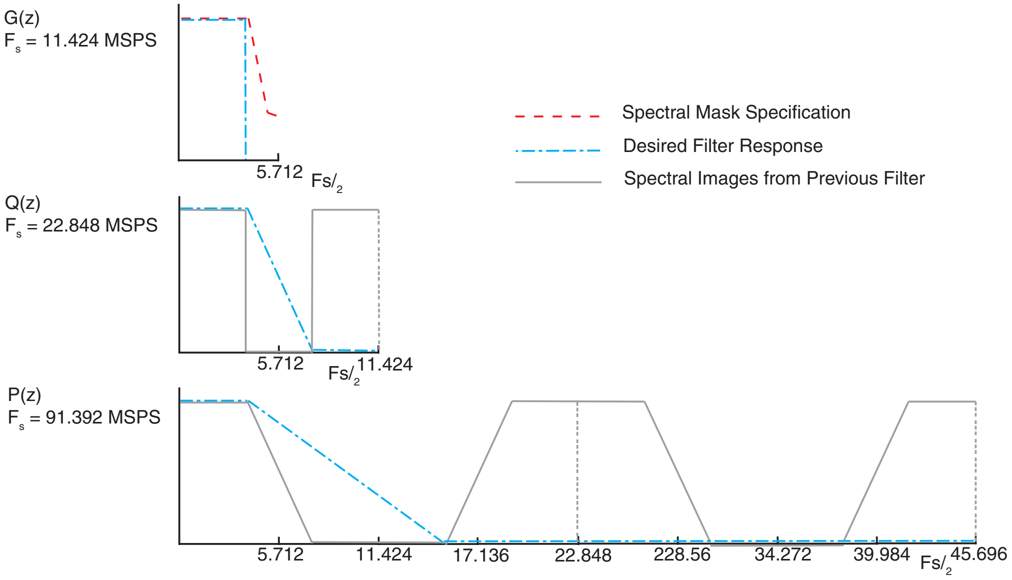


Table 4 summarizes the filters utilized in the DUC and DDC designs.

Table 4. Multistage Partitioning and Filter Characteristics

Filter	Number of Taps	Sample Frequency (MSPS)	Rate Change Factor L
G(z)	111	11.424	1
Q(z)	79	22.848	2
P(z)	39	91.392	4

Fixed Point Filter Design and Performance

Each of the filter stages is designed utilizing floating point arithmetic and the MATLAB filter design toolkit. However, only 18 bits of precision are used to represent the filter coefficients. This has to be taken into account when designing the filters because there is an error between the ideal (floating point arithmetic) frequency response and the quantized (fixed point arithmetic) filter response. In general, the main characteristic that is affected by quantization of the coefficients is the minimum stop band attenuation. Since the filters are required to have a minimum stop band attenuation of -90dB, the filters are designed in floating point with an additional margin. The maximum pass band ripple of the fixed point filters is 0.0416dB and the minimum stop band attenuation is 92.9dB.

Figure 14. Channel Filter G(z)

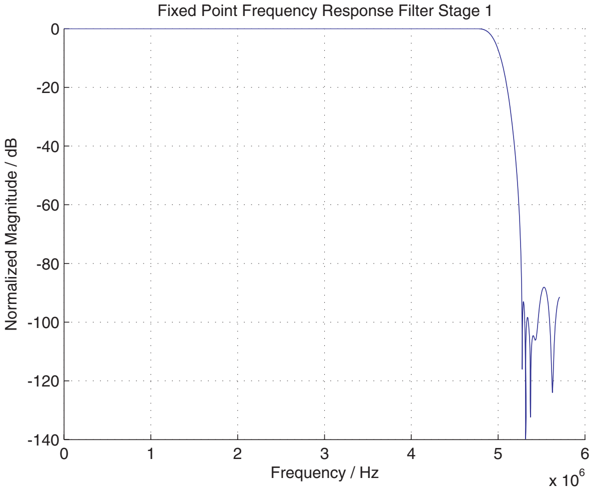


Figure 15. Q(z)

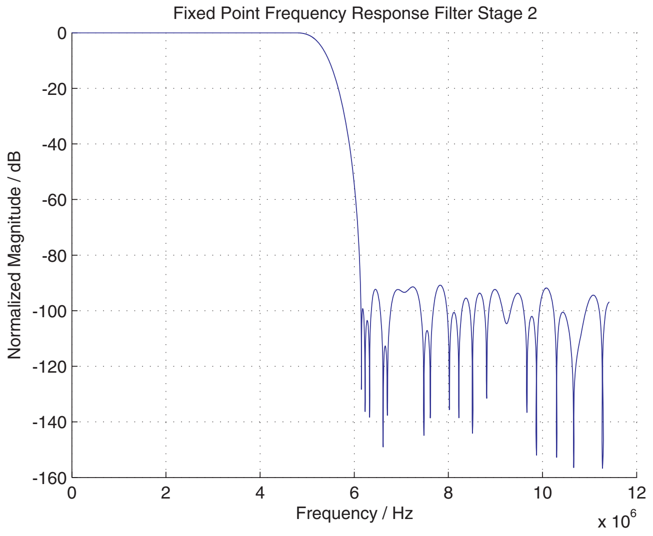


Figure 16. P(z)

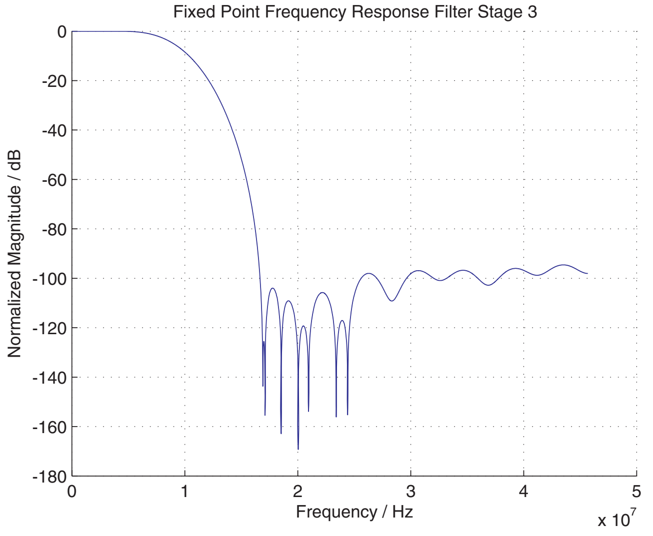


Figure 17. Cascaded Filter Response

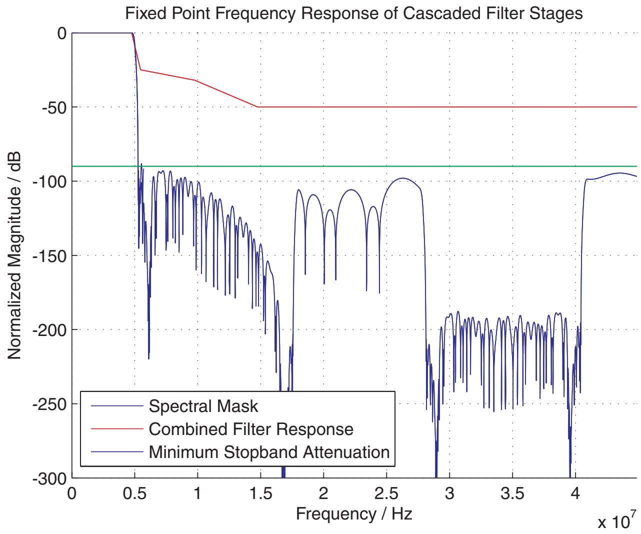
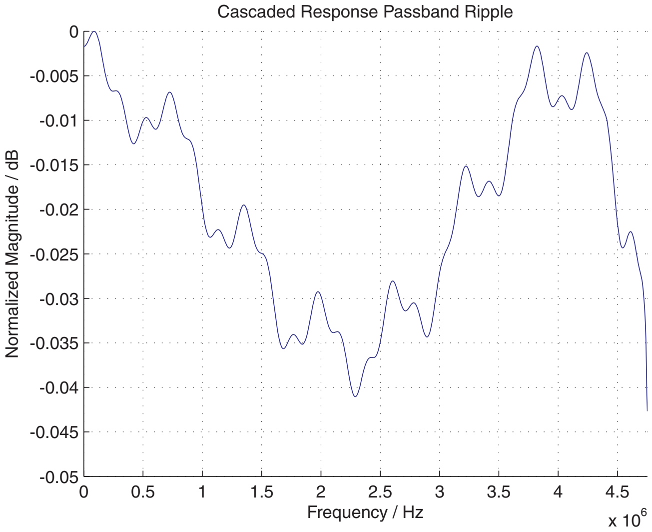


Figure 18. Maximum Pass Band Ripple



Efficient Hardware Implementation

The simplest implementation of a DUC and DDC would be to implement an architecture similar to those shown in Figures 11 and 12 respectively. This architecture requires a separate filter chain for both the I and Q channels and the required clock frequency would be 91.392MHz.

Since Altera FPGAs support significantly higher clock frequencies than this, the first stage of optimization would be to run the design at a higher clock frequency so that it would be possible for the I and Q channels to share the same filter resources. This is referred to as time division multiplexing (TDM) and leads to a reduction in multiplier utilization and coefficient memory storage. To achieve the same throughput with this single filter chain, the clock frequency required would be 182.784 MHz and the hardware architectures are shown in Figures 19 and 20.

Figure 19. Single Channel IQ Time Division Multiplexed DUC

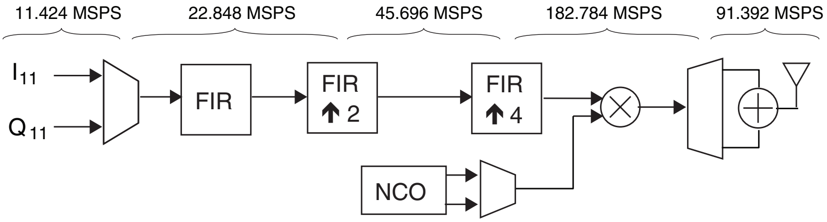
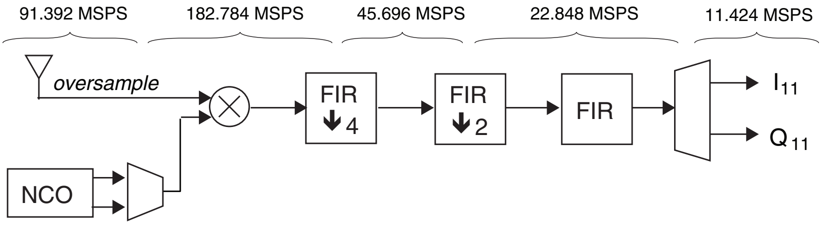


Figure 20. Single Channel IQ Time Division Multiplexed DDC



The FIR Compiler and NCO Compiler MegaCore functions provide multiple channel parameterization, and so the difficulty of realizing a hardware filter chain capable of processing multiple channels is simplified for the user. In addition, this reference design illustrates how to multiplex multiple channels onto a single bus and how to condition the data so that it is compatible with the input protocol of the FIR Compiler MegaCore function IP.

A common requirement for a basestation deployment is for two transmit antennae and four receive antennae. Each transmit antenna requires a DUC and each receive antenna requires a DDC on the RF card. To increase the hardware efficiency further, it is necessary to run as many channels as possible through each of the filters. Figures 21 and 22 illustrate suitable hardware architectures for this type of basestation configuration.

Figure 21. Two Antenna DUC Design

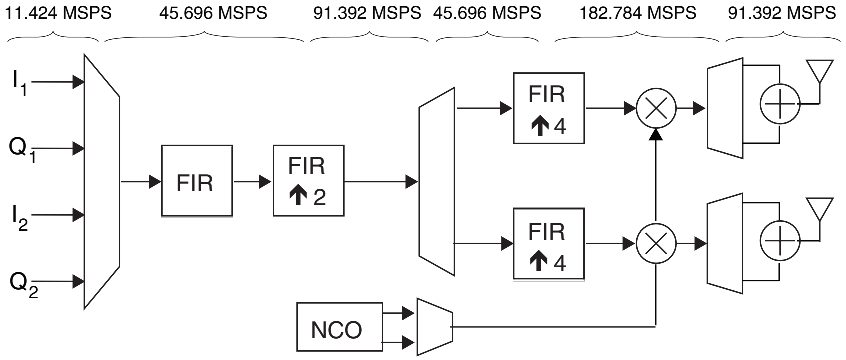
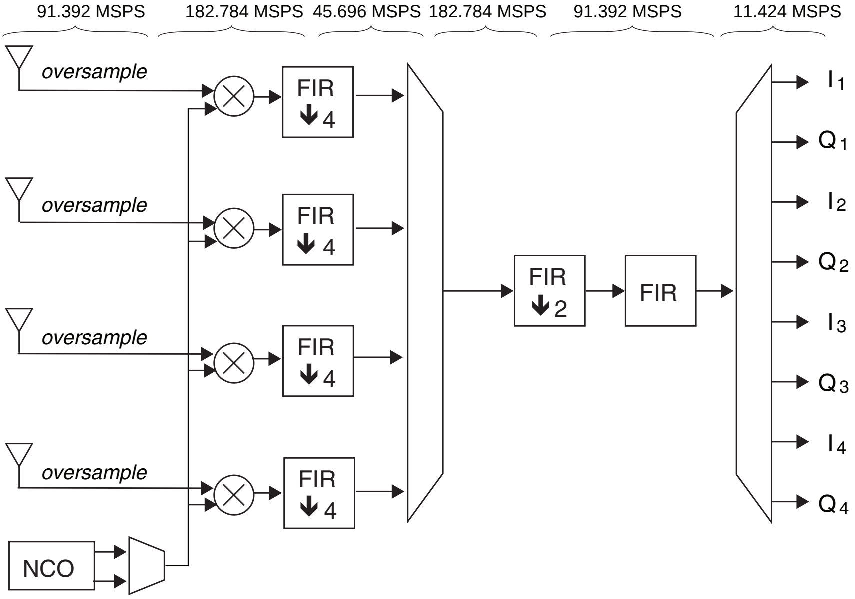


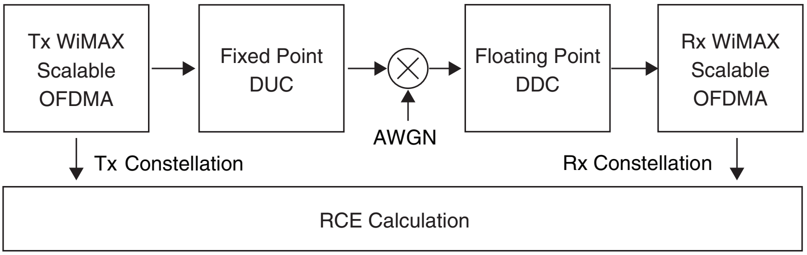
Figure 22. Four Antenna DDC Design



DUC Relative Constellation Error Measurements

Test Methodology

Figure 23. RCE Test Methodology Block Diagram



The test methodology shown in Figure 23 is described by:

1. A WiMAX Scalable OFDMA physical layer model is utilized to generate input stimulus for the DUC:
    a. Generate constellation symbols.
    b. Allocate constellation symbols and boosted binary phase shift keying (BPSK) pilots to the OFDMA subcarriers according to the DL_FUSC sub-channelization scheme
    c. Perform inverse fast Fourier transform (IFFT) and guard interval insertion
2. The resulting time domain OFDMA symbols are passed through the fixed point digital up converter. These symbols are scaled assuming perfect automatic gain control (AGC).
3. An appropriate amount of additive white gaussian noise (AWGN) (Tx_{SNR}) is added to the up converted data stream. This is calculated as the sum of the assumed receiver signal-to-noise ratios given by 8.4.13.1 and the assumption that all measurement errors are taken 10dB less than the required level. In addition, the specification assumes a 5dB implementation loss and 7dB Noise figure.
4. The data is passed through a floating point digital down converter.

5. A WiMAX Scalable OFDMA simulation is utilized to:
    a. Perform synchronization, guard interval removal and FFT.
    b. Recovery of constellation symbols from the OFDMA subcarriers according to the DL_FUSC sub-channelization scheme
6. The relative constellation error was calculated by the equation shown in "Relative Constellation Error (RCE)" on page 10.

Results

The measured relative constellation error of the DUC for the modes specified are given in Table 1.

Table 5. Measured Relative Constellation Error

Burst Type	Required RCE (dB)	Measured RCE (dB)
QPSK $^1/_2$	-16.4	-40.18
QPSK $^3/_4$	-18.2	-41.57
16QAM $^1/_2$	-23.4	-48.26
16QAM $^3/_4$	-25.2	-49.00
64QAM $^2/_3$	-29.7	-53.66
64QAM $^3/_4$	-31.4	-55.29

Notes for Table 1:

(1) The burst type is expressed in terms of quadrature phase shift keying (QPSK) or quadrature amplitude modulation (QAM).

DDC Receiver Sensitivity and Adjacent Channel Rejection

Test Methodology

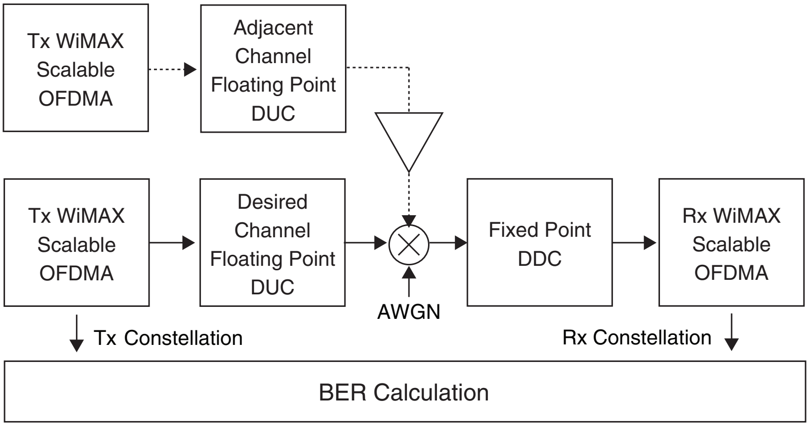
The test harness outlined in Figure 24 on page 27 was set up and using this model it was possible to test both the receiver sensitivity and also the adjacent channel rejection.

A set of OFDMA symbols was generated by a physical layer model and these were processed by an ideal floating point DUC. The required amount of noise was added, before scaling the data such that the dynamic range was maximized for input into the fixed point DDC.

The received constellation points were recovered by the receiver physical layer model, and the bit error rate was calculated. In this case, the adjacent channel shown by the upper signal path was disabled.

To test the adjacent channel rejection, the upper signal path was enabled, and an appropriate gain applied to the signal. This was then combined with the signal from the desired channel before being passed through the fixed point DDC and physical layer model.

Figure 24. Receiver Sensitivity and Adjacent Channel Rejection Test Methodology



Results

The physical layer model was configured to recover the bit stream from the received constellation using hard decision decoding and the uncoded bit error rate was measured.

This represents the worst possible performance of the physical layer (that would not be implemented in a practical receiver) and this approach was used to ensure that the performance of the DDC was satisfactory.

Figure 6 shows the receiver sensitivity measurements and that the performance exceeded the specified BER of 10^{-6} since no error events were observed over the total number of bits shown.

Table 6. Receiver Sensitivity Results

Burst Type	Total Number of Bits	Error Events	Bit Error Rate
QPSK $^1/_2$	10.752×10^6	0	$<10^{-6}$
QPSK $^3/_4$	10.752×10^6	0	$<10^{-6}$
16QAM $^1/_2$	10.752×10^6	0	$<10^{-6}$
16QAM $^3/_4$	10.752×10^6	0	$<10^{-6}$
64QAM $^2/_3$	9.216×10^6	0	$<10^{-6}$
64QAM $^3/_4$	9.216×10^6	0	$<10^{-6}$

The adjacent channel rejection measurements are shown by Figure 7 and the BER is better than the requirement when an adjacent channel interferer is present.

Table 7. Adjacent Channel Rejection Results

Burst Type	Total Number of Bits	Error Events	Bit Error Rate
16QAM $^3/_4$	10.752×10^6	0	$<10^{-6}$
64QAM $^2/_3$	9.216×10^6	0	$<10^{-6}$

Getting Started

This section describes the system requirements, installation and other information about using the WiMAX IF Modem reference design.

System Requirements

Mandatory

- MATLAB Version 7.2 (R2006a)
- Simulink Version 6.4 (R2006a)
- Quartus II Version 6.1
- DSP Builder Version 6.1
- FIR Compiler Version 6.1
- NCO Compiler Version 6.1

Recommended

- MATLAB Signal Processing Toolbox Version 6.3 (R2006a)
- MATLAB Signal Processing Blockset Version 6.5 (R2006a)

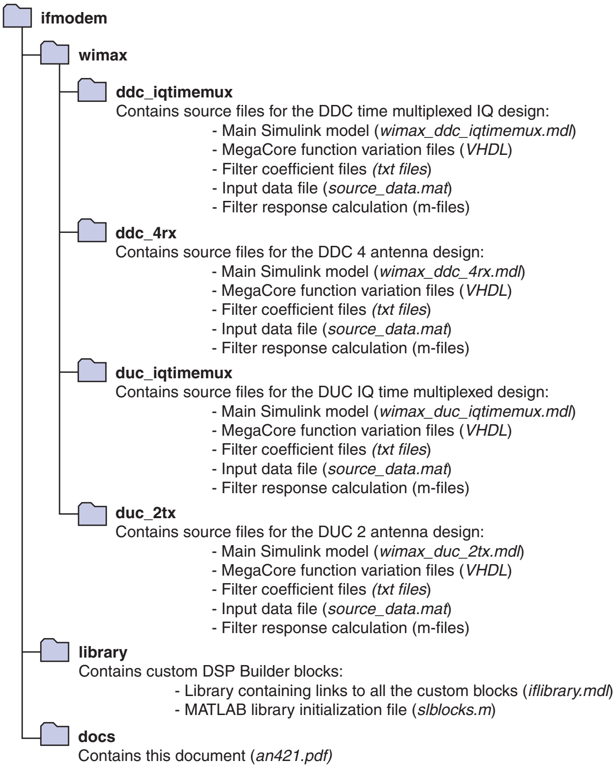
Installing the Reference Design

To install the reference design, run the **an421-v6.1.exe** file to launch Installshield and follow the installation instructions.

The reference design is installed by default in the directory **c:\altera\reference_designs** but you can change the default directory during the installation.

Figure 25 shows the directory structure after installation.

Figure 25. Directory Structure



ifmodem
- **wimax**
  - **ddc_iqtimemux**
    Contains source files for the DDC time multiplexed IQ design:
    - Main Simulink model (*wimax_ddc_iqtimemux.mdl*)
    - MegaCore function variation files (*VHDL*)
    - Filter coefficient files *(txt files*)
    - Input data file (*source_data.mat*)
    - Filter response calculation (m-files)
  - **ddc_4rx**
    Contains source files for the DDC 4 antenna design:
    - Main Simulink model (*wimax_ddc_4rx.mdl*)
    - MegaCore function variation files (*VHDL*)
    - Filter coefficient files *(txt files*)
    - Input data file (*source_data.mat*)
    - Filter response calculation (m-files)
  - **duc_iqtimemux**
    Contains source files for the DUC IQ time multiplexed design:
    - Main Simulink model (*wimax_duc_iqtimemux.mdl*)
    - MegaCore function variation files (*VHDL*)
    - Filter coefficient files *(txt files*)
    - Input data file (*source_data.mat*)
    - Filter response calculation (m-files)
  - **duc_2tx**
    Contains source files for the DUC 2 antenna design:
    - Main Simulink model (*wimax_duc_2tx.mdl*)
    - MegaCore function variation files (*VHDL*)
    - Filter coefficient files *(txt files*)
    - Input data file (*source_data.mat*)
    - Filter response calculation (m-files)
- **library**
  Contains custom DSP Builder blocks:
  - Library containing links to all the custom blocks (*iflibrary.mdl*)
  - MATLAB library initialization file (*slblocks.m*)
- **docs**
  Contains this document (*an421.pdf)*

Opening the Reference Design

You can open the reference design by performing the following steps:

1. Open MATLAB.

2. Add the custom DSP Builder blocks to the Simulink library browser by selecting the **Set Path** command from the File menu and adding `<installation directory>\library` to the path. Then save the path and close the Set Path dialog box.

3. Type Simulink in the MATLAB command window to open the Simulink library browser and check that the **Altera IF Modem** folder is available.

4. Open the required DSP Builder model: **wimax_ddc_iqtimemux.mdl**, **wimax_ddc_4rx.mdl**, **wimax_duc_iqtimemux.mdl**, or **wimax_duc_2tx.mdl**.

5. Type `refresh_megacore` in the MATLAB command window to regenerate the simulation models and configuration files for the MegaCore functions.

Simulation and Synthesis

If input data is not available from the MATLAB workspace when the design is simulated, the model will automatically load (using the `initFcn` found in the model properties) some data from the provided **source_data.mat** file.

For more specific information on simulation and synthesis using DSP Builder, refer to the *DSP Builder User Guide*.

Synthesis Results

The results shown in Table 8 were obtained when the designs were synthesized using the Altera Quartus II 6.1 software targeting the EP2S60F1020C4 device.

Table 8. Synthesis Results

Combinational ALUTs	Logic Registers	Memory			Multipliers 18×18	F_{max} MHz
		M512	M4K	MRAM		
DUC Time Multiplexed IQ Design						
1,387	2,949	24	31	0	30	269
DUC 2 Antenna Design						
1,874	4,111	26	59	0	58	258
DDC Time Multiplexed IQ Design						
1,509	3,181	30	24	0	25	272
DDC 4 Antenna Design						
5,702	11,452	48	73	0	74	208

Conclusion

WiMAX DUC and DDC designs require significant amounts of computation and the architecture of the Altera devices make them an ideal platform for this type of DSP design. This document highlights the system design challenges associated with the implementation of a WiMAX Digital up and down converter module. In addition, it has addressed these issues and identifies how it is easy to overcome them by utilizing Altera intellectual property and tool methodology. Finally, the hardware efficiency is further optimized by applying the system level specification to a multiple channel design.

References

1. The draft *IEEE Standard for Local and Metropolitan Area Networks, Part 16: Air Interface for Fixed Broadband Wireless Access Systems*, IEEE P802.16-REVd/D5-2004, May 2004
2. *Section 8.5.2* of the draft IEEE standard
3. Sanjit K. Mitra, *Digital Signal Processing - A Computer-Based Approach*, McGraw-Hill Second Edition, 2001, p680
4. Section 8.4.12.3 of the draft IEEE standard
5. Section 8.4.13.1 of the draft IEEE standard
6. Section 8.4.13.2 of the draft IEEE standard

Revision History

Table 9 shows the revision history for the *AN-421:Accelerating WiMAX DUC & DDC System Designs* application note.

Table 9. AN-421 Revision History

Version	Date	Errata Summary
2.1	January 2006	Corrected performance figures.
2.0	December 2006	Updated for use with version 6.1 of the Quartus II software.
1.0	May 2006	First release of this application note.

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