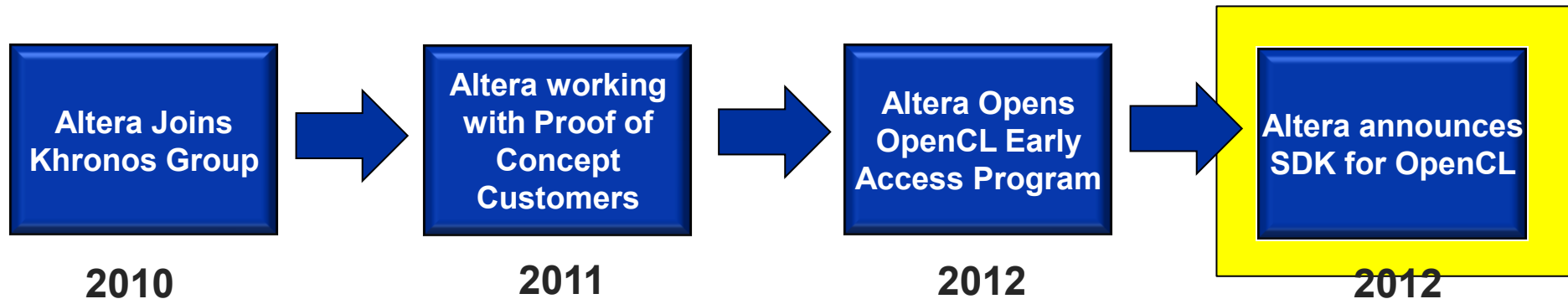# Altera SDK for OpenCL

A novel SDK that opens up the world
of FPGAs to today's developers

Altera Technology Roadshow 2013

Today's News

- Altera today announces its SDK for OpenCL

Altera Joins Khronos Group	→	Altera working with Proof of Concept Customers	→	Altera Opens OpenCL Early Access Program	→	Altera announces SDK for OpenCL
2010		**2011**		**2012**		**2012**

- OpenCL allows software developers to boost system performance by using an FPGA's massively parallel architecture

- Increases designer productivity by raising the level of design abstraction

2

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Performance Challenge

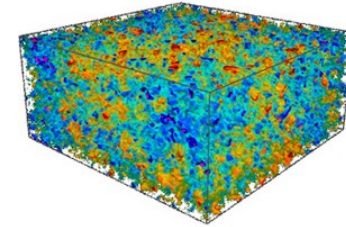**Multimedia**
- HD Video Processing
- Image processing

Medical
- Medical imaging
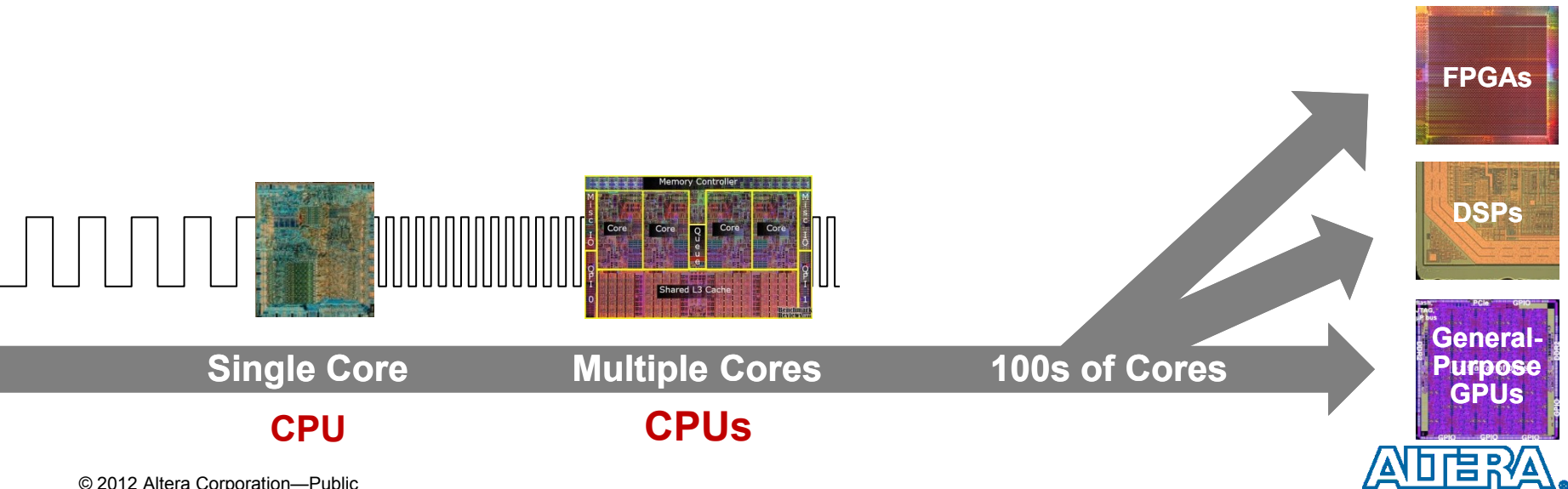- Bio informatics

Military
- Radar image processing
- Persistent surveillance

High-Performance Computing
- Financial Modeling
- Big data analytics
- Scientific computing

Performance Challenges

Single Core

CPU

Multiple Cores

CPUs

100s of Cores

FPGAs

DSPs

General-Purpose GPUs

3

Modern Altera FPGA: Massively Parallel

- \>1M logic elements

- \>3.9 billion transistors

- \>50 Mb of integrated memory

- Variable precision floating-point DSP blocks

- High-speed serial transceivers

4

Altera Is Driving Silicon Convergence
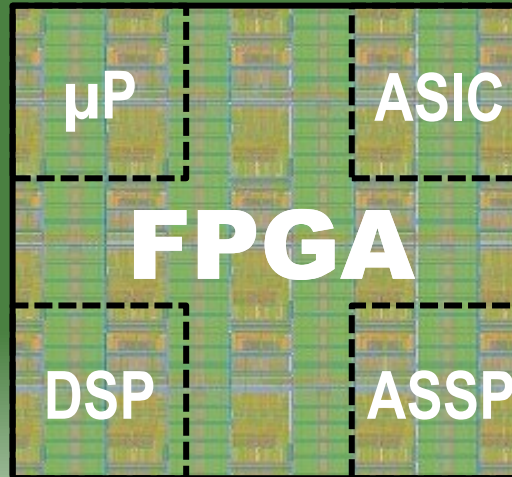
General Processors	FPGAs	Application-Specific

FPGAs

Need for **Efficiency** »

FPGA Combines the **Best of All Four + FPGA**

« Need for **Flexibility**

µP   DSP

µP   ASIC

FPGA

DSP   ASSP

ASIC   ASSP

General Processors
- Software programmable
- Great flexibility
- Poor power efficiency

FPGAs
- Hardware *and* software programmable
- *Great* flexibility
- *Good* power efficiency

= **Microprocessor**
+ **DSP**
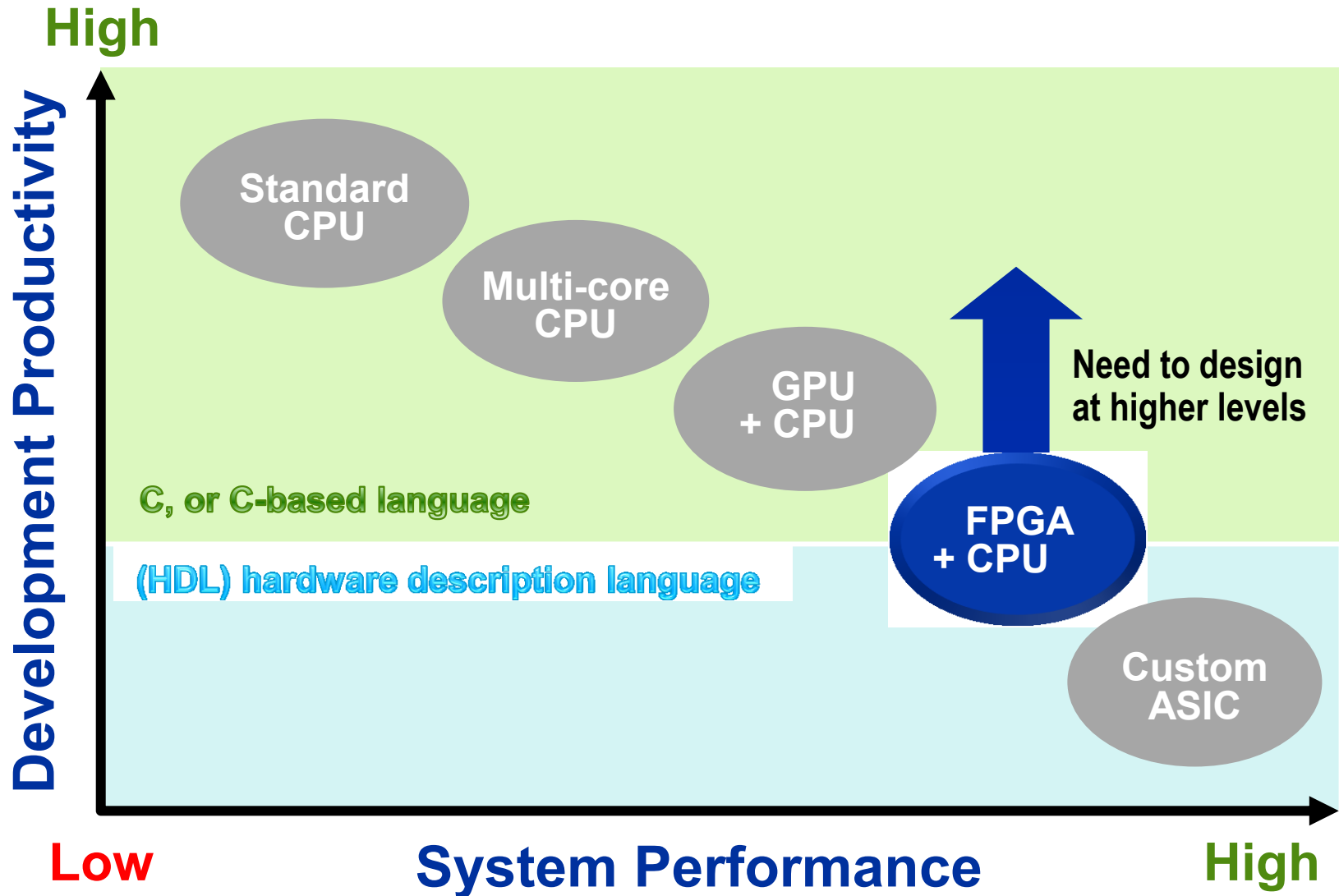+ **Application-Specific IP**
+ **Programmable Fabric**

Application-Specific
- Not programmable, hard wired
- Inflexible
- Great power efficiency
- Many contain embedded processors

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Improving FPGA Development Productivity

Development Productivity (vertical axis, Low to High)

System Performance (horizontal axis, Low to High)

- Standard CPU
- Multi-core CPU
- GPU + CPU
- FPGA + CPU
- Custom ASIC

Need to design at higher levels

C, or C-based language

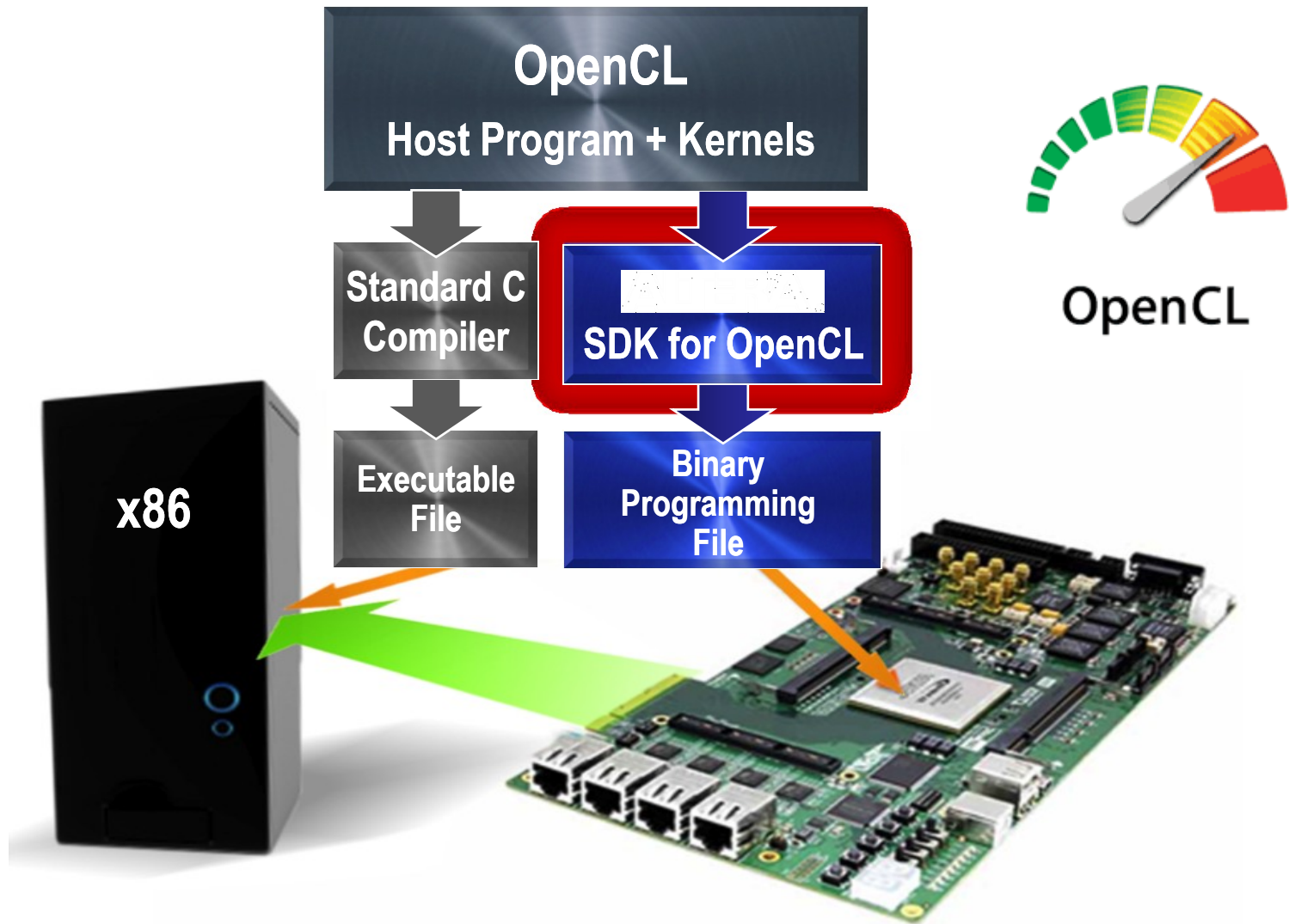(HDL) hardware description language

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OpenCL for Heterogeneous Solutions

- ## C-based language with extensions:
  - Standard C Language
  - Altera OpenCL C extensions (adds parallelism to C)
  - API (Open standard for different devices)

OpenCL

- ## Programming model supports parallelism in heterogeneous systems
  - CPU/GPU/FPGA


```
main(…)
{
    for( … )
    {

}
```

OpenCL

Host Program + Kernels

Compiler

Processor

Hardware Accelerator
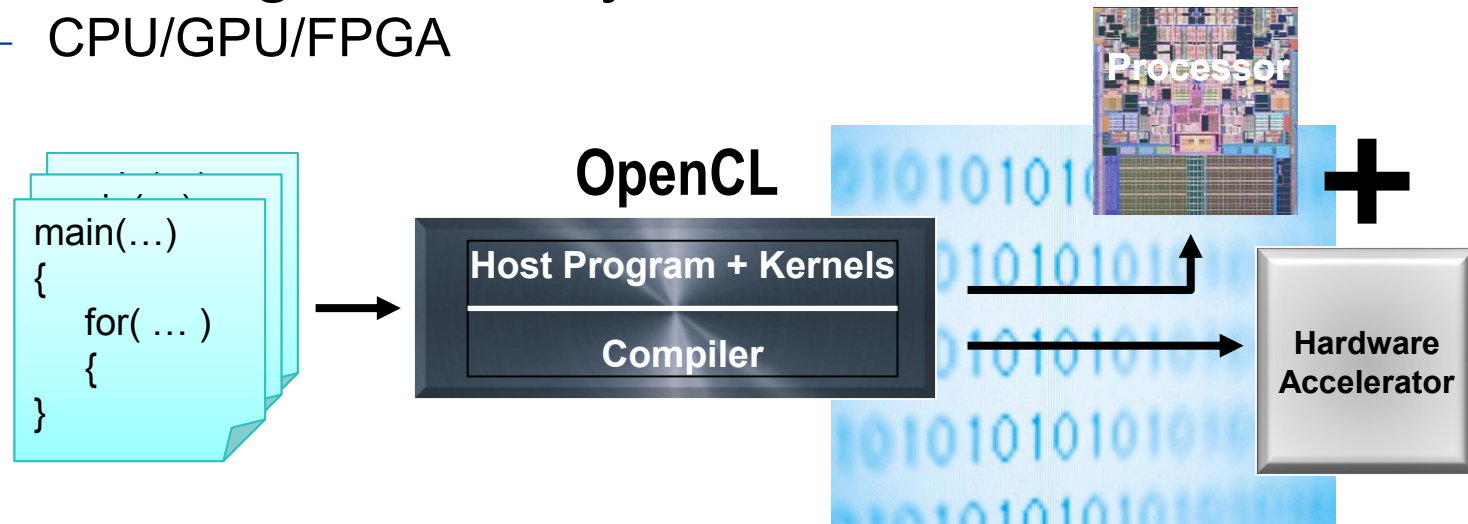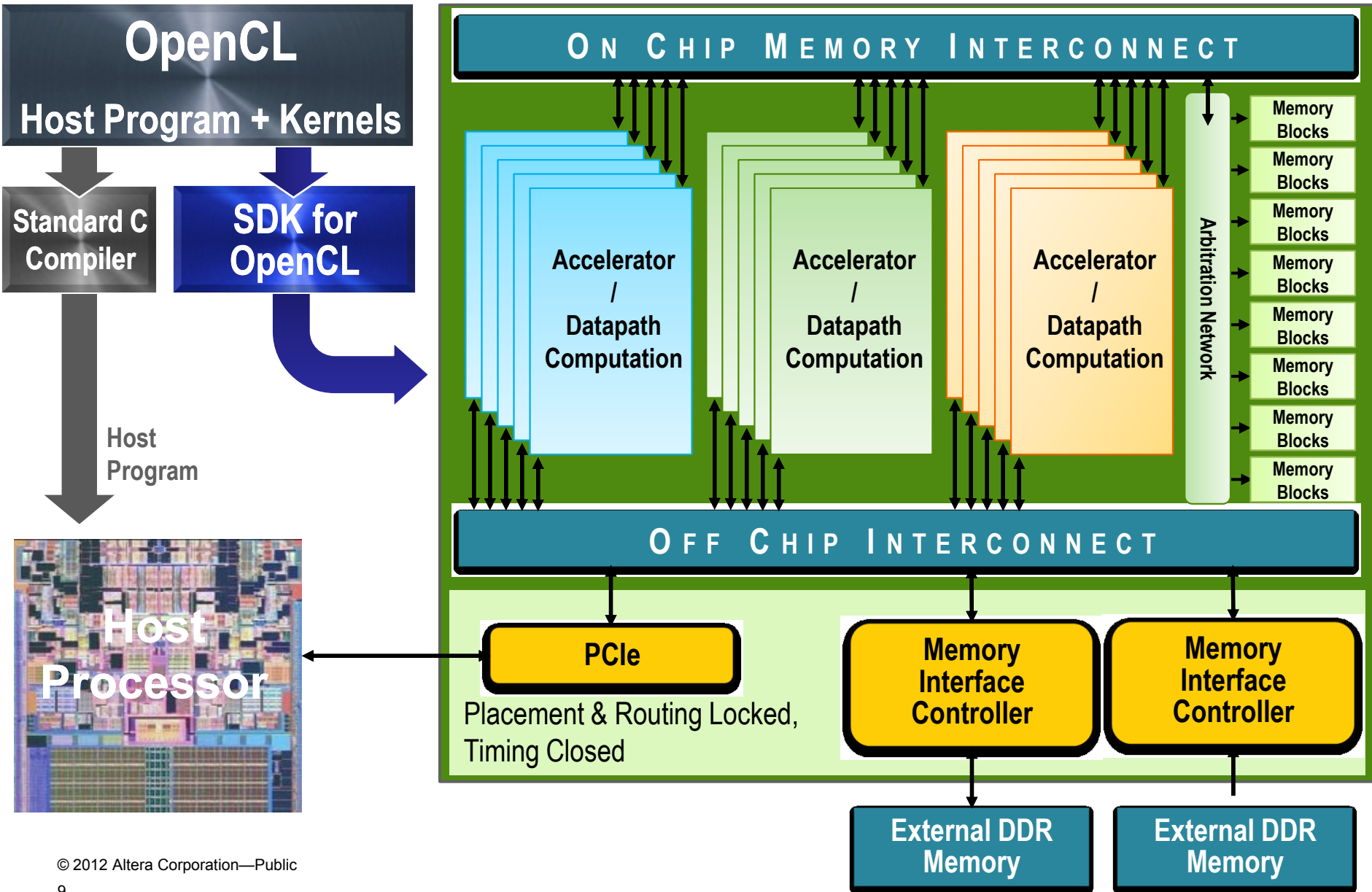
Introducing Altera SDK for OpenCL
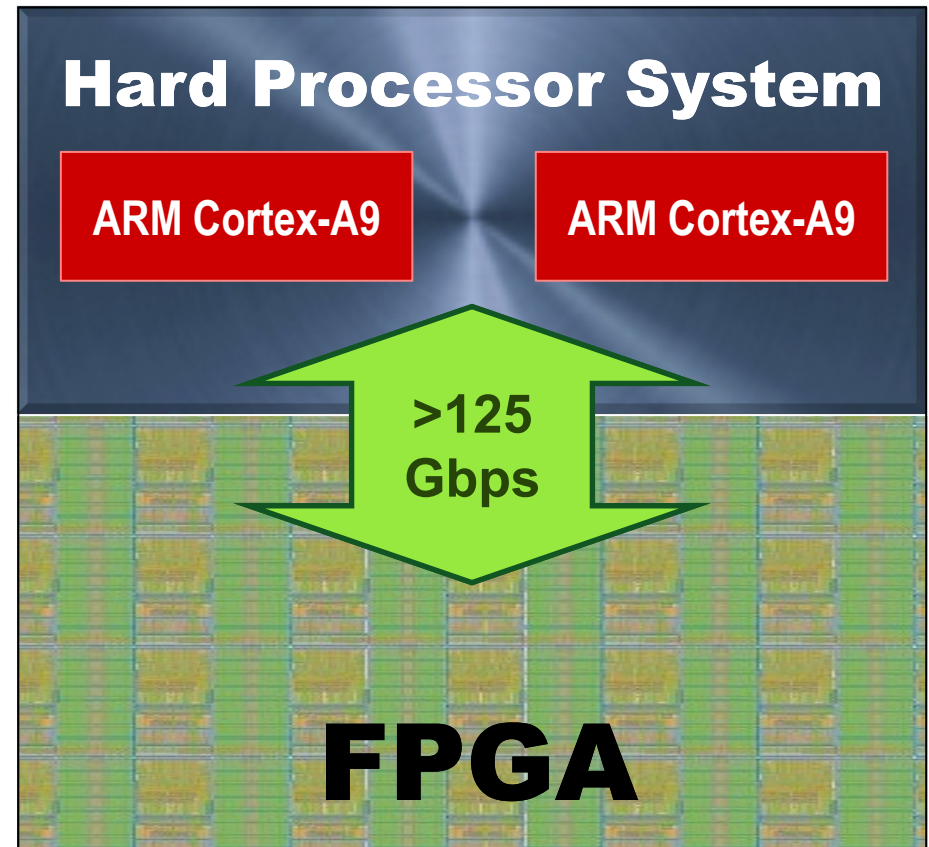
OpenCL Implementation on Altera FPGAs

Accelerating Performance with SoC FPGAs

Single-Chip OpenCL Solution:

- SoC = ARM + FPGA

Integration Enables:

- Higher bandwidth and lower latency between FPGA and processor
  - >125Gbps Interconnect
- Processor integration reduces system cost

Hard Processor System

ARM Cortex-A9   ARM Cortex-A9

>125 Gbps

FPGA

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# OpenCL Example #1 – *Faster Time-to-Market*

Video Camera Requiring Intense Video Processing

- Proprietary video codec algorithms
- Captures frames with different exposure levels → retains highlight and shadow details

Let Customer Implement Code In An FPGA In <1 Week

- Port C-code to OpenCL to FPGA implementation
- C → HDL typically requires 3-6 months

Saved Months of Development
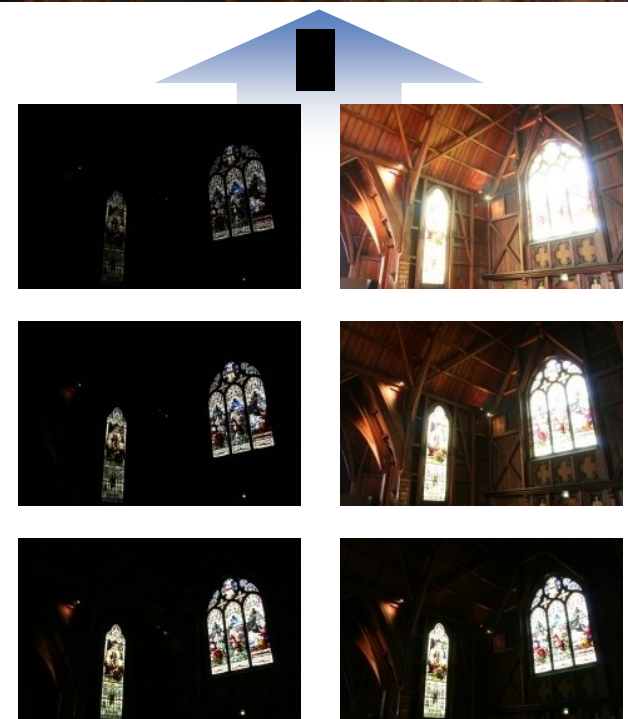
OpenCL Example #2 – *Higher Performance*

Financial Marketplace Monte-Carlo Black Scholes Simulations

- Calculate the value of trading options w/ multiple sources of uncertainty
- FPGA delivers higher performance at a fraction of the power

OpenCL MCBS	Quad-core µP	Comparable GPU	Stratix IV FPGA
Number of Cores	8	448	N/A
Simulations per Second	240M	2100M	
Power (Watts)	130W	215W	21W
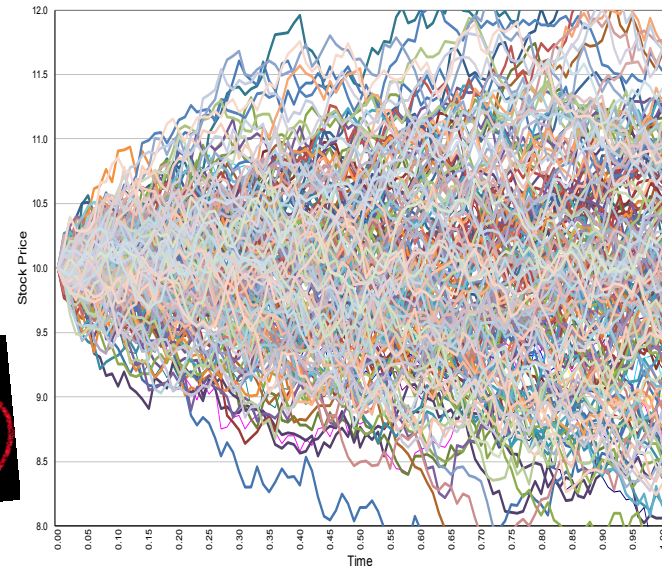
## *>9X Higher Performance vs CPU Alone*

OpenCL Example #3 – *Power Efficiency*

Documenting Search / Filtering Algorithm

- Review incoming stream (documents) and return best match
- E.g. Monitors news feeds and recommends others
- **Power savings = Cost savings (huge issue for server farms)**

Platform	Quad-core µP	Comparable GPU	Stratix IV FPGA
Number of Cores	6	448	N/A
Performance /Watt (MT/J)	15.9	15.1	
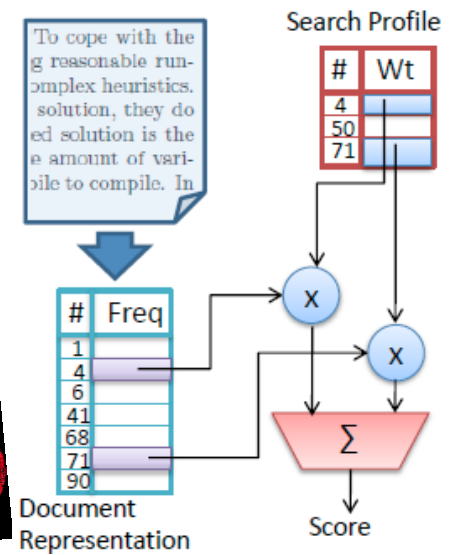
>5X Performance/Watt vs. GPU

Benefits of Altera OpenCL for FPGA

- ✓ **Superior Design Productivity**
    - Quick and easy evaluation of different solutions
    - Fast development / debug / optimization cycles
    - Faster time-to-market
- ✓ **Higher Performance**
    - >9X greater performance vs CPU alone running a Monte-Carlo Black Scholes simulation
- ✓ **Improved Power Savings**
    - >5X performance/Watt vs GPU-based heterogeneous systems running a document search algorithm
- ✓ **Greater Portability**
    - Reuse across multiple platforms, multiple generations