MS13544

Reed-Solomon and Convolutional Encoder (RESCUE)

Preliminary Information

DS5084-2.0 December 1998

The MS13544 is a Reed-Solomon and Convolutional Encoder for coding telemetry channel data according to the European Space Agency (ESA) Telemetry Channel Coding standard (AD1). The MS13544 can be viewed as four separate but interconnected encoders as shown in Figure 2 and in the functional description in this data sheet.

The MS13544 is fabricated on the Mitel Semiconductor SOS5 1·25µm CMOS/SOS process and is a fully static design. It has been designed for operation over the full military temperature range of −55°C to +125°C and is offered in a 28-lead ceramic flatpack.

Features

- Fully compliant with CCSDS and ESA Telemetry Channel Coding standards
- Selectable Interleave Depths from 1 to 8
- Up to 17 Mbit/s Reed-Solomon Throughput Data Rate
- MA1916 Compatible
- 28-pin Ceramic Flat Package, 50-mil lead pitch
- CMOS/SOS5 Technology; Radiation Hard, Latch-up free, very low SEU sensitivity

Applicable Documents

AD1 Telemetry Channel Coding Standard, ESA PSS-04-103, Issue 1, September 1989
AD2 Telemetry Channel Coding, CCSDS 101.0-B-3, May 1992
AD3 Packet Telemetry Standard, ESA PSS-04-106, Issue 1, January 1988
AD4 Packet Telemetry, CCSDS 102.0-B-4, November 1995
AD5 Advanced Orbiting Systems, CCSDS 701.0-B-2, November 1992
AD6 Radio Frequency and Modulation Standard, ESA PSS-04-105, Issue 1, December 1989

Reference documents

RD1 Virtual Channel Assembler Data Sheet, VCA MS12399, Mitel Semiconductor

RD2 Virtual Channel Multiplexer Data Sheet, VCM MS12396, Mitel Semiconductor

RD3 MA1916 Radiation Hard Reed-Solomon and Convolution Encoder Data Sheet, DS3590-3.2

Ordering Information

MS13544

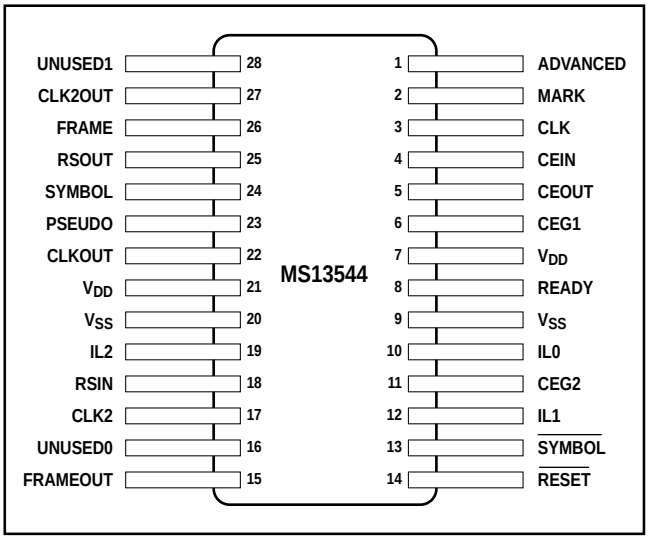

Figure 1 Pin connections – bottom view

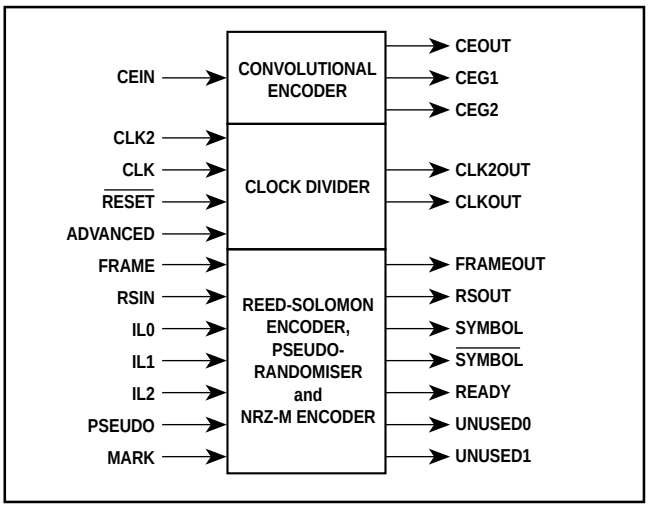

Figure 2 Simplified block diagram

Acronyms and Abbreviations

ASIC Application Specific Integrated Circuit
ASM Attached Synchronisation Marker
CADU Channel Access Data Unit
CCSDS Consultative Committee for Space Data Systems
CMOS Complementary Metal-Oxide Semiconductor
ESA European Space Agency
NRZ-L Non-Return to Zero - Level
NRZ-M Non-Return to Zero - Mark
SRAM Static Random Access Memory
VCA Virtual Channel Assembler
VCM Virtual Channel Multiplexer

FUNCTIONAL OVERVIEW

Summary of operation

The Reed-Solomon encoder generates codeblocks by receiving information symbols that are transmitted unmodified while calculating the corresponding check symbols that are transmitted in their turn after the information symbols. When unmodified data is received and transmitted such as synchronisation markers, the check symbol calculation is disabled. The calculation is independent of any previous codeblock and is performed correctly on the reception of the first information symbol after a reset.

The Pseudo-Randomiser generates a bit sequence according to AD1, which is optionally mixed with the Reed-Solomon encoder output. This function can be used to obtain the required bit transition density on a channel to enable a receiver on ground to maintain bit synchronisation.

The Reed-Solomon output is optionally Non-Return to Zero-Mark (NRZ-M) encoded according to the ESA Radio Frequency and Modulation standard (AD6).

The Convolutional encoder encodes data according to AD1. Data is input bit wise to the encoder synchronously with an input bit clock. For each input bit two symbol bits are generated and are output both serially and in parallel.

The encoding chain shown in Figure 3 is realisable with the MS13544.

The MS13544 operates in one mode where it is largely compatible with the Mitel MA1916 , and in a second mode with enhanced capabilities such as support for additional interleave depths, pseudo-randomising and NRZ-M encoding.

Functions not Included

The MS13544 does not generate the Attached Synchronisation Marker (ASM) as specified in the ESA Telemetry Channel Coding standard (AD1). Instead, it has a means for bypassing the check symbol calculation while receiving and transmitting unmodified data.

Numbering and Naming Conventions

In this document, a Galois Field symbol comprises 8 bits, where bit 7 is the most significant. An octet also comprises 8 bits, but for this and other representations bit 0 is the most significant. For both representations bit 0 is transferred first in a serial bit stream. Since the actual representation of the Reed-Solomon encoder input/output data is irrelevant to the encoding, octet representation may be used when symbols are specified.

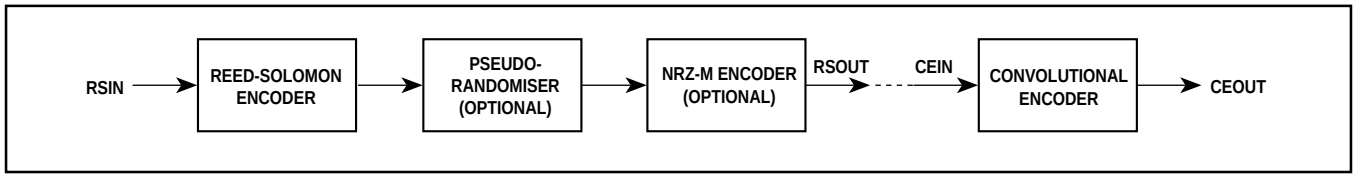

Figure 3 Encoding chain in the MS13544

Data Formats

The Telemetry Channel Coding Standard (AD1) specifies a Reed-Solomon block code with 8 bits per symbol, 255 symbols per codeword, the first 223 symbols containing the information symbols and the last 32 symbols constituting the check symbols. For transfers with more than 223 octets, codeblocks formed by interleaving of 2, 3, 4, 5 or 8 codewords are specified. Shortened codeword lengths are obtained using virtual fill. The CCSDS Telemetry Channel Coding Standard (AD2) allows the interleave depths 1, 2, 3, 4 and 5.

The ESA Packet Telemetry Standard (AD3) allows the standard codeblock lengths of 892, 1115 and 1784 octets when using Reed-Solomon encoding, corresponding to the interleave depths 4, 5 and 8. Shortened codeword lengths are obtained using virtual fill. A Channel Access Data Unit (CADU) protected with Reed-Solomon encoding is structured as shown in Table 1. The CCSDS Packet Telemetry Blue Book (AD4) allows the same interleave depths 1, 2, 3, 4 and 5 as in AD2.

The CCSDS Advanced Orbiting Systems Blue Book (ADS) allows interleave depths 1, 2, 3, 4 and 5. It also allows shortened codeblock lengths to accommodate compatibility with 32-bit microprocessor systems as shown in Table 2, where the number of suppressed symbols must be a multiple of the interleave depth, i.e. all codewords are of equal length. The MA1916 supports interleave depths 1, 4 and 5 as per RD1. The Virtual Channel Multiplexer (VCM) device supports interleave depths 1, 2, 4 and 5 as per RD2.

The MS13544 functionality as derived from the above requirements is specified in the Functional Description.

Attached synchronisation marker	Transfer frame	Reed-Solomon check symbols
4 octets	6 to 1784 octets	32, 64, 96, 128, 160, 192, 224, 256 octets

Table 1 Structure of a CADU as per ESA Packet Telemetry Standard

Interleave depth	Normal codeblock	Shortened codeblock	Suppressed information symbols
1	255	252	3
2	510	508	2
3	765	756	9
4	1020	1020	0
5	1275	1260	15

Table 2 Shortened codeblock length as per CCSDS Advanced Orbiting Systems

Description of a Typical System Using the MS13544

It is foreseen that the MS13544 will be used in telemetry encoders on ESA and commercial spacecraft, replacing the discontinued MA1916 device. The principal functions of a telemetry encoder as per AD3 is to receive data from the on-board data handling system to be formatted and output. The data can be received on virtual channels, where each virtual channel can be seen as an independent communication link. Since there is only one physical output from the telemetry encoder, the data from the virtual channels are time multiplexed on a frame basis. The telemetry encoder generates the Attached Synchronisation Marker (ASM), the header and the optional trailer of the Transfer Frame, and the optional Reed-Solomon check symbols. Optionally, the resulting data stream is convolutionally encoded. The Virtual Channel Assembler (VCA) and the Virtual Channel Multiplexer (VCM) are radiation-hard devices that together with the MS13544 can be used for implementing a telemetry encoder. A block diagram of a typical telemetry encoder is shown in Figure 4, comprising one VCA and SRAM pair per virtual channel, a VCM and an MS13544. In this example the MS13544 is operating in Advanced mode and is directly interfaced to the VCM, generating Reed-Solomon symbols (with optional pseudo-randomising and NRZ-M encoding) and convolutionally encoding the data.

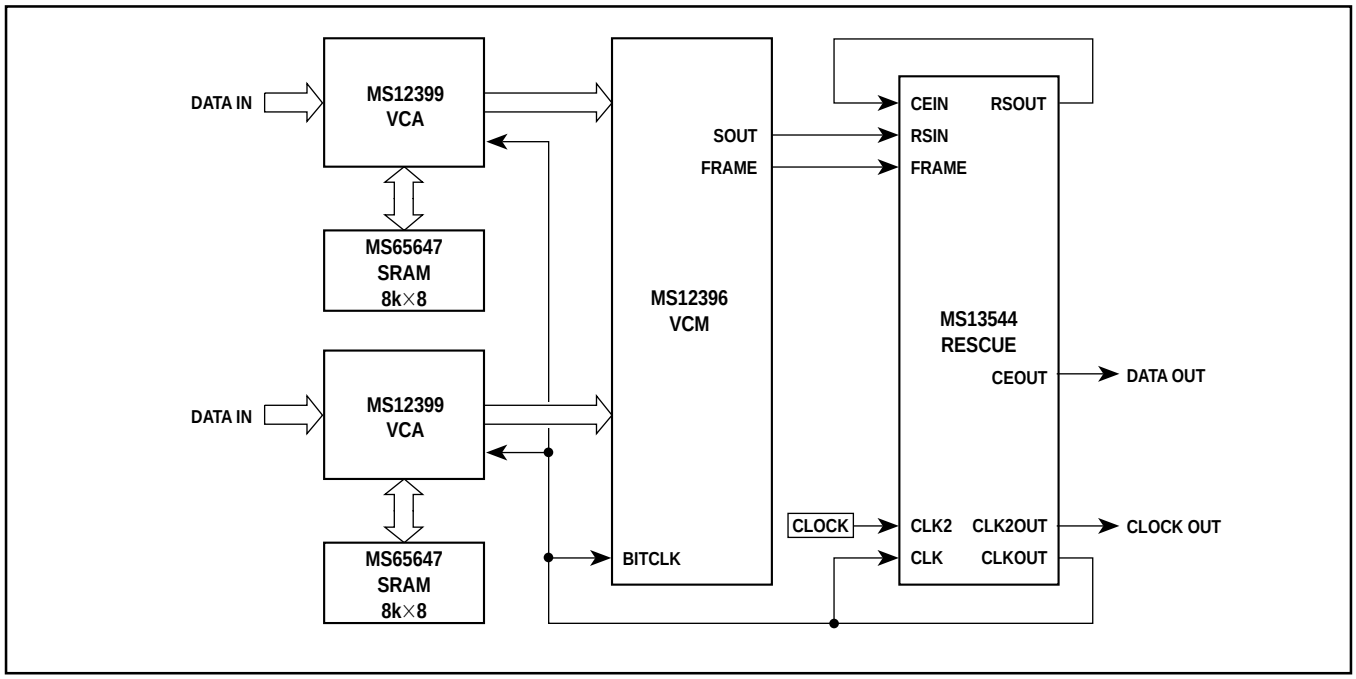

Figure 4 Telemetry encoder implemented with VCA, VCM and RESCUE devices

FUNCTIONAL DESCRIPTION

The MS13544 comprises a Reed-Solomon encoder, a Pseudo-Randomiser, an NRZ-M encoder, a Convolutional encoder and a Clock divider. A block diagram of the MS13544 is shown in Figure 5.

The Reed-Solomon encoder is implemented using a bit serial architecture as shown in Figure 6, except for the multiplication which is performed in parallel. Symbols are transferred serially in a dual basis representation. The multiplier operates directly on the dual basis representation, and there is no explicit base conversion before or after the check symbol encoding. It is possible to bypass the check symbol generation for an arbitrary time period to receive and transmit unmodified data.

The encoder does not require any initialisation of the check symbol memory before encoding a codeblock. Therefore, the feedback from the check symbol memory is suppressed when assumed to be zero; the product from the multiplier is suppressed when assumed to be zero. The symbol output delimiters SYMBOL and $\overline{\text{SYMBOL}}$ are re-synchronised for each codeblock. The READY signal emulates the MA1916 output ST1 as specified in the Interfaces section. The Pseudo-Randomiser and NRZ-M encoder are specified in Protocols and Algorithms, below.

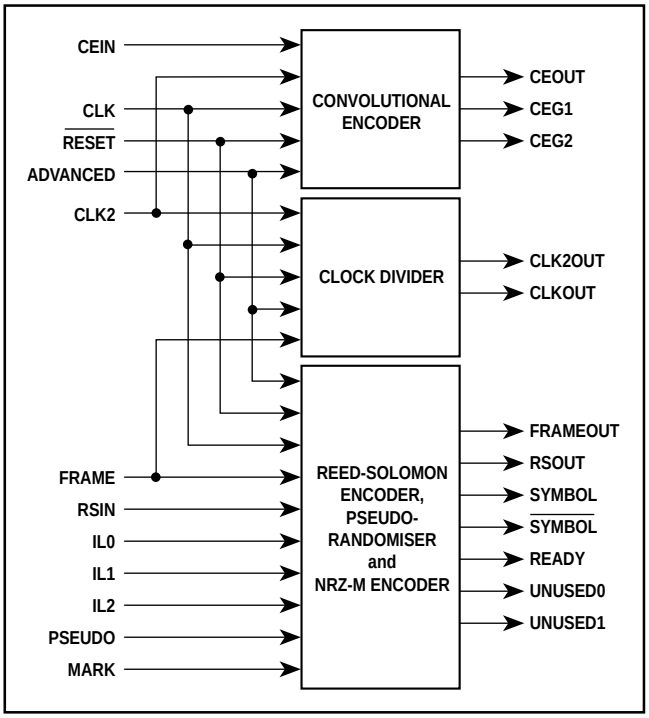

Figure 5 Block diagram of the MS13544

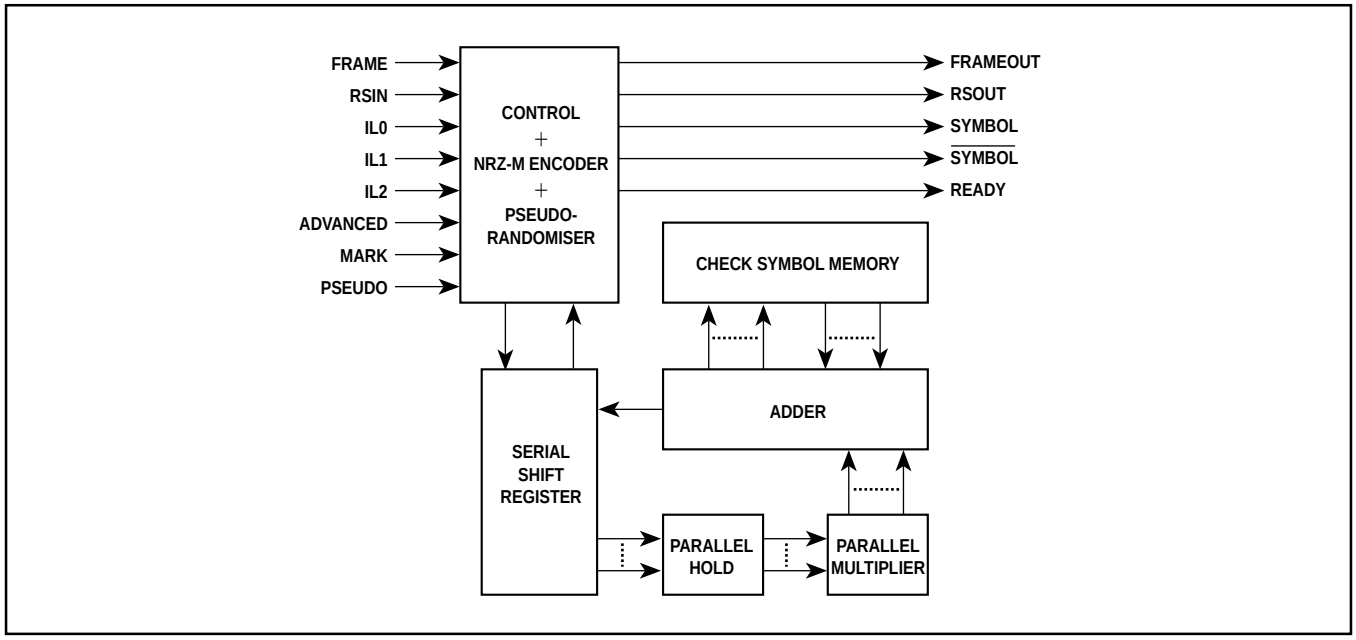

Figure 6 Block diagram of the Reed-Solomon, Preudo-randomiser and NRZ-M encoders

The Convolutional encoder shown in Figure 7 receives data bit wise synchronously with an input clock. For each input bit, two symbols are generated. When output serially, they are multiplexed on one output with a rate twice the input frequency. When output in parallel, they are output with a rate equal to the input frequency.

The Clock divider is driven by the rising edges of the CLK2 input, which is buffered and output as CLK2OUT. The CLKOUT output always outputs a clock with half the CLK2 input frequency, but its behaviour after reset is different for the two principal modes as further specified in Operational Modes, below. For the Advanced mode, the CLKOUT output becomes active as soon as the ADVANCED input is set to a logic 1. For the Basic mode (when ADVANCED = 0), the clocking and sampling schemes are similar to those of the MA1916 device. The CLKOUT output is inactive until the first low-to-high Frame transition after a reset (i.e. after RESET has been asserted). Further transitions on the Frame input do not affect the operation of the Clock divider. The behaviour of the clock divider is further specified in the Interfaces section.

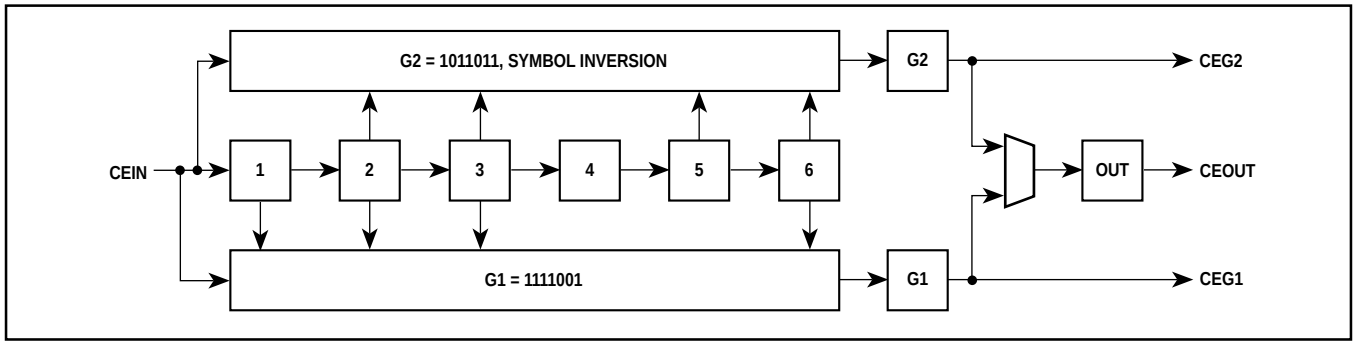

Figure 7 Block diagram of convolutional encoder

Operational modes

The MS13544 operates in two principal modes:

- **Basic:** largely compatible with the MA1916 device;
- **Advanced:** with enhancements as listed herein.

For the Basic mode (ADVANCED = 0), the Pseudo-Randomiser, the NRZ-M encoder and the Convolutional encoder outputs CEG1 and CEG2 are always disabled. The Reed-Solomon encoder supports the interleave depths as specified in Table 3 . No data is output before the first low-to-high transition on the FRAME input (since no driving clock is available until then); initially disabling any transfer of unmodified data.

For the Advanced mode (ADVANCED = 1), the Pseudo-Randomiser and the NRZ-M encoder are optionally enabled, and the Convolutional encoder outputs CEG1 and CEG2 are always enabled. The Reed-Solomon encoder supports the additional interleave depths as specified in Table 4.

The Reed-Solomon encoder operates in two modes: Receiving mode (when FRAME = 1): receiving and transmitting information symbols while calculating check symbols, Transmitting mode (when FRAME = 0): transmitting check symbols or receiving and transmitting unmodified data. Should Frame remain at logic 0 after all check symbols have been transmitted, then data arriving on RSIN will be output, allowing transfer of unmodified data (such as an ASM). It is not required to hold RSIN at logic 0 while check symbols are transmitted.

Protocols and algorithms

The Reed-Solomon encoder is compliant with the coding algorithm in AD1:

- There are 8 bits per symbol
- There are 255 symbols per codeword
- The encoding is systematic: the first 223 symbols transmitted are information symbols, and the last 32 symbols transmitted are check symbols
- The code can correct up to 16 symbol errors per codeword
- The field polynomial is:

$$f_{ESA}(x) = x^8+x^6+x^4+x^3+x^2+x+1$$

- The code generator polynomial is:

$$g_{ESA}(x) = \prod_{i=112}^{143}(x+\alpha^i) = \sum_{j=0}^{32} g_j \times x^j$$

for which the highest power of x is transmitted first.

- Interleaving is supported for depth I in range 1 to 8, where information symbols are encoded as I codewords with symbol numbers $i+j\times I$ belonging to codeword i (where $0 \leqslant i < I$ and $0 \leqslant j < 255$)
- Shortened codeword lengths are supported, allowing suppression of a number of information symbols equalling to any multiple of the selected interleave depth, where such suppressed symbols (maximum 221 per interleave depth) are assumed to be in the beginning of the codewords
- The input and output data from the encoder are in the representation specified by the following transformation matrix T_{ESA}, where ι_0 is transferred first:

$$[\iota_0\ \iota_1\ \iota_2\ \iota_3\ \iota_4\ \iota_5\ \iota_6\ \iota_7] = [\alpha_7\ \alpha_6\ \alpha_5\ \alpha_4\ \alpha_3\ \alpha_2\ \alpha_1\ \alpha_0] \times \begin{bmatrix} 0 & 1 & 1 & 1 & 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 1 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 0 & 1 & 1 & 1 \end{bmatrix}$$

and with the following matrix T^{-1}_{ESA} specifying the reverse transformation:

$$[\alpha_7\ \alpha_6\ \alpha_5\ \alpha_4\ \alpha_3\ \alpha_2\ \alpha_1\ \alpha_0] = [\iota_0\ \iota_1\ \iota_2\ \iota_3\ \iota_4\ \iota_5\ \iota_6\ \iota_7] \times \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 \end{bmatrix}$$

The Pseudo-Randomiser is compliant with the ESA Telemetry Channel Coding Standard (AD1) implementing the polynomial

$$h_{ESA}(x) = x^8+x^7+x^5+x^3+1$$

The memory elements of the Pseudo-Randomiser are re-initialised to all-ones before each codeblock. The generated sequence is optionally XOR-ed bit wise with the Reed-Solomon codeblock (selectable with the Pseudo input). The codeblock comprises the information and check symbols, but not the Attached Synchronisation Marker or any other unmodified data that is transferred while not transmitting information or check symbols. If a gap is inserted between the last bit of the check symbols and the first bit of the Attached Synchronisation Marker, while the transferred data stream will not be XOR-ed with the pseudo-random sequence. The XOR-ing of the Pseudo-Randomiser sequence and the Reed-Solomon encoder output is performed before the optional NRZ-M encoding. The Reed-Solomon output stream is either NRZ-L or NRZ-M encoded (selectable with the Mark input) according to ESA Radio Frequency and Modulation standard (AD6). NRZ-L encoding is equal to the logical bit value, whilst the NRZ-M encoded output only changes between levels on the occurrence of a logic 1. The encoding is performed after the optional pseudo-randomising and covers all data transmitted, including the Attached Synchronisation Marker and the codeblock. The waveforms for NRZ-L and NRZ-M encoding are shown in Figure 8.

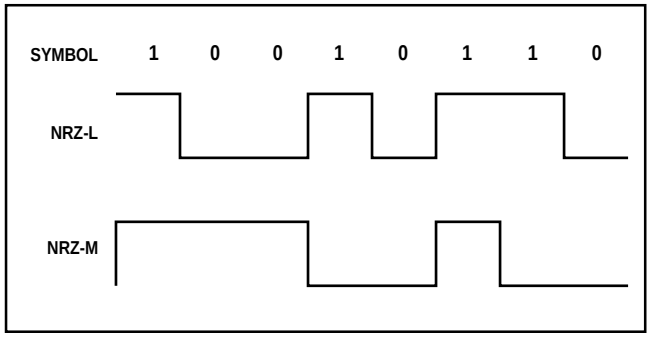

Figure 8 NRZ-L and NRZ-M waveforms

The Convolutional encoder is compliant with ESA Telemetry Channel Coding Standard (AD1), having a bit length of 7, a bit rate of 1/2, a G1 = 1111001 and a G2 = 1011011 with symbol inversion. G1 is associated with the first symbol.

Initialisation, state after reset and error handling
No explicit initialisation is required for the Reed-Solomon encoder before correct operation. Correct codeblock generation begins immediately on the reception of the first information symbol after a reset. It is possible to transfer unmodified data directly after a reset in Advanced mode, whereas for Basic mode unmodified data can only be transferred after the detection of FRAME = 1.

The output from the Reed-Solomon encoder, which is XOR-ed with the RSIN input, is held at logic 0 until the first low-to-high transition on the FRAME input after a reset (i.e. after $\overline{\text{RESET}}$ has been asserted). This ensures that unmodified data can be directly transferred after a reset for the Advanced mode, without being affected by the, at that time undefined, check symbol memory contents of the Reed-Solomon encoder.

The control logic is reset and re-synchronised on each detection of a rising or falling FRAME transition (sampled on the rising CLK edge), confining any bit error due to a single event upset to a single codeblock.

All registers in the Pseudo-Randomiser are re-initialised to logic 1 before each codeblock transfer (marked by a low-to-high transition on the FRAME input). The NRZ-M encoder is reset to level 0 when the $\overline{\text{RESET}}$ input is asserted.

All registers in the Convolutional encoder are reset to logic 0 when the $\overline{\text{RESET}}$ input is asserted, to be compatible with the MA1916 device, see Application Notes. Asserting the $\overline{\text{RESET}}$ input resets the clock divider to ensure a deterministic relation between the CLK2 input and CLKOUT.

Functionality for production test
The Pseudo and Mark inputs enable production test modes (when ADVANCED = 0) required for the testing of the MS13544. For the random logic a fault coverage greater than 96% is achieved with the production test. The check symbol memory is 100% tested during production test.

INTERFACES

The MS13544 has 12 input signals, 12 output signals (of which two are nominally unused) and no bidirectional signals, as shown in Figure 5. Together with four power supply pins, this gives a total pin count of 28.

Clock Divider Interface

CLK2: Convolutional output bit rate clock (I)
This CMOS input is the output bit clock for the Convolutional encoder. It is the single-phase clock driving the Convolutional encoder and the Clock divider, being active on the rising edge.

CLK: Convolutional input bit rate clock (I)
This CMOS input is the bit delimiter for the Convolutional encoder, with half the CLK2 frequency, and is sampled on the rising CLK2 edge. The CLK input is the input and output bit clock and the single-phase clock driving the Reed-Solomon encoder, the Pseudo-Randomiser and the NRZ-M encoder, being active on the rising edge.

CLK2OUT: Buffered CLK2 output (O)
This output carries a buffered version of the CLK2 input.

CLKOUT: Reed-Solomon bit rate clock (O).
This output carries a clock with half the CLK2 frequency. CLKOUT operates in two modes:

- **Basic:** outputs a logic 0 until the first low-to-high Frame transition after a reset has been sampled on the rising CLK2 edge, after which it begins to toggle (note that for the MA1916 device the sampling has been specified on the falling CLK2 edge). FRAME should be held at logic 0 during reset up until the first input codeblock, to ensure correct CLKOUT operation.
- **Advanced:** begins immediately to toggle on the rising CLK2 edge when a clock signal is supplied on the CLK2 input. (The Advanced mode allows the bit clock of the VCM device to be directly driven from the MS13544, without the need for an external clock divider as being the case with current VCM/MA1916 configurations).

ADVANCED: Selection between Advanced and Basic mode (I)
This static CMOS input selects between the Advanced and the Basic operational mode, the Advanced mode being selected when ADVANCED = 1. ADVANCED has a built-in pull-down resistor and may only change state while $\overline{\text{RESET}}$ = 0.

$\overline{\text{RESET}}$: Asynchronous reset (I)
The asynchronous Schmitt trigger input resets the MS13544 when asserted (i.e. $\overline{\text{RESET}}$ = 0). RESET is synchronised in the MS13544.

Reed-Solomon Encoder Interface

The Reed-Solomon encoder interface timings are shown in Figures 9 and 10.

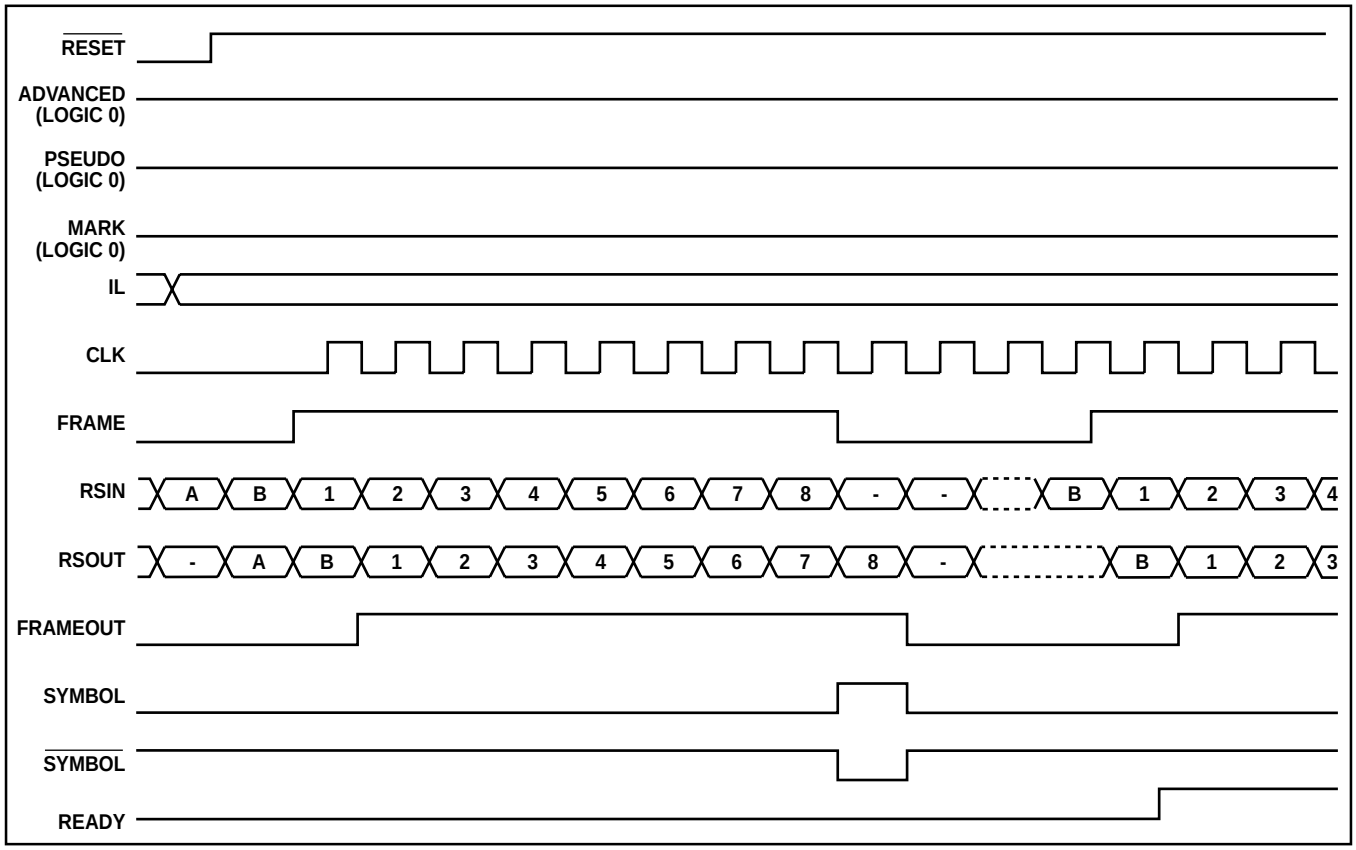

Figure 9 Reed-Solomon interface in Basic mode

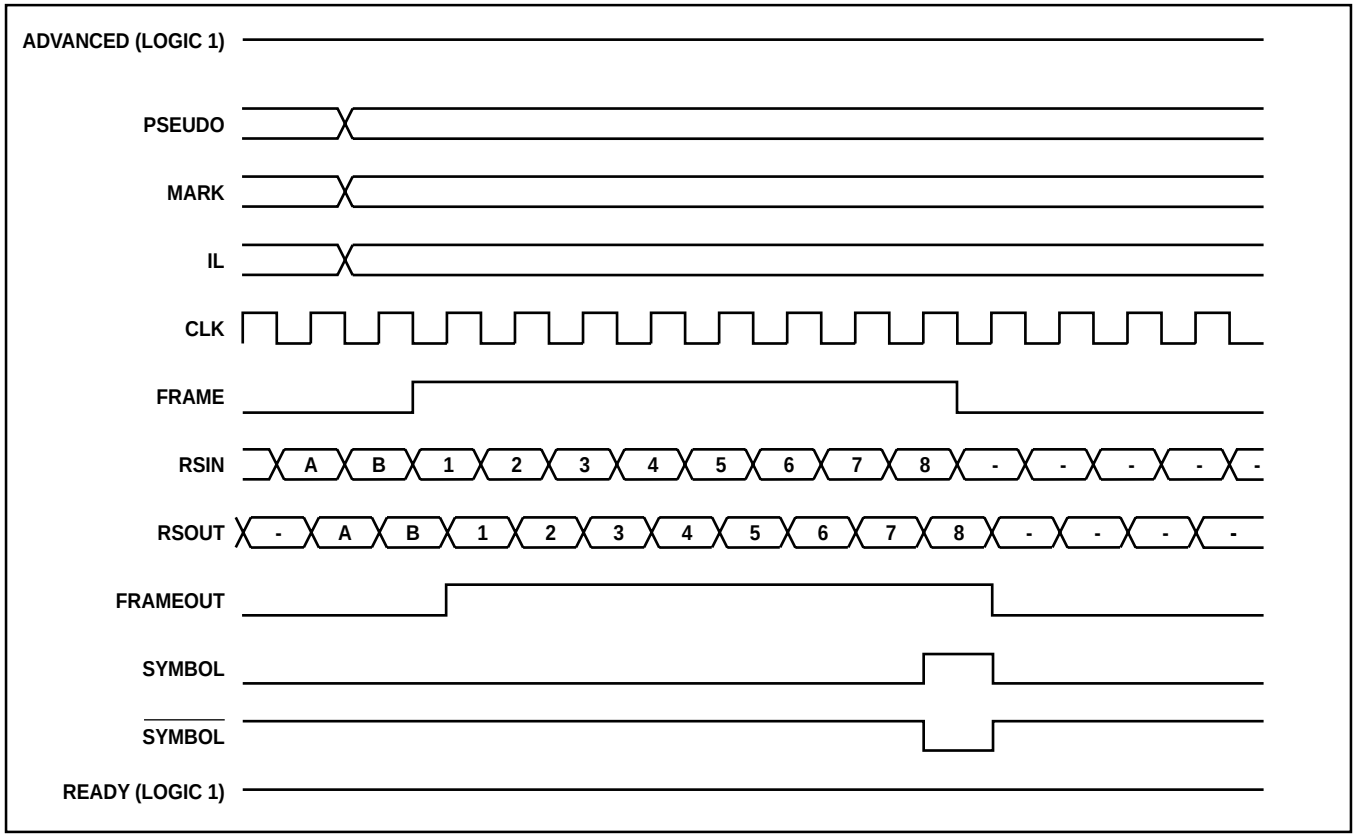

Figure 10 Reed-Solomon interface in Advanced mode

FRAME: Receive information symbols (I)
This CMOS input selects between the Receiving and Transmitting modes as described above. Information symbols are received when FRAME = 1 and check symbols are transmitted or unmodified data is transferred when FRAME = 0. It is sampled on the rising CLK edge.

FRAMEOUT: Receiving information symbols (O)
The FRAME input value is sampled on the rising CLK edge and is output as follows:

- **Basic:** FRAMEOUT changes state on the falling CLK edge and can be captured on the rising CLKOUT edge.
- **Advanced:** FRAMEOUT changes state on the rising CLK edge and can be captured on the rising CLK edge.

RSIN: Serial data input (I)
This CMOS input is used for receiving symbols or unmodified data. symbol bit 0 shall be transmitted first. RSIN is not required to be held at logic 0 while check symbols are transmitted (as being the case for the MA1916). RSIN is sampled on the rising CLK edge.

RSOUT: Serial data output (O)
This output is used for transmitting symbols or unmodified data. symbol bit 0 is transmitted first. Output data can optionally be pseudo-random encoded, and NRZ-L or NRZ-M encoded. RSOUT changes state as follows:

- Basic: on the falling CLK edge (on the edge after input data have been sampled on the rising CLK edge), and can be captured on the rising CLKOUT edge. A logic 0 is output until the first low-to-high FRAME transition after a reset. (The MA1916 asynchronously transmits RSIN data to RSOUT, whereas MS13544 outputs it on the falling CLK edge).
- Advanced: on the rising CLK edge, and can be capture on the rising CLKOUT edge.

SYMBOL: Symbol delimiter (O)
This output is asserted while the last bit of each symbol bit 7 is transferred (also generated when unmodified data is transferred). It is possible to capture SYMBOL as asserted on the same clock edge as symbol bit 7 is valid. SYMBOL changes state as follows:

- **Basic:** on the falling CLK edge, and can be captured on the rising CLKOUT edge. A logic 0 is output until the first low-to-high Frame transition after a reset;
- **Advanced:** on the rising CLK edge, and can be captured on the rising CLKOUT edge.

$\overline{\text{SYMBOL}}$: Inverted symbol delimiter (O)
This output behaves as the SYMBOL output, but with the inverted logical level.

READY: Reed-Solomon data valid (O)
This output operates in two modes:

- **Basic:** a logic 0 is output until the second low-to-high FRAME transition after a reset has been sampled on the rising CLK2 edge, after which a logic 1 is output on the subsequent falling CLK edge. (READY emulates the MA1916 pin ST1, which indicates that sufficient dummy data have been clocked through the Reed-Solomon encoder to allow correct encoding).
- **Advanced:** a logic 1 is output.

IL0 to IL2: Interleave depth selection (I)
These CMOS inputs select the interleave depth of the Reed-Solomon encoding, operating in two modes as defined in Table 3 and Table 4. The inputs have built-in pull-down resistors. In Advanced mode, the IL inputs can be dynamically changed between codewords. The inputs must then be stable one CLK period before FRAME is sampled on the rising CLK edge, taking into account the setup time. In Basic mode the inputs should not change after reset.

IL0	IL1	IL2	Interleave depth	Remarks	Information symbols	Check symbols
0	0	-	5	IL2 tied to logic 0 or 1	1115	160
0	1	-	4	IL2 tied to logic 0 or 1	892	128
1	0	-	1	IL2 tied to logic 0 or 1	223	32
1	1	-	5	IL2 tied to logic 0 or 1	1115	160

Table 3 Interleave depth selection in Basic mode

IL0	IL1	IL2	Interleave depth	Remarks	Information symbols	Check symbols
0	0	0	1		223	32
0	0	1	2		446	64
0	1	0	3		669	96
0	1	1	4		892	128
1	0	0	5		1115	160
1	0	1	6		1338	192
1	1	0	7		1561	224
1	1	1	8		1784	256

Table 4 Interleave depth selection in Advanced mode

PSEUDO: Enable pseudo-random encoding (I)
This CMOS input operates in two modes and has a built-in pull-down resistor:

- **Basic:** should be held at logic 0 for nominal operation, a production test mode is enabled when set to logic 1
- **Advanced:** enables the standard pseudo-random sequence to be XOR-ed with the output data from the Reed-Solomon encoder (when PSEUDO = 1). The PSEUDO input can be changed dynamically between codewords, taking the setup time to CLK into account.

MARK: Enable NRZ-M encoding (I)
This CMOS input operates in two modes and has a built-in pull-down resistor:

- **Basic:** should be held at logic 0 for nominal operation, a production test mode is enabled when set to logic 1
- **Advanced:** enables NRZ-M encoding of the output data from the Reed-Solomon encoder or the Pseudo Randomiser that is output on RSOUT (when MARK = 1). The MARK input can be changed dynamically between codewords, taking the setup time to CLK into account.

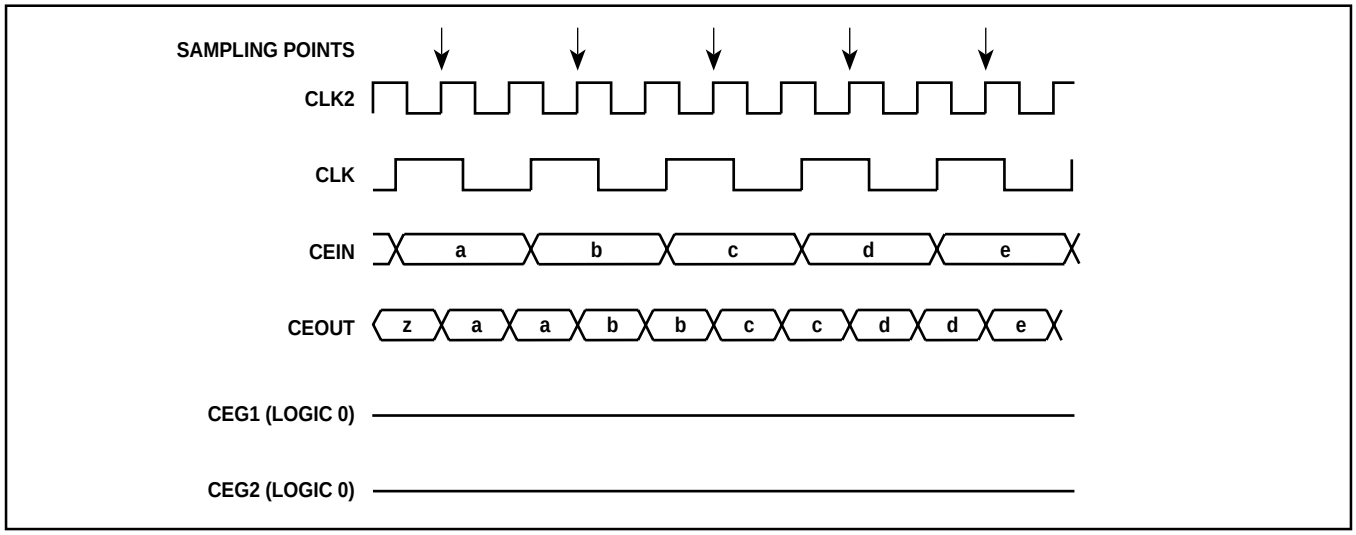

Figure 11 Convolutional encoder interface in Basic mode

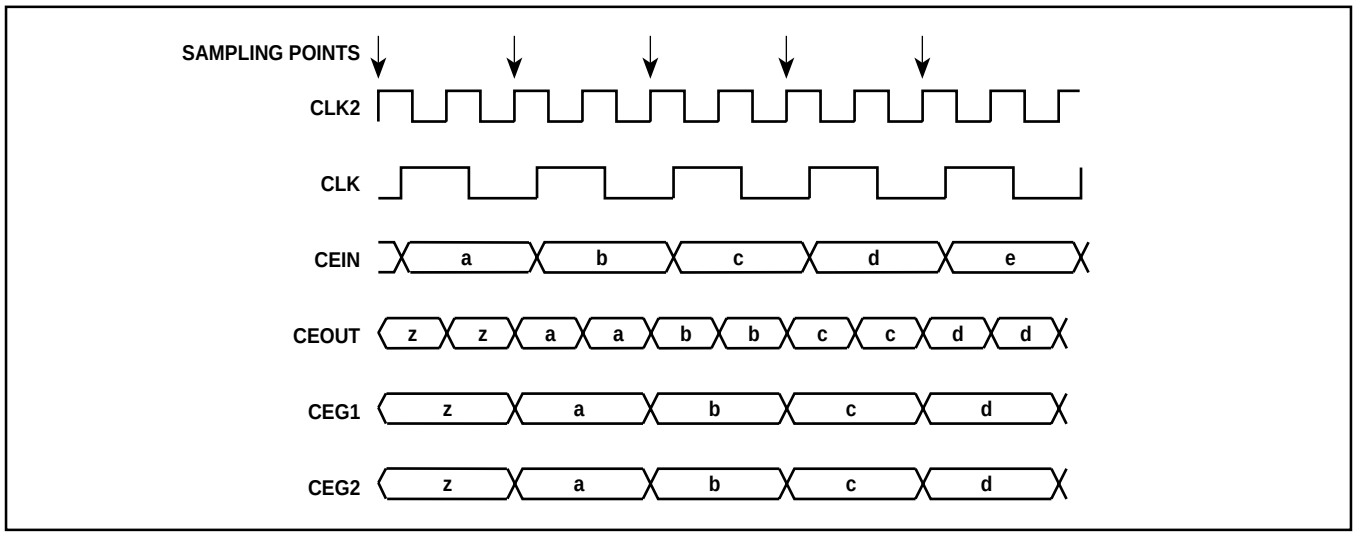

Figure 12 Convolutional encoder interface in Advanced mode

Convolutional Encoder Interface

The Convolutional encoder interface timings are shown in Figures 11 and 12, above.

CEIN : Serial data input (I)
This CMOS input is used for receiving input bits with a bit rate corresponding to half the CLK2 frequency. CEIN is sampled on the rising CLK2 edge when CLK = 1 in Basic mode, and when CLK = 0 in Advanced mode.

CEOUT: Multiplexed serial data output (O)
This output is used for transmitting output symbols with a bit rate equal to the CLK2 frequency. The G1 and G2 symbols are multiplexed on this output. The G2 symbol includes the associated inversion. CEOUT changes state on the rising CLK2 edge and can be captured on the falling CLK2OUT edge.

CEG1: Unmultiplexed serial data output (O)
This output operates in two modes:

- **Basic:** a logic 0 is output
- **Advanced:** the G1 symbol value is output with a bit rate corresponding to half the CLK2 frequency. CEG1 changes state on the rising CLK2 edge when CLK = 0 and can be captured on the falling CLK2OUT edge.

CEG2: Unmultiplexed serial data output (O)
This output behaves as the CEG1 output, but with the G2 symbol value (including the associated inversion).

Miscellaneous Pins

UNUSED0: Unused output (O)
This output is used only in production test mode. It outputs data read from the check symbol memory in serial form. In normal operation it outputs a logic 0.

UNUSED1: Unused output (O)
This output is at logic 0 in normal operation and is used for input testing in production test mode.

V_{DD} and V_{SS}: Power supply and ground
There are two power supply pins and two ground pins.

ELECTRICAL DESCRIPTION

Electrical Characteristics

T_{CASE} = −55°C to+125°C, V_{DD} = +5V±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Static current			TBD	µA	T_{AMB} = 25°C
			TBD	mA	T_{AMB} = 125°C
Dynamic current			TBD	mA	T_{AMB} = 25°C, f_{CLK} = TBD MHz
			TBD	mA	T_{AMB} = 125°C, f_{CLK} = TBD MHz
CMOS inputs					
Input low voltage	0·0		70%V_{DD}	V	V_{DD} = 5·5V
Input high voltage	30%V_{DD}		V_{DD}	V	
Input leakage current			±10	µA	
Capacitance			10	pF	
Schmitt trigger inputs					
Input low trigger voltage			0·9	V	V_{DD} = 4·5V
Input high trigger voltage	3·3			V	V_{DD} = 4·5V
Schmitt trigger hysteresis	0·4			V	V_{DD} = 4·5V
Input leakage current			±10	µA	V_{DD} = 5·5V
Capacitance			10	pF	
CMOS outputs					
Output low voltage			0·4	V	V_{DD} = 4·5V, I_{LOAD} = 4mA
Output high voltage	3·9			V	V_{DD} = 4·5V, $_{LOAD}$ = −4mA
Output leakage current			±100	µA	V_{DD} = 5·5V
Capacitance			10	pF	

AC characteristics
The maximum operating data rate for the Reed-Solomon encoder, Pseudo-Randomiser and the NRZ-M encoder is 17 Mbit/s.

The maximum operating input data rate for the Convolutional encoder is 17 Mbit/s with the corresponding output rate of 34 Mbit/s.

The maximum operating frequency of the Clock divider is 34 Mbit/s.

When the Reed-Solomon and the Convolutional encoders are cascaded, the maximum input data rate to the Reed-Solomon encoder is 15 Mbit/s.

When the Reed-Solomon encoder is interfaced with the VCM device, the maximum data rate is 8Mbit/s.

Absolute Maximum Ratings

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55 °C to +125 °C
Supply voltage, V_{DD}	−0.5 V to +7.0 V
Input voltage	−0.5 V to V_{DD} + 0.5 V
DC input current (any pin)	+10 mA
Power dissipation	200 mW
Output dissipation	50 mW/output
ESD minimum critical path failure voltage	1000V
Total radiation dose tolerance	>100 kRad (Si)
Latch-up	Immune
SEU sensibility	Minimised

Timing Characteristics
All timing characteristics are based on post-layout simulations and static timing analysis, and are subject to change without notice. All timing values are valid for the full operating temperature range, radiation range and power supply range, with 25 pF output load (add 4ns to the output delays per 25 pF load). See Figure 13.

Characteristic	Name	Value			Units	Conditions
		Min.	Typ.	Max.		
$\overline{\text{RESET}}$ low period	t_1	4			Clock periods	CLK2 periods when ADVANCED = 0 and CLK periods when ADVANCED = 1
CLK2 period	t_2	30			ns	
CLK2 low	t_3	15			ns	
CLK2 high	t_4	15			ns	
CLK period	t_5	60			ns	
CLK low	t_6	30			ns	
CLK high	t_7	30			ns	
CLK setup to CLK2 rise	t_8	6			ns	
CLK hold after CLK2 rise	t_9	5			ns	
ADVANCED setup time to $\overline{\text{RESET}}$ rise	t_{10}	4			Clock periods	CLK and/or CLK2periods
ADVANCED rise to CLKOUT enabled	t_{11}	-			ns	$\overline{\text{RESET}}$ = 0
CEln setup to CLK2 rise	t_{12}	5			ns	
CEln hold after Clk2 rise	t_{13}	6			ns	
FRAME setup to CLK2 rise	t_{14}	5			ns	ADVANCED = 0
FRAME hold after CLK2 rise	t_{15}	6			ns	ADVANCED = 0
FRAME hold after CLK rise	t_{16}	0			ns	
FRAME setup to CLK rise	t_{17}	26			ns	
RSIN hold after CLK rise	t_{18}	0			ns	
RSIN setup to CLK rise	t_{19}	13			ns	
PSEUDO hold after CLK rise	t_{20}	0			ns	ADVANCED = 1
PSEUDO setup to CLK rise	t_{21}	39			ns	ADVANCED = 1
Mark hold after CLK rise	t_{22}	0			ns	ADVANCED = 1
Mark setup to CLK rise	t_{23}	38			ns	ADVANCED = 1
IL hold after CLK rise	t_{24}	0			ns	
IL setup to CLK rise	t_{25}	38			ns	
CLK2 rise to CLKOUT stable	t_{26}	3		20	ns	ADVANCED = 1
CLK2 rise to CEOUT stable	t_{27}	3		24	ns	ADVANCED = 1
CLK2 rise to CEGI stable	t_{28}	3		25	ns	
CLK2 rise to CEG2 stable	t_{29}	3		26	ns	
CLK2 rise to CLK2OUT stable	t_{30}	2		15	ns	ADVANCED = 1
CLK rise to RSOUT stable	t_{31}	4		24	ns	ADVANCED = 0
CLK fall to RSOUT stable	t_{32}	4		27	ns	ADVANCED = 1
CLK rise to SYMBOL stable	t_{33}	4		25	ns	ADVANCED = 0
CLK fall to SYMBOL stable	t_{34}	4		28	ns	ADVANCED = 0
CLK fall to READY stable	t_{35}	4		29	ns	ADVANCED = 0
CLK rIse to $\overline{\text{SYMBOL}}$ stable	t_{36}	4		24	ns	ADVANCED = 1
CLK fall to $\overline{\text{SYMBOL}}$ stable	t_{37}	4		31	ns	ADVANCED = 0
CLK fall to FRAMEOUT stable	t_{38}	4		28	ns	ADVANCED = 0
CLK rise to FRAMEOUT stable	t_{39}	4		29	ns	ADVANCED = 1

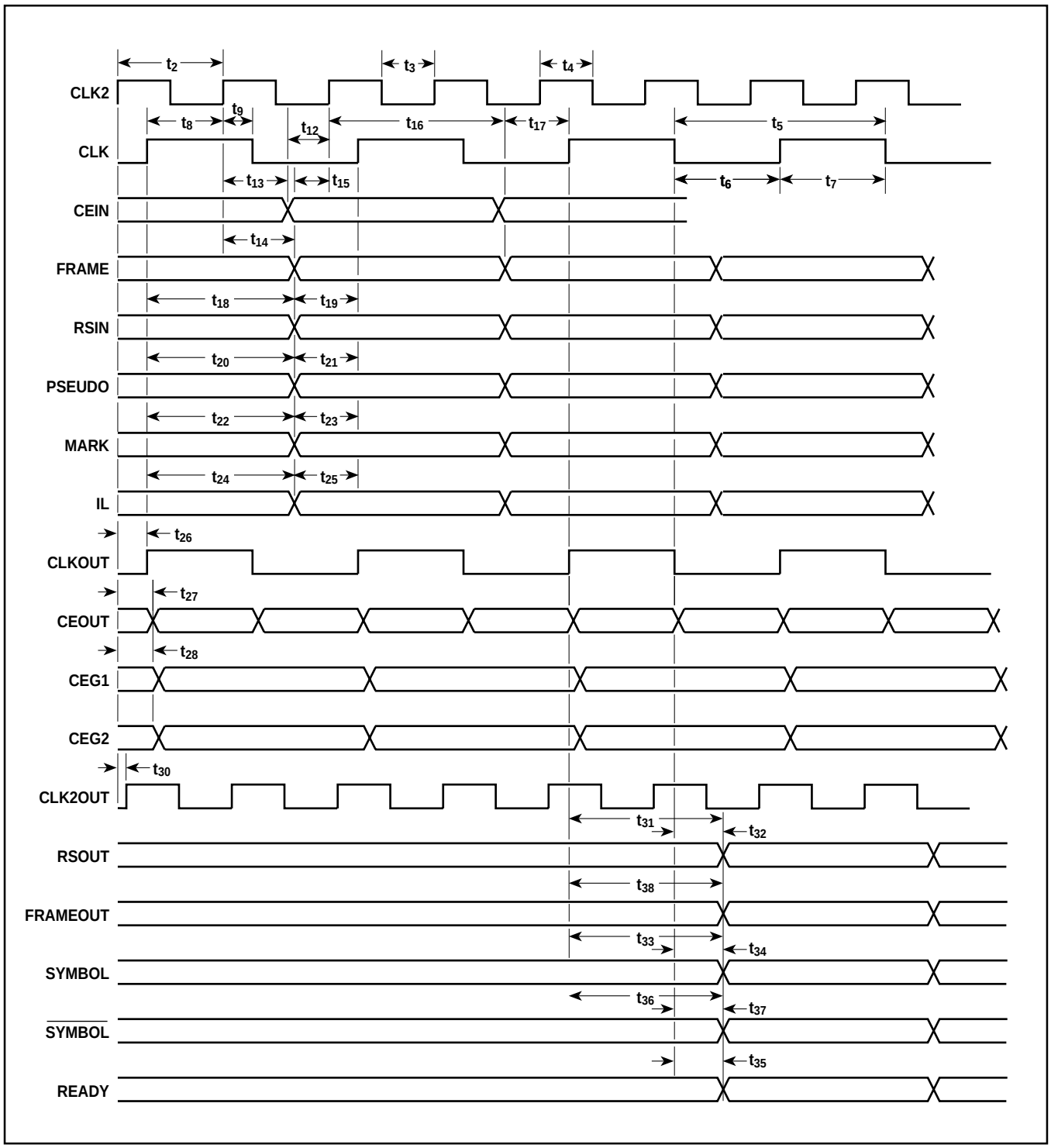

Figure 13 Waveforms for various signals

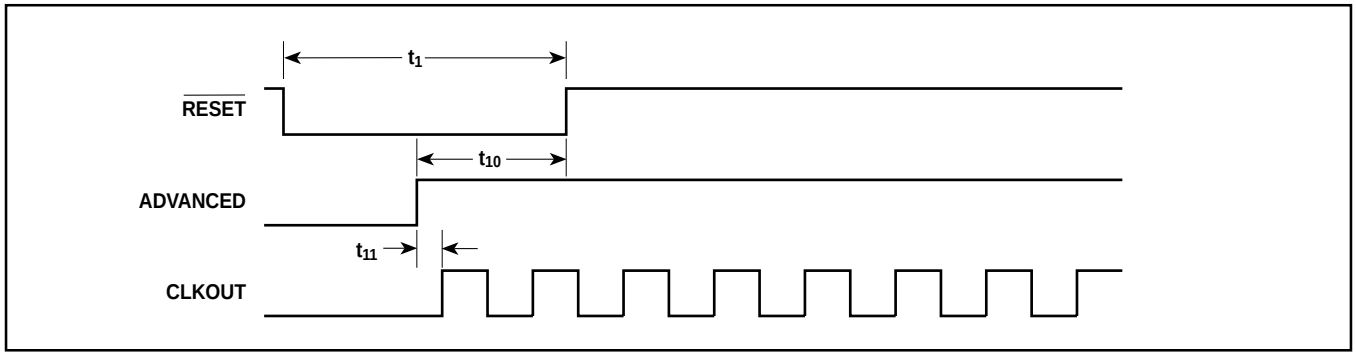

Figure 14 CLKOUT timing depending on ADVANCED

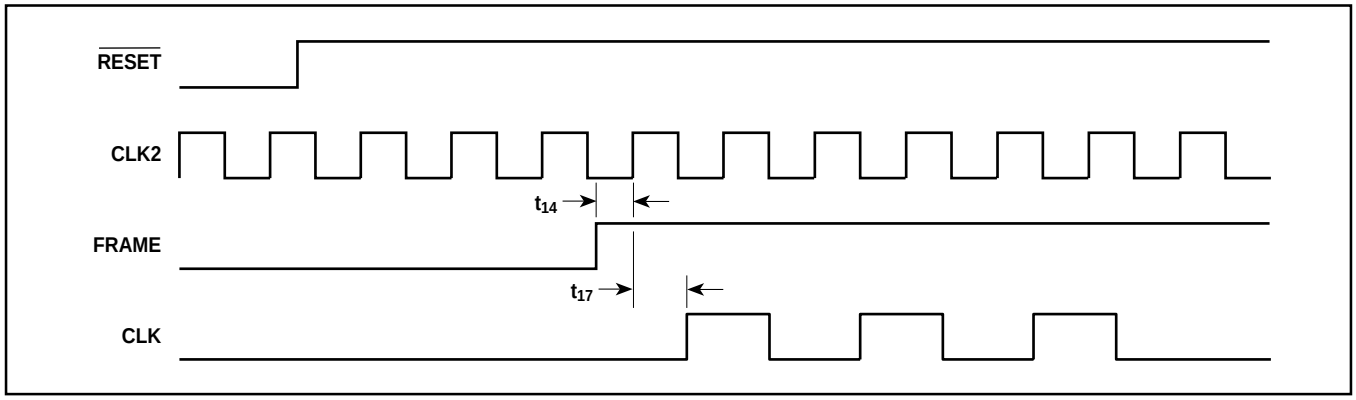

Figure 15 CLKOUT timing depending on FRAME and CLK2

APPLICATION NOTE

This is an application note on MS13544 compatibility with MA1916 when in Basic mode. See Table 5.

Difference in Clocking Schemes

The CLK input of the MA1916 is internally divided in a clock divider and drives the Reed-Solomon encoder with a bit clock having half the frequency. The MA1916's CE_CLKS input is used for delimiting input data to the Convolutional encoder.

The internal bit clock feed between the clock divider and the Reed-Solomon encoder has been avoided for the MS13544 since it would had precluded separate use of the encoders. Instead the CLK input directly drives the Reed-Solomon encoder. The user has therefore to connect externally the CLKOUT output with the CLK input whenever the internal clock divider is to drive the Reed-Solomon encoder. This external connection is normally already done in MA1916 applications when using the Reed-Solomon and the Convolutional encoders together, and should not pose any major limitations on backward compatibility.

Toggling CEOUT Output

The CEOUT output from the Convolutional Encoder is always toggling when the Clock divider is used while the MS13544 is in Basic mode, even when this encoder is not used. CEOUT is output on each rising CLK2 edge when the encoder is provided with input data. Since there is no internal bit clock feed from the internal clock divider to the Reed-Solomon encoder, the CLKOUT output has to be fed externally to the input clock CLK that drives the Reed-Solomon encoder. The same input pin is also used as the input bit delimiter for the Convolutional encoder, the encoder will therefore sense input data and consequently introduce activity on the CEOUT output.
The produced CEOUT output data will only be correct if also RSOUT is externally connected to CEIN, which should be the case when the Reed-Solomon and Convolutional encoders are cascaded.

First Attached Synchronisation Marker

An Attached Synchronisation Marker (ASM) preceding the first FRAME low-to-high transition after reset is not transmitted through the MS13544 when in Basic mode. The internal clock driving the Reed-Solomon encoder is not operating until the first rising FRAME edge is sampled. This is because the internal clock divider needs to synchronise the phase of the internal bit clock with that of the external bit clock. Therefore, the first ASM will be ignored since the FRAME input will not have yet been assert when the ASM is to be transmitted.
The MA1916 device will, however, transmit the first ASM since it asynchronously transfers the input data to the output, and is thus not dependent on the internal Reed-Solomon clock at that stage.

Clock synchronisation at start-up

In Basic mode, the CLKOUT output clock will begin toggling when the FRAME input is sampled asserted on the rising CLK2 edge. CLKOUT output clock will then be asserted for the first time. The MA1916 device samples the FRAME input on the falling CLK edge, and asserts the CLKS output on the subsequent rising CLK edge. For sake of simplicity, both the sampling and asserting has been done on the same CLK2 edge for the MS13544. FRAME should be held at logic 0 during reset up until the first input codeblock, to ensure correct CLKOUT operation.

The selected clocking scheme in Basic mode is compatible with MA1916 device assuming that the external bit clock driving the FRAME source is derived and divided from the rising CLK2 edge, and that FRAME (and RSIN) is clocked out on the falling edge of this external clock (as would be the case when connecting the MS13544 to a VCM).

Difference in Input/Output Signal Relations
With the MA1916 device, the RSE_OUT, SYZ, SZY and ST1 outputs and the SMC input can all be captured on the rising CLKS output clock. This is possible since the MSG input data is asynchronously transferred to the RSE_OUT when receiving data. The SMC input can thus be used as a frame delimiter, sampled on the same clock edge as the Reed-Solomon encoder outputs listed above.

In Basic mode, the RSIN input is sampled on the rising CLK edge and is then clocked out as RSOUT on the subsequent falling CLK edge to emulate the timing of the MA1916 device, but with the difference that all outputs are delayed by half a CLK clock period compared to the input data stream. The FRAMEOUT output has therefore been produced, being a delayed version of the FRAME input, suitable for being sampled on the rising CLKOUT edge together with the RSOUT, SYMBOL SYMBOL and READY outputs. In principle, the user will have to sample the MS13544 outputs one CLK period later than for the MA1916 device.

Note the difference between the FRAMEOUT and the SMC_OUT functionality, since the latter is used by the MA1916 test generator, which not implemented in the MS13544. Note that SYMBOL may change position due to re-synchronisation of internal logic on FRAME edges.

Static and Dynamic Mode Pins
In Advanced mode the IL and PSEUDO pins may be changed dynamically during the transmission of the Attached Synchronisation Marker, but have to be stable one CLK period before the FRAME input is sample asserted on the rising CLK edge. A change of the Mark input value will cause a disruption in the NRZ-M encoding whenever it take place, it is therefore recommended that the MS13544 is subsequently reset. Note that there is a setup time with respect to the rising CLK edge that has to be respected for the IL, PSEUDO and MARK inputs.

In Basic mode the IL, PSEUDO and MARK shall be held statically at a logic level during normal operation. Whenever one of the input values is changed, the MS13544 should be subsequently reset. Note that PSEUDO and MARK inputs will always be held at logic 0 during normal operation.

Since the MA1916 test generator is not implemented in the MS13544, the PSEUDO, IL(2) and MARK pins have different functions compared to the corresponding MA1916 pins. However, the pins can be held at logic 0 when in Basic mode, allowing for partial MA1916 compatibility.

Pinout Comparison
Pin 7 and pin 20 are specified as N/C for the MA1916 but are used for V_{DD} and V_{SS}, respectively, for the MS13544.

As explained above, the user has to externally connect the CLKOUT output to the CLK input whenever the internal clock divider is to drive the Reed-Solomon encoder.

The MS13544 does not implement the test generator and the production test structures available in the MA1916. Instead, it has its own production test structures. This affects the following inputs that have to be held statically at logical 0 during normal operation in Basic mode: IL2, PSEUDO, MARK and ADVANCED.

The above also affects the following outputs that have a different behaviour compared to the corresponding MA1916 pins: FRAMEOUT, UNUSED0, UNUSED1, CEG1 and CEG2.

Pin number	I/O type	MS13544 pin name	MA1916 pin name	Basic mode	Advanced mode	MA1916 compatible	Remarks
1	I	ADVANCED	T2	Tie to logic 0	Tie to logic 1	Partial	Mode selection
14	I	$\overline{\text{RESET}}$	n_RST	As n_RST	As Basic mode	Yes	Reset
17	I	CLK2	CLK	As CLK	As Basic mode	No	Does not drive Reed-Solomon encoder
27	O	CLK2OUT	CLK_OUT	As CLK_OUT	As Basic mode	Yes	CLK2 buffered
22	O	CLKOUT	CLKS	As CLKS	Always toggling	Yes	CLK2 divided by 2
3	I	CLK	CE_CLKS	As CE_CLKS	As Basic mode	No	Drives Reed-Solomon encoder
10	I	IL0	SEL_A	As SEL_A	Selects interleave depth	Yes	Supports 1-8 in advanced mode
12	I	IL1	SEL_B	As SEL_B	Selects interleave depth	Yes	Supports 1-8 in advanced mode
19	I	IL2	T 0	Tie to logic 0 or 1	Selects interleave depth	Partial	Supports 1-8 in advanced mode
23	I	PSEUDO	T3	Tie to logic 0	Enables pseudo randomiser	Partial	Production test when logic 1 in advanced mode
2	I	MARK	T1	Tie to logic 0	Enables NRZ-M encoding	Partial	Production test when logic 1 in advanced mode
26	I	FRAME	SMC	As SMC	As Basic mode	Yes	Compatible with VCM
15	O	FRAMEOUT	SMC_OUT	Logic 0	Delayed FRAME	No	Test generator not supported
18	I	RSIN	MSG	As MSG	As Basic mode	Yes	Compatible with VCM
25	O	RSOUT	RSE_OUT	As RSE_OUT	As Basic mode but on rising CLK edge	Yes	
28	O	UNUSED1	MSG_OUT	Logic 0	As Basic mode	No	Test generator not supported
16	O	UNUSED0	READY	Logic 0	As Basic mode	No	Test generator not supported
24	O	SYMBOL	SYZ	As SYZ	As Basic mode but on rising CLK edge	Yes	
13	O	$\overline{\text{SYMBOL}}$	SZY	As SZY	As Basic mode but on rising CLK edge	Yes	
4	I	CEIN	CE_IN	As CE_IN	As Basic mode	Yes	
5	O	CEOUT	CE_OUT	As CE_OUT	As Basic mode	Yes	
8	O	READY	ST1	As ST1	Logic 1	Yes	Emulates ST1
6	O	CEG1	TEST_POINT	Logic 0	G1 output	No	Old production test not supported
11	O	CEG2	ST2	Logic 0	G2 output (with inverter)	No	Old production test not supported
7	P	V_{DD}	N/C			No	Old N/C pin
20	P	V_{SS}	N/C			No	Old N/C pin
9	P	V_{SS}	V_{SS}			Yes	
21	P	V_{DD}	V_{DD}			Yes	

Table 5 Comparison between the pinouts of the MS13544 and the MA1916

http://www.mitelsemi.com

World Headquarters - Canada
Tel: +1 (613) 592 2122
Fax: +1 (613) 592 6909

North America
Tel: +1 (770) 486 0194
Fax: +1 (770) 631 3213

Asia/Pacific
Tel: +65 333 6193
Fax: +65 333 6192

Europe, Middle East and Africa (EMEA)
Tel: +44 (0) 1793 518528
Fax: +44 (0) 1793 518581

South America
Tel/Fax: +1 (48) 225 2016

For information regarding availability and pricing of the MS13544, contact:

Mitel Semiconductor AB
Parc Club du Golf
Bat. 9
F. 13856 Aix en Provence Cedex 3
Tel: + 33 (0) 4 42 39 33 60
Fax: + 33 (0) 4 42 39 72 27

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