

8 *Flip-Flops*

Logic elements that process **memory** - circuits that retain their output even though their inputs change - are introduced. These single-bit logic elements, called **flip-flops** or **latches**, are available in various types. Those examined are:

- **D** flip-flops
- **JK** flip-flops
- **SR** latches

Flip-flops or latches such as these can be used to form **registers** capable of holding or manipulating multiple bits of data. A serial-in, parallel-out register is studied.

NOTE: The PRELAB for this lab has Altera MAXPLUS simulation requirements. See the Prelab sheets for more information.

I. D Flip-Flop

The 7474 has two D-type flip-flops on the same chip. This section will use only one of these two flip-flops.

- A. Asynchronous Preset and Clear (fill out Table I.A on lab data sheet)
1. Connect power and ground to a 7474. Connect Q (pin 5) to DI-1 and Q' (pin 6) to DI-2. Q is the output of the flip-flop and Q' is the complement of the output.
 2. Connect DS-1 to PR (pin 4) and DS-2 to CLR (pin 1). Set both data switches high.
 3. The preset and clear inputs are active low. To see how this works, toggle DS-1 (change it from high to low to high) with DS-2 remaining high. This presets the flip-flop. Q should be a 1 and Q' should be a 0.
 4. Toggle DS-2 with DS-1 remaining high. This clears the flip-flop. Q should be a 0 and Q' should be a 1.
 5. The clear and preset inputs are usually used during a system initialization and must remain high for normal flip-flop operation. Practice presetting and clearing the flip-flop a few more times.
- B. Normal Operation Using the D and Clock Inputs (fill out Table I.B on lab data sheet)
1. Connect DS-3 to the D input (pin 2) and DS-4 to the clock input (pin 3) of the flip-flop. Set both DS-3 and DS-4 low.
 2. Use DS-1 to preset the flip-flop. Make sure Q is a 1, also that DS-1 and DS-2 are high after presetting.
 3. The 7474 is a positive edge-triggered device which means that data is only transferred from the D input to the Q output when the clock makes a low to high transition. With the D input remaining low, change the clock from low to high. Notice that the state of Q has changed from 1 to 0. Q' has also changed.
 4. Change the D input to a 1 and change the clock from a 1 to a 0. Notice that the state of Q did not change to the input present at the D input since the proper clock transition was not provided. Change the clock back to a 1 and notice that Q changes to a 1.
 5. Practice making Q a 1 and a 0 by changing the state of the D input and toggling the clock.
- C. D Flip-Flop Truth Table Inputs (fill out Table I.C on lab data sheet)
1. One way of presenting the truth table for a D-type flip-flop is given in your TTL Data Book. Another way is presented below.

2. The state of Q (1 to 0) before the positive clock edge occurs is called the present state. The state of Q after the clock edge is called the next state. The present state can be denoted by Q and the next state by Q^+ . A positive edge at an input is denoted by an arrow in the upward direction. Complete Table 1 below for the D flip-flop.
3. Table 1 is only valid if the preset and clear inputs are held high. Construct a new table for the D flip-flop with two columns added, one for preset and one for clear. Have the instructor check this truth table.
4. Inputs which are left unconnected are said to be floating. A floating input normally floats high in the TTL logic family. This allows the preset and clear inputs of the D flip-flop to be left unconnected for normal operation in most cases. However, in some instances, floating inputs may not float high. If the preset and clear inputs are left unconnected and they do not float high, then the flip-flop will not operate properly. Since there is no way to be sure which way an input will float, the preset and clear inputs should always be connected to a logic high. This can easily be done by using a data switch.

D	Q	CLOCK	Q^+
0	0	↑	
0	1	↑	
1	0	↑	
1	1	↑	

Table 1 D Flip-Flop Truth Table

II. JK Flip-Flop



Like the 7474, the 74109 has two flip-flops on the same chip. The difference is that the 74109 has two JK flip-flops. Use only one of these flip-flops in this part of the experiment.

A. Asynchronous Preset and Clear

1. Connect power and ground to the 74109. Notice that these connections are different from other chips. Connect Q and Q' to data indicators. Connect DS-1 and DS-2 to the preset and clear inputs. Perform the same operations with the preset and clear inputs of the JK flip-flop as was done with the D flip-flop.

B. Normal operation using the J, K, and Clock Inputs

1. The JK flip-flop is a positive edge-triggered device which means that the outputs, Q and Q' will only be affected by the J and K inputs when a low to high transition is produced at the clock input. Note that for the 74019 the J input is high true, the K input is low true (note the bar over the K input in the 74109 data sheet). Use a 7404 inverter to invert the switch input to the

K input so that both J and K are high true inputs. You may have a 7476 in your parts kit instead of a 74019 - a 7476 also has two JK flip-flops, but both J and K are high true inputs so you would not need the inverter with a 7476.

2. The JK flip-flop operation is as follows (assuming that both J,K are high true - 0 = L, 1 = H):
 - a. J=0, K=0 : No Change. Q will not change state (neither will Q') when a negative edge is supplied to the clock.
 - b. J=0, K=1 : Go to 0. Q will become a 0 (Q' goes to 1) when a negative edge is supplied to the clock.
 - c. J=1, K=0 : Go to 1. Q will become a 1 (Q' goes to 0) when a negative edge is supplied to the clock.
 - d. J=1, K=1 : Complement. Q gets the complement of its previous state (as does Q') when a negative edge is supplied to the clock.

C. JK Flip-Flop Truth Table

1. Consult the TTL Data Book for one version of the JK flip-flop truth table.
2. Construct a truth table similar to the one which was made for the D flip-flop (fill out Table II on lab data sheet). Include columns for J, K, the clock, Q, preset, clear, and Q'. Have the instructor check your truth table.

III. SR Flip-Flop

.....

- A. The SR flip-flop operation is as follows (there is no clock):
 1. S=0, R=0 : No Change. Q will not change state (neither will Q')
 2. S=0, R=1 : Reset. Q gets reset (goes to 0). Q' will be a 1.
 3. S=1, R=0 : Set. Q gets set (goes to 1). Q' will be a 0.
 4. S=1, R=1 : Not allowed.
- B. NOR Implementation
 1. Connect the circuit shown in Figure 1. Use DS-1 for S, DS-2 for R, DI-1 for Q, and DI-2 for Q'.

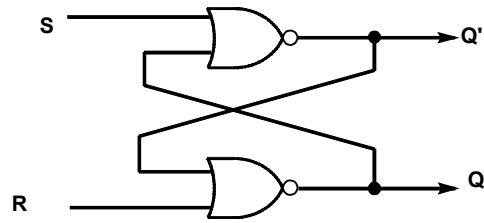


Figure 1

2. Set S to 0 and R to 1. This resets the flip-flop which means that Q is a 0 and Q' is a 1. This will always be the case when S=0 and R=1 regardless of the previous state of Q.
3. Go from S=0 and R=1 to S=0 and R=0. Q stays at 0 because SR=00 is the no change input combination and the previous state of Q was a 0.
4. Set S to 1 and R to 0. This input combination sets the flip-flop (Q=1, Q'=0) regardless of the previous state of Q.
5. Go from SR=10 to SR=00. This time Q stays at 1 which confirms that Q does not change state if S and R are 00.
6. Set S to a 1 and R to a 1. This input combination is disallowed since Q and Q' are both 0 and are not complements of each other. This input combination should always be avoided.
7. Do steps 2 through 5 a few more times to get the feel of the operation of the SR flip-flop. Include changing S and R from 01 to 10 and from 10 to 01.

C. NAND Implementation

1. Connect the circuit shown in Figure 2. Use DS-1 for S, DS-2 for R, and DI-1 for Q, and DI-2 for Q'. Notice that this implementation is different from the previous one in that S feeds into the gate whose output is Q and R feeds into the gate whose output is Q'.

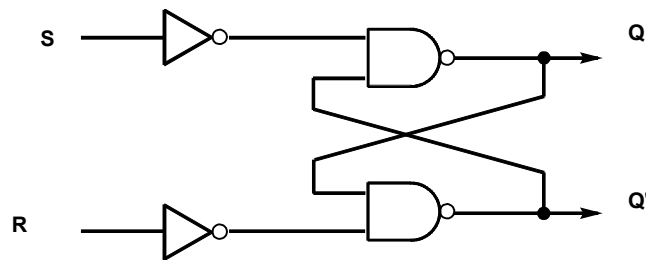


Figure 2

2. Repeat steps 2 through 5 of the previous section to verify that this implementation of the SR flip-flop is equivalent to the NOR implementation.
3. Set S and R to 11 and notice that Q and Q' are once again not complements of each other, but this time they are both equal to 1. This is the only

difference in the two implementations, but causes no problem since SR=11 is a disallowed input combination in both cases.

D. SR Flip-flop with Enable

1. Connect the circuit of Figure 3. Use DS-1 for S, DS-2 for R, DS-3 for Enable, DI-1 for Q and DI-2 for Q'.

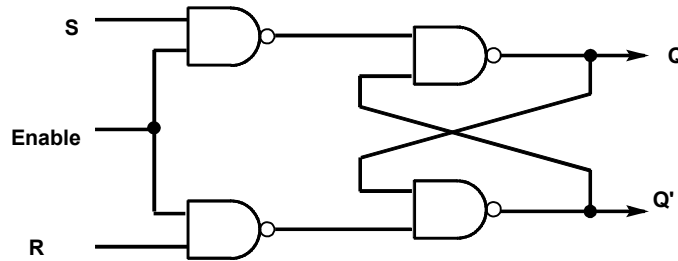


Figure 3

2. Enable=1 enables the S and R inputs. To see what this means, set enable high and verify that the circuit works exactly like the circuit of Figure 2.
3. Enable=0 disables the inputs. Show this by setting enable low and changing the S and R inputs. Notice that the outputs will not change regardless of what changes occur at S and R.

E. SR Flip-flop Truth Table

1. Make out a truth table for the SR flip-flop with the enable. Include columns for S, R, Enable, Q and Q'.
2. Consult the TTL Date Book for the truth table of 74LS279 which is a quadruple SR Latch.

IV. Serial-in, Parallel-out, Shift Register

.....

- A. A serial-in, parallel-out, shift register has one data input line and multiple data output lines. Such a shift register with four outputs is shown in Figure 4. Connect this circuit.

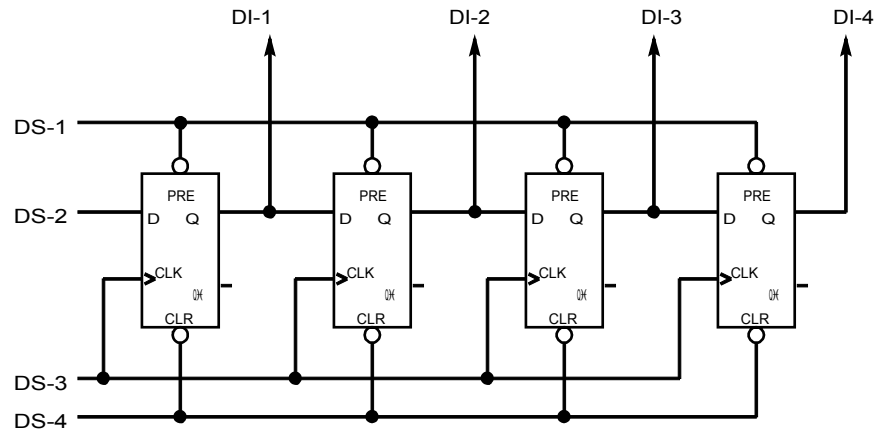


Figure 4

- B. Use DS-1 and DS-4 to clear all four flip-flops.
- C. DS-2 is the data input line. Set DS-2 high. DS-3 is used to provide clock pulses. Toggle the clock several times to see the results. Change DS-2 to a 0 and toggle the clock several more times. Continue to toggle the clock, but change the logic level of DS-2 after each clock pulse to further understand the operation of this type of shift register. Have the instructor verify the operation of your shift register.

V. Report

.....

Include only the following sections of this experiment in the laboratory report:

- A. Section I. C.3
- B. Section II.B
- D. Section II.C.2
- E. Section III.B

PRE LAB DATA SHEET**TA CHECKOFF** _____

ANSWER THE FOLLOWING QUESTIONS

:

1. Give an example of a level sensitive storage device (a latch), and an edge sensitive storage device (a flip-flop). Explain the operation of each (draw timing diagrams).
2. What do Preset, Set and Clear do to a flip-flop? These are called Asynchronous inputs. How are they different from a Synchronous input?
3. How are the NOR implementation and the NAND implementations of an SR latch functionally different?
4. Locate the datasheets for the 74LS74, 74LS76 (or 74LS109, whichever one is in your parts kit), and 74LS279 devices and have them with you in lab.
5. ALTERA MAXPLUS REQUIREMENTS: The ZIP archive with this lab contains an incomplete schematic called *fig4.gdf*. Complete this schematic so that it corresponds to Figure 4 (see Part IV). Simulate this circuit using the provided *fig4.scf* waveform file and verify it produces the results that you expect. You should have a screenshot of your schematic + simulation at the beginning of lab or demo the design for the TA using a portable PC at the beginning of the prelab.

ALTERA SIMULATION CHECKOFF (TA Signature): _____

LAB DATA SHEET

TA CHECKOFF _____

I. D FLIP-FLOP

A.

PRE	CLR	Q	/Q
1	1		
0	1		
1	1		
1	0		
1	1		

B.

PRE	CLR	D	CLK	Q	/Q
1	1	0	0		
1	1	0	↑		
1	1	1	0		
1	1	1	↑		
1	1	1	0		

C.

PRE	0	1	0	1	1	1	1	1
CLR	1	0	0	1	1	1	1	1
CLK	x	x	x	↑	↑	↑	↑	0
D	x	x	x	1	1	0	0	x
Q	1	0	1	1	0	1	0	
Q+						0	0	

II. J-K FLIP-FLOP (assuming both JK are high true)

PRE	0	1	0	1	1	1	1	1	1	1	1
CLR	0	0	1	1	1	1	1	1	1	1	1
CLK	x	x	x	↓	↓	↓	↓	↓	↓	↓	↓
J	x	x	x	0	0	1	1	0	0	1	1
K	x	x	x	0	0	1	1	1	1	0	0
Q				0	1	0	1	0	1	0	1
Q+											

III. S-R FLIP-FLOP

S	R	NOR		NAND		SR with Enable		
		Q	Q'	Q	Q'	Enable	Q	Q'
0	0					1		
0	1					1		
1	0					1		
1	1					1		
0	0					0		
0	1					0		
1	0					0		
1	1					0		
1	0					1		
0	0					1		
0	1					1		
1	1					1		

IV. SERIAL IN, PARALLEL OUT SHIFT REGISTER

INPUT				OUTPUT			
PRE	D	CLK	CLR	DI1	DI2	DI3	DI4
0	x	x	0				
0	x	x	1				
1	x	x	0				
1	x	x	1				
1	1	↑	1				
1	1	↑	1				
1	1	↑	1				
1	1	↑	1				
1	0	↑	1				
1	0	↑	1				
1	0	↑	1				
1	0	↑	1				
1	1	↑	1				
1	0	↑	1				
1	1	↑	1				
1	0	↑	1				
1	1	↑	1				
1	0	↑	1				
1	0	↑	1				
1	1	↑	1				

In your lab report, discuss the following:

1. How does the Enable affect your SR flip-flop? (1)
2. What is a serial-in, parallel-out shift register? Explain how the data is shifted using a timing diagram as described below. Make sure you use ENOUGH clock cycles to show the nature of the circuit. (5)
3. How do you clear all the flip-flops in the shift register? (1)

