CHOOSE THE IDEAL VIRTEX-4 DEVICE FOR YOUR APPLICATION

				Virtex-4 L	X (Logic)							Virtex-4	SX (Signal	Processing)	Virtex-4 F	X (Embedd	ed Processi	ng & Serial	Connectivity	<i>ı</i>)
				XC4VLX15	XC4VLX25	XC4VLX40	XC4VLX60	XC4VLX80	XC4VLX100	XC4VLX160	XC4VLX200	XC4VSX25	XC4VSX35	XC4VSX55	XC4VFX12	XC4VFX20	XC4VFX40	XC4VFX60	XC4VFX100	XC4VFX140
Easyl	Path™ Cost Reduc	tion Solu	tions 1	_	XCE4VLX25	XCE4VLX40	XCE4VLX60	XCE4VLX80	XCE4VLX100	XCE4VLX160	XCE4VLX200	XCE4VSX25	XCE4VSX35	XCE4VSX55	_	XCE4VFX20	XCE4VFX40	XCE4VFX60	XCE4VFX100	XCE4VFX140
	CLB Array	(Row x Co	olumn)	64 x 24	96 x 28	128 x 36	128 x 52	160 x 56	192 x 64	192 x 88	192 x 116	64 x 40	96 x 40	128 x 48	64 x 24	64 x 36	96 x 52	128 x 52	160 x 68	192 x 84
			Slices	6,144	10,752	18,432	26,624	35,840	49,152	67,584	89,088	10,240	15,360	24,576	5,472	8,544	18,624	25,280	42,176	63,168
		Logi	c Cells	13,824	24,192	41,472	59,904	80,640	110,592	152,064	200,448	23,040	34,560	55,296	12,312	19,224	41,904	56,880	94,896	142,128
		CLB Flip	Flops	12,288	21,504	36,864	53,248	71,680	98,304	135,168	178,176	20,480	30,720	49,152	10,944	17,088	37,248	50,560	84,352	126,336
	Max. Distri	ibuted RA	M Bits	98,304	172,032	294,912	425,984	573,440	786,432	1,081,344	1,425,408	163,840	245,760	393,216	87,552	136,704	297,984	404,480	674,816	1,010,688
Bloc	k RAM/FIFO w/ECC	(18 kbits	each)	48	72	96	160	200	240	288	336	128	192	320	36	68	144	232	376	552
	Total Bi	ock RAM ((kbits)	864	1,296	1,728	2,880	3,600	4,320	5,184	6,048	2,304	3,456	5,760	648	1,224	2,592	4,176	6,768	9,936
	Digital Clock N	Managers ((DCM)	4	8	8	8	12	12	12	12	4	8	8	4	4	8	12	12	20
Phas	e-matched Clock I	Dividers (F	PMCD)	0	4	4	4	8	8	8	8	0	4	4	0	0	4	8	8	8
		Max Selec	t I/O™	320	448	640	640	768	960	960	960	320	448	640	320	320	448	576	768	896
		Total I/O	Banks	9	11	13	13	15	17	17	17	9	11	13	9	9	11	13	15	17
	Digitally Contro	olled Impe	dence	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Max Diffe	erential I/O) Pairs	160	224	320	320	384	480	480	480	160	224	320	160	160	224	288	384	448
		I/O Star	ndards	LDT-25, LVDS-	25, LVDSEXT-25,	BLVDS-25, ULVDS	5-25, LVPECL-25,	LVCMOS25, LVC	MOS18, LVCMOS	15, PCI33, LVTTL,	LVCMOS33, PCI->	C, PCI66, GTL, C	GTL+, HSTL I (1.5	5V,1.8V), HSTL II (1	.5V,1.8V), HSTL III	(1.5V,1.8V), HST	L IV (1.5V,1.8V),	SSTL21, SSTL211, S	STL18 I, SSTL18 II	
	Xtre	emeDSP™	Slices	32	48	64	64	80	96	96	96	128	192	512	32	32	48	128	160	192
	PowerPC™ P	rocessor E	Blocks	_	_	_	_	-	_	-	_	_	-	-	1	1	2	2	2	2
	10/100/1000 Ether	net MAC	Blocks	_	-	-	_	_	_	_	_	_	_	_	2	2	4	4	4	4
	RocketIO™ Ser	ial Transc	eivers	_	_	-	_	-	_	-	_	_	-	-	0	8	12	16	20	24
	Commercial (slo	west to fa	istest)	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11
	Industrial (slo	west to fa	istest)	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10
	Configurati	ion Memo	ry Bits	4,765,568	7,819,904	12,259,712	17,717,632	23,291,008	30,711,680	40,347,008	51,367,808	9,147,648	13,700,288	22,745,216	4,765,568	7,242,624	13,550,720	21,002,880	33,065,408	47,856,896
Package ²	Area	MGT ³	Pins		XC4VLX25		XC4VLX60	XC4VLX80	XC4VLX100		XC4VLX200	XC4VSX25	XC4VSX35	XC4VSX55	XC4VFX12	XC4VFX20	XC4VFX40	XC4VFX60	XC4VFX100	XC4VFX140
SF363	17 x 17 mm	-	240	240	240										240					
FF668	27 x 27 mm	-	448	320	448	448	448					320	448		320					
FF1148	35 x 35 mm	 	768			640	640	768	768	768				640						
FF1513	40 x 40 mm	_	960						960	960	960									
FF672	27 x 27 mm	12	352													320 (8)4	352 (12)4	352 (12)4		
FF1152	35 x 35 mm	20	576														448 (12)4	576 (16)4	576 (20)4	
FF1517	40 x 40 mm	24	768																768 (20)4	768 (24)4
FF1760	42.5 x 42.5 mm	24	896																	896 (24)4

EasyPath solutions provide conversion-free path for volume production.
 SFA Packages (SF): flip-chip fine-pitch BGA (0.80 mm ball spacing).
 FFA Packages (FF): flip-chip fine-pitch BGA (1.00 mm ball spacing).
 All Virtex-4 LX and Virtex-4 SX devices available in the same package are footprint-compatible.







TAKE THE NEXT STEP

Visit us online at www.xilinx.com/virtex4

Quality Commitment & Policy

Xilinx is committed to excellence in quality, reliability, and on-time delivery. We strive for continuous improvement in business processes, engineering & development, service & support, and manufacturing. At Xilinx, Quality is Everyone's Business.

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BREAKTHROUGH CAPABILITIES. LOWEST PRICE POINTS EVER.

ONE FAMILY-MULTIPLE PLATFORMS

The Virtex-4[™] family of FPGAs includes three platforms, each with an optimized balance of capabilities and cost. It's a breakthrough in technology and value, only from Xilinx.

UNBEATABLE PERFORMANCE

500 MHz Clocking

Achieve the highest system speeds with flexible, precise clock control

622 Mbps—10.3125 Gbps Serial I/O

Solve your toughest serial I/O challenges.

256 GMACS Digital Signal Processing

Create ultra-high-performance DSP systems

Processor Acceleration

Build hardware accelerators easily for the 450 MHz PowerPC™ processor with the Auxiliary Processor Unit (APU) controller.

HIGHEST INTEGRATION

200,000 Logic Cells Plus Embedded Functionality

Increase effective logic capacity and decrease device cost; embedded cores deliver guaranteed performance while preserving logic fabric for custom functions.

REDUCED POWER CONSUMPTION

Save 1 to 5 Watts per FPGA

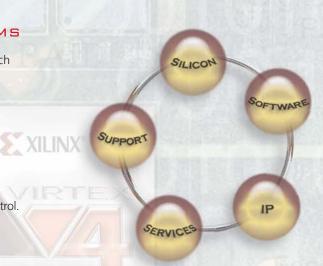
Achieve performance goals while staying within your power budget.

73% Lower Static Power

Enabled by Triple-Oxide Technology.

Up to 86% lower Dynamic Power

Enabled by abundant, flexible, embedded IP blocks.



SUPERIOR SIGNAL INTEGRITY

7x Less SSO Noise and Crosstalk

Ensure high performance, low jitter, and low error rate with advanced packing technology.

MAXIMUM PRODUCTIVITY

Complete Design Tool Suite

Speed design creation with twice the productivity of ASIC design flows. Slash debug cycle time with the advanced verification and real-time debug capabilities of ChipScope™ Pro tools.

Over 200 Pre-Verified IP Cores

Design faster and reduce risk with the latest pre-verified, pre-optimized intellectual property cores.

Education and Customized Support

Accelerate product development with online resources, training courses, and premium support services. The Xilinx Productivity Advantage (XPA) offers bundled packages of software, education, support services, and IP cores.

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Augment your development team with our worldwide network of Xilinx Design Service (XDS) and partner system design experts.

LOWEST SYSTEM COST

Freedom to Choose

Our multiple platforms enable you to select the device that most cost-effectively implements your unique application; you pay only for the capabilities you need.



Optimized for high-performance logic:

- · Highest logic-to-feature ratio
- Highest I/O-to-feature ratio



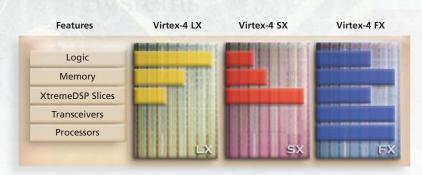
Optimized for high-performance signal processing:

- Highest DSP-to-feature ratio
- Highest memory-to-feature ratio



Optimized for embedded processing and high-speed serial connectivity:

- Embedded PowerPC and Ethernet MAC
- RocketIO™ multi-gigabit serial transceivers



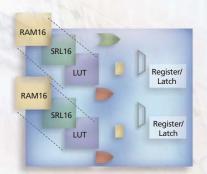
The innovative ASMBL (Advanced Silicon Modular BLock) architecture enables Xilinx to assemble FPGA platforms with varying feature mixes to meet the requirements of different application domains.



VIRTEX-4 EASYPATH

The lowest system cost just got lower with the industry's easiest, conversion-free path for volume production.

- EasyPath devices identical in every way to the FPGA—there is no risk of conversion, no hidden costs
- Enjoy unprecedented flexibility and fastest turn-around times at prices below Structured ASICs



Most Flexible High-Performance Logic Architecture

Achieve the most compact utilization.

- Up to 200,000 logic cells
- High-speed carry logic
- Configurable as logic, RAM, or shift registers









LX SX FX

500 MHz Xesium™ Clocking Technology

Obtain the highest performance with up to 80 clocks.

- 32 global and 48 regional clocks
- Up to 20 digital clock managers
- Phase precision <30 ps for better design margin
- Differential global clocking to minimize skew and jitter
- Precision phase-matched clock dividers











 Large-External • SRAM, DRAM, Flash

500 MHz Smart RAM Hierarchy

Build the right memory for any application with compact utilization and highest performance.

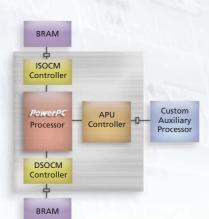
- · Configure multi-rate FIFO from block RAM without consuming logic resources
- · Block RAM with built-in Error Checking and Correction (ECC) for high-reliability systems
- Integrated source-synchronous support for easy interfaces to external memory











Enhanced IBM PowerPC™ 32-bit RISC **Processor with APU Controller**

Build area-efficient, high-performance embedded systems or complex control functions.

- 702 DMIPS @ 450 MHz; up to 1,404 DMIPS in a single FPGA with two processors
- Low power consumption: 0.45 mW/MHz
- Auxiliary Processor Unit (APU) controller makes it easy to integrate hardware accelerators









10.3125

Gbps

500 MHz XtremeDSP™ Slice

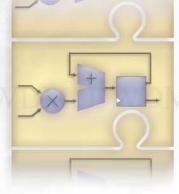
Create ultra-high-performance DSP systems.

- Up to 512 slices for 256 GMACS
- Configurable for over 40 DSP and arithmetic functions
- · Cascadable within a column at full system speed
- · Low power consumption: 2.3 mW/100 MHz at a typical toggle rate









Fourth-Generation Design Security

Safeguard your design with SecureChip AES.

Advance Encryption Standard with 256-bit key



1+ Gbps SelectIO™ Technology

simplifies board design

• 1+ Gbps differential I/O

• 600 Mbps single-ended I/O

• Digitally controlled impedance







10/100/1000 Mbps Ethernet **Media Access Controller**

Connect to the Internet via an integrated tri-mode EMAC

- UNH-verified compliance
- Built-in hard IP frees user logic resources









622 Mbps-10.3125 Gbps RocketIO™ Transceivers

Implement serial protocols to connect or bridge "anything to anything"

- Flexible SERDES with the broadest operating range supports multi-rate applications
- Compliance with the widest range of standards and protocols to connect chips, backplanes, and optical devices



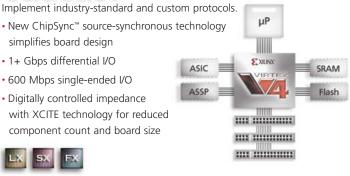












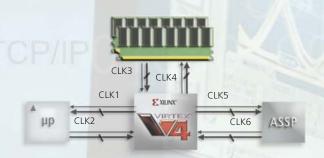


A SOLUTION FOR EVERY Servers MPLS Chip-rate Processing SYSTEM DESIGN CHALLENGE

IMPLEMENT NETWORKING AND SYSTEM INTERFACE STANDARDS

SelectIO technology, combined with pre-verified IP cores, makes it easy to support all popular interface standards and offers the flexibility to interface/bridge to virtually any external component.

- Design with PCI, RapidIO, XSBI, SPI4.2, and more
- Configure I/Os: 1.5V to 3.3V; HSTL, LVDS, and more
- Flexibly support multiple electrical standards in the same device with 16 individually configurable I/O banks



SIMPLIFY SOURCE-SYNCHRONOUS INTERFACING

ChipSync technology integrated into every SelectIO block makes it easy to create high-performance source-synchronous interfaces.

- Achieve performance targets and simplify PCB layout with flexible per-bit deskew
- Easily synchronize incoming data to FPGA internal clock with optional Serializer/Deserializer and Bitslip technology

BUILD HIGH-SPEED MEMORY INTERFACES

ChipSync, Smart RAM, and Xesium clocking technologies make it easy to interface to the latest high-speed memories.

Memory	Clock Rate	Data Rate
DDR2 SDRAM	267 MHz	534 Mbps
QDR II SRAM	300 MHz	2 x 600 Mbps
rldram II	300 MHz	600 Mbps
FCRAM II	300 MHz	600 Mbps
DDR SDRAM	200 MHz	400 Mbps

ACCELERATE DESIGN WITH COMPLETE SERIAL SOLUTIONS

Build chip-to-chip, board-to-board, and box-to-box applications quickly and easily.

- · Obtain assured compliance with multiple standards
- · Reduce system design time with pre-verified IP
- Implement custom solutions
- Reduce pin/trace count to simplify board design and reduce manufacturing cost

UPGRADE LEGACY BACKPLANES WITH 10.3125 GBPS ROCKETIO

Future-proof your backplanes with data rates adjustable to any speed from 622 Mbps to 10.3125 Gbps.

• Simplify backplane design with advanced channel equalization

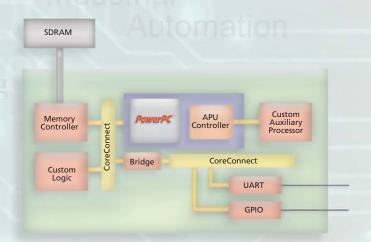
Storage	SAS 1GFC 2FGC 4GFC SATA SATA2	SAS2 8GFC 10GFC SATA3
Networking	GbE XAUI	10GbE CEI (OIF) _{Aurora} CEI (OIF)
Telecom	OC-12 OC-48	OC-192* Aurora
Computing	SATA SATA2 GbE PCIE SRIO	Aurora
Video	HD-SDI	
Rate (Gbps)	0.622 1.0 2.0 3.0	5.0 6.0 10.0

Virtex-4 FX FPGAs support all of these standards

BRIDGE PROTOCOLS

Protect your investment by interfacing easily to legacy ASSPs or ASICs.

- Implement all major protocols with pre-verified IP
- Connect external peripheral components to any processor with standards-compliant I/O



ACCELERATE PROCESSING PERFORMANCE

The PowerPC processor's APU controller makes it easy to create powerful custom co-processors in the Virtex-4 logic fabric.

- Optimize hardware/software partitioning to maximize FPGA utilization and minimize hardware cost
- Offload CPU-intensive operations such as video processing,
 3D data processing, and floating-point math

INTEGRATE COMPLETE PROCESSOR SUBSYSTEMS

Build an embedded processor subsystem custom tailored to your requirements.

- Start with the embedded PowerPC core or MicroBlaze™ soft processor core.
- Add an IBM CoreConnect bus for flexible connectivity and guaranteed performance
- Complete your subsystem with pre-verified peripheral IP cores
- Reduce design time with a ready-to-use UltraController PowerPC 405-based microcontroller subsystem package

CREATE ULTRA-HIGH-PERFORMANCE DSP SYSTEMS

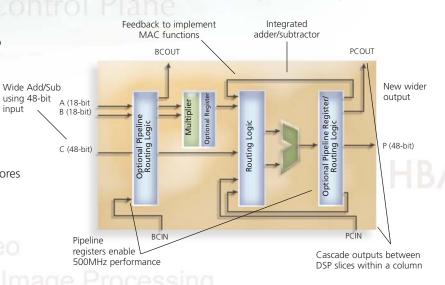
Turbocharge your DSP systems with Virtex-4 FPGAs.

- Achieve 256 GMACS performance with 512 XtremeDSP slices in a medium logic-density FPGA
- Take the performance of your favorite DSP processor to new levels by building custom pre/post/co-processing hardware
- Configure XtremeDSP slices to create more than 40 different functions, such as MACs, multipliers, adders, and Muxes, without consuming logic fabric resources or incurring logic routing delays
- Build high-performance filters by cascading slices with no loss in speed

SOLVE MULTI-CHANNEL DSP CHALLENGES

Build economical multi-channel DSP systems.

- Reduce system cost with Virtex-4 SX devices offering up to 512
 Xtreme DSP slices in a single package
- Minimize power consumption—the XtremeDSP slice consumes only 2.3 mW/100 MHz, at a typical toggle rate of 38%, that gives you only 6% of the power consumption of previousgeneration circuits
- · Achieve high compute density using SRL16 shift registers



XtremeDSP slice: increased functionality, flexibility, and performance

^{*} Payload compatible